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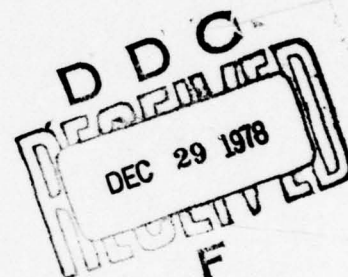
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FOREWORD

The 1978 Charge Coupled Device (CCD) Applications Conference marks the fifth such event entirely devoted to presentation of ideas, problems, and solutions in this phase of the semiconductor technology.

Pursuing the guidelines established at the first Conference in 1973 at the Naval Electronics Laboratory Center, San Diego, California, this Conference aims to reflect the impact of device concept in design of present and future systems for improved performance and lower cost. Technology has been extended to a high level of sophistication in the move from the laboratory demonstration to varied applications, such as development of focal plane infrared (IR) arrays, analog and digital signal processors, imagers, and memory components.

This year the technical presentations reflect the fact that there is more to CCD than the television camera. There are four main sessions, with a double session on signal processors. The varied areas illustrate the wide technical scope of CCD development at this period of time. Each session is structured around an invited paper which is followed by the contribution papers. The invited paper describes the device technological approach and its characteristics, and the contributed papers, in general, state current system limitations and demonstrate how the inclusion of a CCD device results in enhanced overall performance. The "Performance Characterization and Analysis" session has been included to cover specific topics common to various application areas such as radiation effects or techniques for leakage reduction, high-speed operation, and interfacing to Surface Acoustic Wave devices.

Special appreciation is expressed for the contributions of the Program Committee in producing this program.

ISAAC LAGNADO
CCD '78 Conference Chairman

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4. CCD PERFORMANCE CHARACTERIZATION AND ANALYSIS

TECHNIQUES FOR THE DESIGN OF HIGH-DENSITY HIGH-SPEED
TDI-CCD IMAGE SENSORS[*]

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ABSTRACT

New techniques are described for construction of high-speed, high-density TDI-CCD image sensors. The new design concepts incorporated in a 748x96 TDI-CCD test array were: (1) electrode-per-bit clocking of the TDI array which increases vertical resolution, (2) two types of 4:1 output register multiplexing to increase the horizontal resolution, and (3) charge-gating multiplexer and temporary one-horizontal-line storage to achieve a high performance transfer of data from the TDI array to the multiplexed output registers.

A. INTRODUCTION

New techniques are described for the construction of high-speed, high-density charge-coupled image sensors which can be used in future Electronic Message Service systems. An example of one potential application is a high-speed page-reader that would be capable of processing up to 20 standard pages per second. This CCD sensor would have 1728 or 2200 horizontal picture elements and, for improved sensitivity up to 96 time-delay and integration (TDI) vertical elements. The new design concepts required for such a CCD sensor were implemented in a 748x96 element TDI-CCD test array, which was designed and fabricated to study the feasibility of a full-size high-speed 2200x96-element TDI-CCD sensor with 4:1 multiplexed output [1]. The following new techniques were incorporated into this test array:

1. Electrode-Per-Bit Clocking of the TDI Array

The concept of electrode-per-bit clocking, that is now widely used in the area of

CCD memories [2,3], was adapted to increase the vertical resolution of the TDI sensor. With four-phase electrode-per-bit clock the vertical resolution of the TDI sensor is increased by a factor of 1.5 above the value obtained for the same gate structure operated with the conventional two-phase or four-phase clock.

2. Output Multiplexing

By using the horizontal output multiplexing a CCD area image sensor can be constructed with very high horizontal resolution that is not limited by the definition of the serial output register [4]. However, in addition to allowing higher horizontal resolution, the output multiplexing also provides an increase in the effective serial scanning rate of the TDI array.

3. High-Speed TDI Multiplexer

A new charge-gating structure has been incorporated in the 748x96-element test array. With this new technique high resolution 2:1 and 4:1 multiplexing of the TDI output can be achieved. Also to minimize the time required to load the four parallel output registers, the concept of a temporary line storage register has been introduced into the multiplexer section. Before discussing these new techniques in detail,

it is necessary to consider possible approaches to page-reader systems.

B. HIGH-SPEED CCD PAGE READER SYSTEMS

To satisfy the requirement of reading up to 20 pages per second, a 2200 element line reader CCD sensor should be capable of a horizontal scanning rate of 84 MHz. Since it is difficult to provide drivers for clocking the CCD output register much above 21 MHz, the readout of this array must involve some form of output multiplexing. The four different systems with 4:1 multiplexed outputs considered for this purpose are illustrated in Fig. 1.
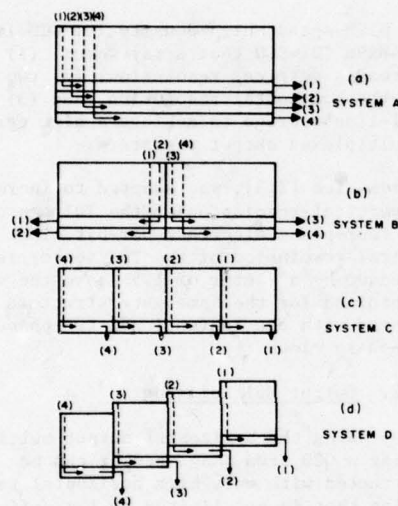
Fig. 1. System organization for TDI array with 4:1 multiplexed output.

System A shown in Fig. 1(a) represents the approach with 4:1 multiplexed output that is capable of the highest horizontal resolution. In this system every four adjacent pixels of the sensor array are transferred into four adjacent horizontal CCD output registers as will be shown. System B, shown in Fig. 1(b), is split into two sections, each having a separate set of 2:1 multiplexed registers. System C, shown in Fig. 1(c), provides the output signals from four simultaneously scanned output registers.

This system represents four smaller sensors in adjacent locations designed to form a single and continuous (in the horizontal direction) optical sensor. System D, see Fig. 1(d), was suggested by Frank Martin of Naval Ocean Systems Center. This system is similar to System C, but is designed with each adjacent section (from right to left) displaced down one line of TDI delay. In this system a sequential reading of sections 1, 2, 3, and 4 provides a readout of one continuous line of the TDI sensor array.

A more detailed description of the 4:1 and 2:1 output multiplexing used in Systems A and B is given in Sections D and E. The main advantage of using such horizontal output multiplexing in the design of CCD image sensors is that it allows an increase in the horizontal resolution without the requirement of a simultaneous decrease in the stage length of the output register. This, however, also imposes a trade-off between the improvement in the horizontal resolution and a limitation on the maximum clock frequency at which the output register can be operated with low transfer losses. This loss in transfer efficiency due to the higher order of horizontal output multiplexing is due to the proportionally longer gates in the output register.

The main advantage of an approach such as that used in Systems C and D is that it is not limited by the frequency response of the output registers. However, at the same time this form of output multiplexing imposes the restriction that the length of the pixel in horizontal direction be equal to the length of one stage of the output register.

Finally, a compromise between the improvement in the horizontal resolution and the maximum allowable frequency response is achieved in system B, as shown in Fig. 1(b). This type of splitting of the imager into two parallel sections can be used also to achieve an 8:1 multiplexed output in the form of two sets of 4:1 multiplexed outputs. Such an approach may be desirable if the frequency response of System A is too low to satisfy the required effective serial output scanning rate of 8.4×10^7 pixels per second, and the construction of System B imposes too-small feature length for the design of the dual 2:1 horizontally multiplexed output registers.

C. GENERALIZED ANALYSIS OF MTF ROLLOFF DUE TO TIME-DELAY AND INTEGRATION

The time-delay and integration mode of operation is required since sensitivity must be increased due to the low levels of illumination used in page-reader systems. However, MTF degradation occurs in the TDI mode because the image is moving at a constant velocity while the collecting potential wells move with a "jerky" motion. Thus, the center of the collecting well will move relative to the image with a periodic motion, falling behind, and then jumping ahead, etc. The degree of the MTF degradation due to this effect depends upon the details of the clocking scheme, the gate dimensions as well as the spatial frequency of the pattern being imaged. The following discussion is a generalized analysis of the contrast transfer function (CTF, appropriate for square wave patterns) for electrode-per-bit clocking with unequal gate lengths and three-phase clocking for unequal gate lengths.

1. CTF for Electrode-Per-Bit Clocking of a TDI Sensor

As shown in Fig. 2, this discussion assumes a generalized electrode-per-bit clocking scheme consisting of pairs of
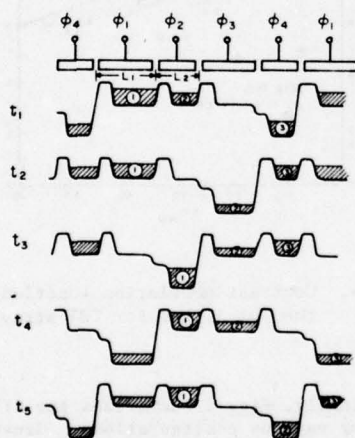
Fig. 2. Operation of a TDI array with four-phase electrode-per-bit clocking, illustrating the presence of the three variable sizes of pixels for each four electrodes.

gates, one of length L_1 and the other of length L_2, in which p packets are stored under p + 1 gates. Each gate consists of a storage region and a barrier. P + 1 clocks would be required for this scheme. Figure 2 illustrates the progress of a charge packet for p + 1 = 4. After three clock transitions (t = t_4), each packet has moved one gate ahead - one quarter of a full stage. Thus, it takes p(p + 1) clock transitions to move the charge pattern to the right one full stage.
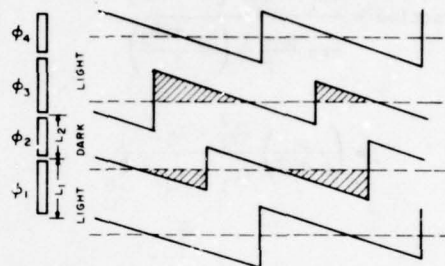
Fig. 3. Position of the collection wells of the TDI array with four-phase electrode-per-bit clocking relative to the moving image in the form of light and dark bar pattern.

Figure 3 shows the position of the collecting wells relative to the moving image (i.e., the reference is assumed to be moving with the image) as a function of time for p + 1 = 4. Six time periods are shown. The light pattern shown corresponds to the Nyquist limit. The relative speed between a stationary well and the image is

$$\left(\begin{array}{l}\text{length of} \\ \text{full stage} \\ \hline \text{time to transit} \\ \text{full stage}\end{array}\right) = \left(\frac{(p+1)\frac{L_1+L_2}{2}}{p(p+1)\,\Delta t}\right) \quad (1)$$

where Δt is the time between clock transitions, i.e., $f_{clock} = 1/(p + 1)\,\Delta t$. The shaded areas indicate the regions where the collecting well centered on the dark part of the image extends into the light regions.

The area of the larger triangular shaded

region is $\frac{1}{2}\left(\frac{L_1}{2}\right)\left(\frac{L_1}{2}\right)\left(\frac{2p\Delta t}{L_1 + L_2}\right)$. The smaller

area is $\frac{1}{2}\left(\frac{L_2}{2}\right)\left(\frac{L_2}{2}\right)\left(\frac{2p\Delta t}{L_1 + L_2}\right)$. There is one

of each such triangular areas for every p time periods. Therefore, the fraction for dark in light is

$$\text{Fraction} = \frac{\frac{\Delta t p}{(L_1 + L_2)}\left[\frac{L_1^2}{4} + \frac{L_2^2}{4}\right]}{\Delta t p \frac{p + 1}{p}\left(\frac{L_1 + L_2}{2}\right)} \quad (2)$$

$$= \left(\frac{p}{p + 1}\right)\frac{(L_1^2 + L_2^2)}{(L_1 + L_2)^2}\frac{1}{2}$$

The contrast is reduced by twice this amount since the light wells spend an equal time in the dark, so that

$$\text{CTF} = 1 - \left(\frac{p}{p + 1}\right)\frac{(L_1^2 + L_2^2)}{(L_1 + L_2)^2} \quad (3)$$

In this case the resolution center-to-center spacing is given by:

$$D = \left(\frac{p + 1}{p}\right)\frac{(L_1 + L_2)}{2} \quad (4)$$

An example of such a structure would be $L_1 = 10$ µm, $L_2 = 7.5$ µm and $p + 1 = 4$. Here the resolution center-to-center would be 11.7 µm and the CTF at the Nyquist limit would be 0.61735. If all the gates were 10 µm, the center-to-center spacing would increase to 13.3 µm and the CTF would increase only slightly to 0.62500. Therefore, using $L_2 = 7.5$ µm vs 10 µm would provide a 10% decrease in chip size at a negligible change in CTF.

2. CTF for Three-Phase Clocking

This discussion assumes a standard three-phase clocking scheme but with unequal gate lengths, L_1, L_2 and L_3. Using an analysis similar to the ripple-clocking case, the CTF can be shown to be:

$$\text{CTF} = 1 - \frac{11(L_1^2 + L_2^2 + L_3^2) - 2(L_1 L_2 + L_1 L_3 + L_2 L_3)}{36(L_1 + L_2 + L_3)^2} \quad (4)$$

The resolution center-to-center spacing is:

$$D = L_1 + L_2 + L_3 \quad (5)$$

An example is a three-phase device with $L_1 = 7.5$ µm, $L_2 = 5$ µm, and $L_3 = 5$ µm. Here the resolution center-to-center is 17.5 µm and the CTF is 0.91213. If the gates were all equal to 7.5 µm, the resolution center-to-center would be 22.5 µm and the CTF 0.91667.
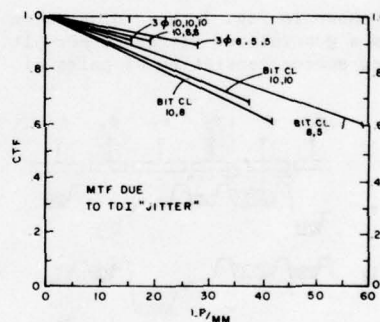
Fig. 4. Contrast modulation function due to the TDI jitter for TDI array.

Finally, Fig. 4 summarizes the CTF rolloff for various configurations. Generally the electrode-per-bit clocking approach results in smaller pixel dimensions and correspondingly higher Nyquist limits but more CTF rolloff. The three-phase approach has better CTF characteristics but larger dimensions.
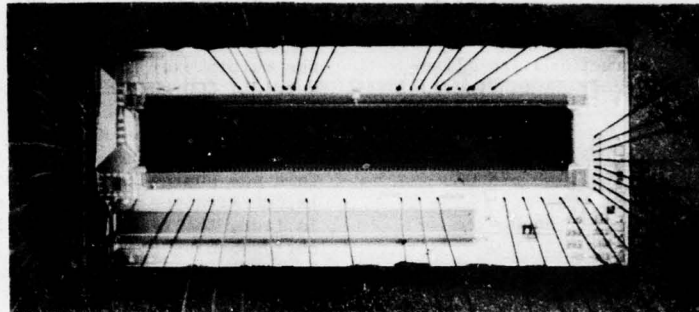
Fig. 5. Page-reader test chip.

D. PAGE-READER TEST CHIP

The photomicrograph of the 14.5 mm x 5.9 mm page-reader test chip is shown in Figure 5. The masks for this chip were masterplates photocomposed from three reticles. The page-reader test chip was fabricated with two-level polysilicon buried-channel CCD technology. A 748x96-element TDI-CCD line sensor with a 4:1 multiplexed output (System A in Fig. 1) was chosen as the main device for the page-reader test chip. The 748x96-element array represents about 35% of the area of the 2200x96-element TDI line sensor, and it contains all of the features necessary for construction of the full-size page reader.

To achieve an effective resolution in the TDI array of 15 µm x 15 µm pixels, the TDI electrodes were designed with 8 µm gates and 3 µm spaces for both levels of polysilicon. The resulting 11 µm electrodes in conjunction with 4-phase electrode-per-bit clocked TDI array results in an effective vertical pixel dimension of 15 µm. The horizontal pixel dimension of 15 µm has been defined by 10 µm TDI-CCD channels and 5 µm channel stops. In addition to the 4:1 output, the 748x96-element TDI array can be read out by a double 2:1 multiplexed output register (System B).

A block diagram of the test array is shown in Figure 6. The main structural difference between the two types of 4:1 multiplexed outputs is that in the case of

4:1 multiplexed output (shown on the bottom), the output registers have 60 µm long CCD stages, while in the case of the double 2:1 multiplexed output the output registers have 30 µm long stages. The advantage of the 4:1 multiplexed output registers with 60 µm stages is that they can be laid out with two-level polysilicon gates using rather non-critical design rules. The layout of 2:1
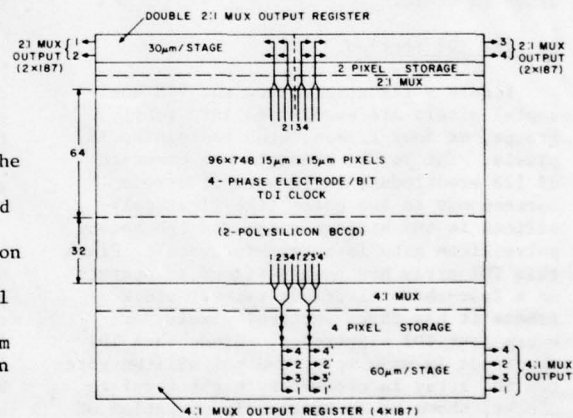
Fig. 6. Block diagram of 748x96-element TDI-CCD line sensor with 4-phase electrode-per-bit TDI clock and two types of 4:1 multiplexed outputs.

multiplexed output registers with 30 μm stages, on the other hand, requires much tighter design rules. The advantage of the double 2:1 multiplexed design is that it offers a higher speed capability. The layout details of the output registers of both the 2:1 and the 4:1 structures are illustrated by the photomicrograph in Figures 7 and 8, respectively.

E. CONSTRUCTION AND OPERATION OF 748x96-ELEMENT TDI-CCD LINE SENSOR

1. General Description of the Device

In this section a more complete description will be given of the construction and the operation of the 4:1 multiplexed output of this TDI array. A schematic sketch of the complete 748x96-element TDI array with 4:1 multiplexed output is shown in Fig. 9. The second-level polysilicon gates are illustrated in this figure by solid lines. The first-level polysilicon gates are shown as dotted lines. In the actual layout the second-level polysilicon gates overlap the first-level polysilicon gates. For simplicity, the first-level polysilicon gates are shown in Fig. 9 as narrower than the actual size. In fact, the spaces between the second-level polysilicon gates in the direction of the CCD channels are intended to represent the length of the first-level polysilicon gates, however, they are not drawn to scale.

2. The TDI Section

Figure 9 illustrates how the 748 horizontal pixels are subdivided into four groups, or four frames, each containing 187 pixels. The 96 TDI elements are composed of 128 electrodes, where each electrode corresponds to two gates (the first polysilicon is the storage gate, and the second polysilicon gate is a transfer gate). Since this TDI array has been designed to operate on a four-phase electrode-per-bit clock scheme it has three vertical pixels for every four TDI electrodes. Since each TDI electrode is made up of two polysilicon gates, the TDI array is clocked by eight separate clocks, shown as ϕ_1 to ϕ_8. In operation of the array, the pairs of clocks ϕ_1 and ϕ_2, ϕ_3 and ϕ_4, ϕ_5 and ϕ_6, as well as ϕ_7 and ϕ_8 have the same waveforms but different dc voltage levels.

3. The 4:1 Multiplexer and Temporary Storage Register

The output from the TDI image sensor section is transferred directly into the parallel to serial multiplexer section. In the multiplexer section, every fourth vertical CCD channel is routed into one of the four horizontal CCD channels. The clocks M1 through M7 are used to provide the timing to clock the charge through the multiplexer. This new charge gating technique allows a layout with very high horizontal resolution. In fact, the resolution of this TDI array, corresponding to 15 μm x 15 μm pixels is limited mainly by the vertical resolution, which in turn is limited by the minimum practical gate length of the TDI array.

Two novel techniques have been developed for the multiplexer section. One technique uses a "window-gate" structure and the other uses ion implanted barriers to control the charge flow in the multiplexer.

The operation of the "window-gate" 4:1 signal charge multiplexer is illustrated in Figs. 10 and 11. This parallel-to-serial signal-charge gating is accomplished by two sequential binary switches. The first charge switch is formed by gates M1 and M2 which separates the channels 1 and 3 from channels 2 and 4. The window gate shown in a top view of Fig. 9 is shown in cross-sectional view in Fig. 10. The cross-sectional structure in Fig. 10(a) applies only to channel 2 and 4. The first polysilicon gate, M1, over these two channels contains a window and the second polysilicon gate that covers this window can be used to control the channel potential in the window. The other channels (1 and 3) have a continuous gate M1 and the charge transfer in that case is conventional.

The ideal operation of the charge gate shown in Fig. 10(a) is illustrated by the potential profile in Fig. 10(b). In this case, when gate M2 forms a barrier (as is illustrated by the solid line in Fig. 10(b)), the signal charge will be prevented from being transferred into the potential well under gate M4. But, when gate M2 is turned on (as is illustrated by the dotted lines), the signal charge originally stored under the left-hand part of gate M1 will be completely transferred to the potential well
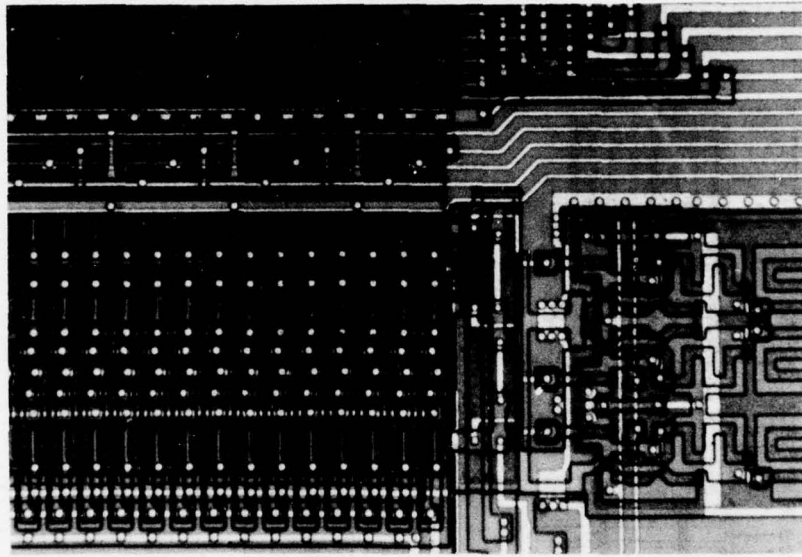
Fig. 7. The output section of the dual 2:1 multiplexed output registers.
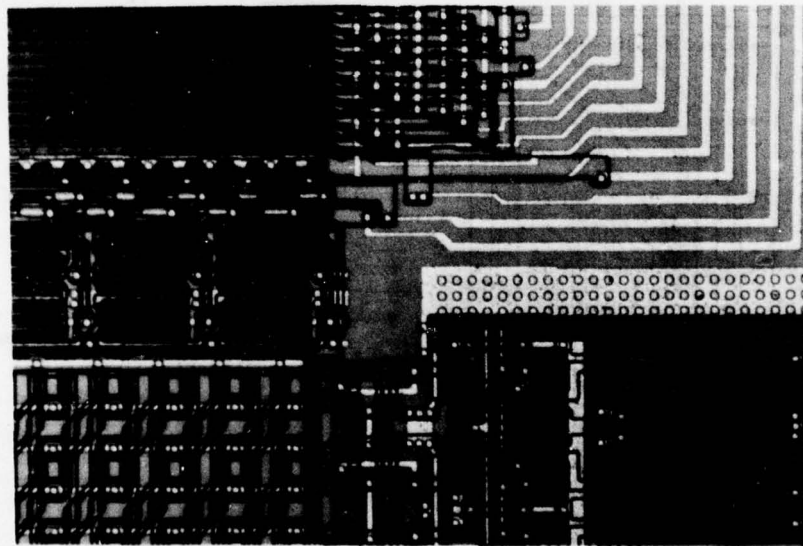
Fig. 8. The output section of the 4:1 multiplexed output registers.
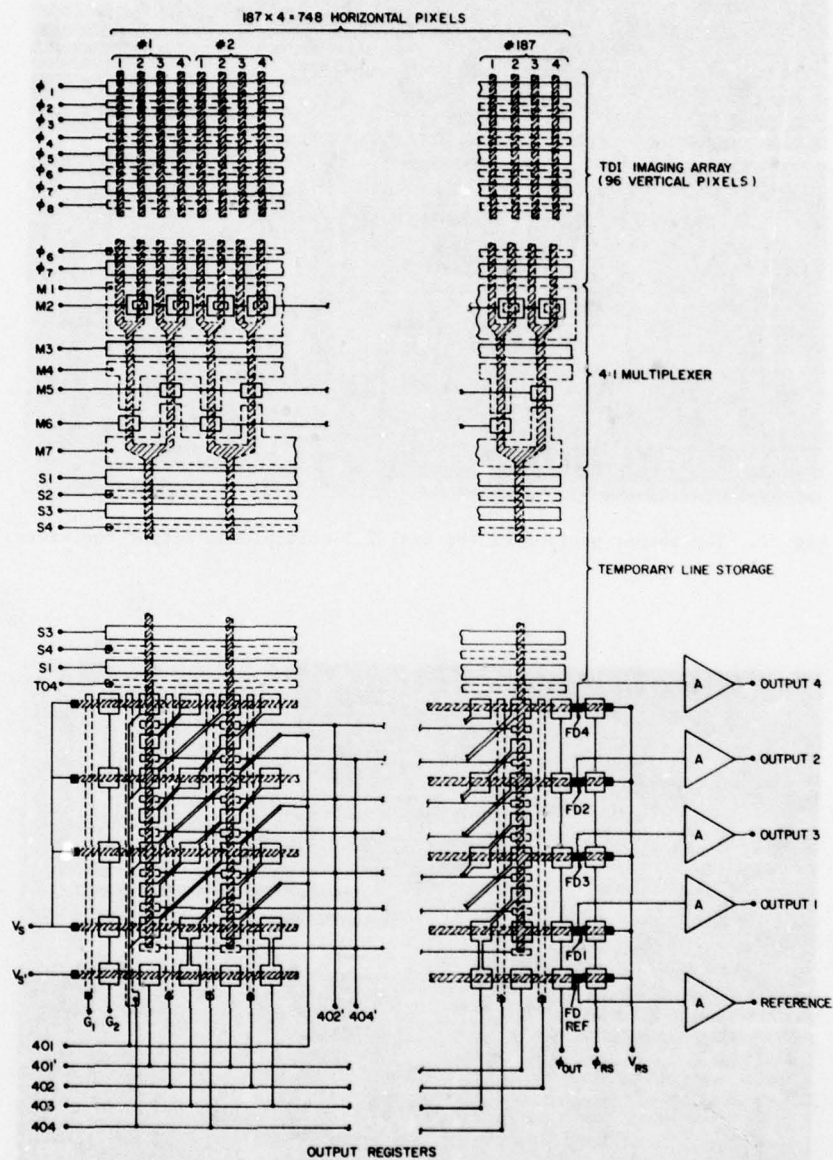
Fig. 9. Schematic layout of the 748x96-elment array with 4-phase electrode-per-bit TDI clock and 4:1 multiplexed output.

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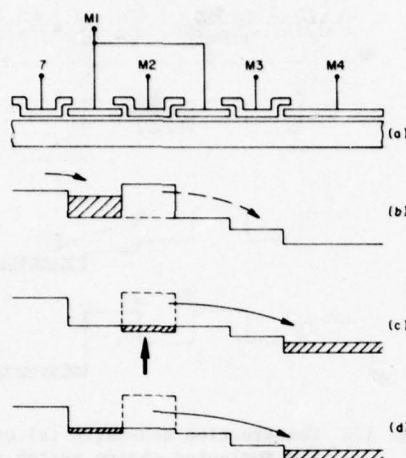
Fig. 10. Construction schematic (a) of the "window-gate" charge switch used in the 748x96-element array as the first 2:1 multiplexer in Fig.9, and its operation (b), (c) and (d).

Fig. 11. Construction in (a) and (c), and operation in (b) and (d) of the "interleaved gate" charge switch used as the second 2:1 multiplexer.

under gate M4, which is the receiving well for the next charge multiplexer section.

In actual operation, it is difficult to maintain the channel potential under gate M2 exactly equal to the channel potential under gate M1. Therefore, this charge gate must be operated in one of the modes shown in Fig. 10(c) or Fig. 10(d). Consider the mode illustrated in Fig. 10(c). During the transfer of the charge signal from the well under the left part of gate M1 a potential well is formed under gate M2. This well will momentarily trap some of the signal charge. However, it is possible to make a substantially complete charge transfer, if the fall time of the clock M2 is relatively slow. A slow fall time of M2 will assure that all the original charge under gate M2 is pushed from this well into the potential well under gate M4. Thus, no appreciable amount of charge can be trapped under the left-hand part of gate M1. However, any charge trapped at this position will tend to degrade the vertical MTF of the imager.

The second mode of operation of the charge gate is illustrated in Fig. 10(d). Here, during the transfer of charge to the potential well under gate M4, a potential barrier is formed under gate M2. Due to this potential barrier some charge will always be left behind under the left part of gate M1. This mode of transfer is referred to as incomplete transfer or bucket-brigade mode of operation and contributes to the device transfer loss. In steady-state operation with a bias signal, a fat zero, a typical transfer loss for this type of transfer is on the order of 10^{-3}. However, even without a fat zero, the expected charge transfer loss in this case is expected to be on the order of 10^{-2} (or 1%), which should have a negligible effect on the MTF of the TDI array.

The most important advantage of the first 2:1 multiplexing by the window-gate is that it can be accomplished with very high resolution. The second charge switch is accomplished by the interleaved gates

M4 and M7 which allow the charge to be transferred either by the transfer gate, M5, as is shown in Figs. 11(a) and (b), or by the transfer gate, M6, as is illustrated in Figs. 11(c) and (d). From the operational point of view, this second switch is much more straightforward, however, it does not allow the packing density that is possible with the window gate.

The operation of the implanted 4:1 multiplexer is very similar in operation to the previous approach except the window and the interleaved gates are replaced by implants. A cross-section of channel two is shown in Fig. 12. Channel one has an identical gate structure without the ion implanted regions. Initially the charge is transferred into the storage well under gate M3 in both channels. If M4 goes to an intermediate value between its low and high value, the charge in channel one will flow into the M5 electrode area. However, the charge in channel two will remain under the M3 electrode because of the potential in the ion implanted region. After the charge in channel one has been clocked to the desired location, M4 can be clocked to its high value which will allow the charge under M3 in channel two to flow into the M5 electrode area. The two parallel charge packets have now become serial packets. This structure can be repeated horizontally and vertically for the desired 2:1 and 4:1 multiplexing structures. The advantage of the ion implanted structure is that all gates can have the same minimum geometry and therefore packing density and transfer efficiency is improved. In addition, bucket-brigade mode operation is avoided. However, it does require an extra implant step and slightly more complicated clocking waveforms.

The loading time of the output registers can be minimized by incorporating a temporary storage register which holds four pixels from the multiplexer section, see Fig. 9. The temporary storage section of the array corresponds to four stages of two-phase CCD registers which are powered by clock phases S1 to S4. Here, S1 and S3 are transfer gates, and S2 and S4 are storage gates. The function of this temporary storage register is to allow essentially a full line readout time for multiplexing the TDI output by loading the parallel output regis-
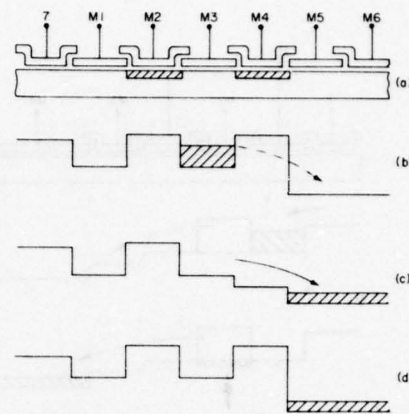
Fig. 12. Construction schematic (a) of the ion implanted charge switch which can be used as a 2:1 multiplexer and its operation (b), (c) and (d).

ters in minimum time. The output register loading time in this design should take about 2.0 μs, or less than 10% of the minimum line readout time. To insure the minimum time for the loading of the output registers, all of the gates involved in this type of transfer have been strapped by aluminum busses.

The temporary storage register is separated from the output register by a transfer gate, T04.

4. The Output Register Section

The construction of the output registers is shown in Fig. 7, 8 and 9. Although this is a schematic representation, it illustrates the general stategy used for the layout of the output registers. There are actually five parallel output registers. Each of these registers has 187 two-phase stages, an electrical input, and a high-speed, source follower output amplifier. The first four output registers serially read out the 4:1 multiplexed output of the TDI array. The fifth output register has been included in this design to serve as a reference channel

for differentially canceling the clock pick-up in the outputs.

The two-phase clocks for the operation of the output registers consist of clock phases 401, 401', 402, 403, and 404; where the clocks 401, 401', and 403 drive the transfer gates and the clocks 402, and 404 drive the storage gates. Other gates and timing clocks for the output register are the input gates, G_1 and G_2. The last gate before the floating diffusion, FD, is ϕ_{OUT}. The gate resetting the floating diffusion to the drain potential V_{RS} is ϕ_{RS}. The voltage V_S is the voltage driving the source diffusions of the first four output registers. The fifth, the reference register, has a separately controlled source diffusion voltage, V_S', so that an independent charge signal can be introduced into the reference register during the readout of the TDI array by the first four registers. In this case, the four output registers will be operated without the electrical input.

The data transfer from the temporary storage section into the output registers is described in the following. In this charge transfer the four-stage temporary storage registers are clocked together with the four output registers in an inter-register transfer mode. The contents of the temporary storage registers are trans-ferred to the four output registers, by a two-phase interregister clocking scheme. The clocks involved in this transfer are S1 to S4, T04, 401, 403, 402', and 404'. During this vertical transfer from the temporary storage section into the output registers, the clock phases 402 and 404 act as channel stops preventing the charge from flowing horizontally in the output registers. Conversely, during the horizon-tal readout time, the clock phases 402', 404' and T04 act as channel stops, prevent-ing charge flow in the vertical direction.

The floating diffusion, FD, output of each channel is amplified by a three-stage MOS amplifier, to provide maximum dynamic range and frequency response up to the clock frequency of 21 MHz. The first two stages are designed to operate as source followers. The first stage is followed by a sample-and-hold circuit to reduce the output clock noise. The second stage isolates the sample-and-hold circuit from the high-capac-itance output device required to drive the load.

F. CONCLUSION

The new CCD imager design concepts in-corporated in the 748x96-element page-reader test array include:

(1) Electrode-per-bit clocking of the TDI array to increase vertical resolution.

(2) Output register multiplexing to in-crease horizontal resolution and the effec-tive read-out rate.

(3) Charge-gating multiplexer and temporary one-horizontal-line storage to achieve a high performance transfer of data from the TDI array to the multiplexed output registers.

ACKNOWLEDGMENT

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HIGH RESOLUTION IMAGE LINE SCANNING WITH AN AREA IMAGE SENSOR

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A technique is discussed which can be used to achieve high resolution image line scanning with a low resolution area detector array. The image illuminates a metallized mask which is either fabricated as the top layer of the array or is fabricated separately and relay imaged onto the array. The mask is opaque except for small clear apertures which are located over the detector elements. These apertures are equal in size to one picture element (which is a small fraction of the size of one detector element) and have locations which are staggered sideways from one row of detectors to the next. As a two dimensional image is moved vertically past the mask, any given picture element along a horizontal line is sampled by only one row of detectors. The picture elements read out in each frame of data are thus distributed over several lines in the image. They are "destaggered" in a shift register buffer or computer memory to achieve a properly formatted image. The linear scan resolution obtainable using such a technique is equal to the total number of detector elements in the array, despite their rectilinear layout.

A breadboard document scanner was set up to demonstrate this basic concept. A commercially available area CCD detector array having 190 x 244 elements was used in conjunction with a separately fabricated metal mask and relay optics. The mask format consisted of 15 rows of apertures, with 190 elements per row, resulting in a net line scan resolution of 2850 elements. The array design was of the interline transfer type, with 190 columns of detectors and every other row interlaced. For this experiment, the top few rows of each interlaced frame were read out at an average data rate of 5 MHz, with the remaining rows rapidly dumped into the output shift register to clear dark current. This resulted in a frame rate of 250 frames per second. Data was single level thresholded, read into a high speed FIFO, and then destaggered using a NOVA computer. Results are shown which demonstrate the full resolution capability of the system, without artifacts produced by the "staggered aperture" technique.

I. Introduction

The most commonly used technique for reading high resolution imagery into an electronic data system makes use of an image line scanner. This line scanner is used in conjunction with a relative cross-scan motion between the object and the viewing system to achieve raster input scanning. Such a system is diagrammatically shown in Figure 1, where an object, which could be an original scene, a photograph, or any other two dimensional set of data, is imaged onto a linear CCD detector array. As the array is repetitively read out to detect image intensity, the object is translated perpendicular to the scanning direction to achieve raster scanning of this image data. The resolution (as measured in total number of resolvable picture elements) is limited by the number of detector elements in the linear scanner. The number of elements which can be fabricated in such a single solid state device is determined by the maximum allowable chip length divided by the minimum detector size, and is limited by the particular photolithographic process and such things as allowable yields, shift register CTE's, and minimum barrier heights.

This paper proposes an alternative way to perform line scanning which uses an area image sensor to achieve a scan resolution equal to the total number of
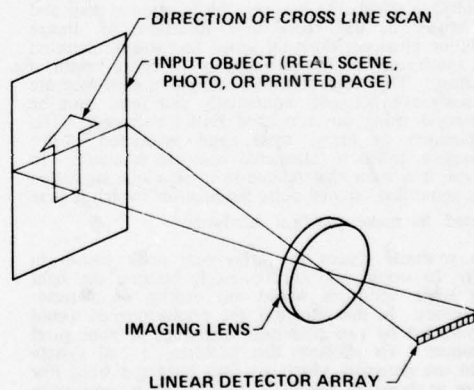
Fig. 1   Image line scanner

detector elements in the area image sensor independent of their orientation in rows and columns. A superimposed metalized mask and an auxilliary data buffer are used to achieve much higher resolution scanning than obtainable with a single linear detector chip, since the chip length/detector size limitation is no longer important.

II. Concept Description

The basic concept is explained using the diagram in Figure 2a. A two dimensional strip region of the scene to be scanned is imaged onto an area detector array consisting of a number of rows of detector elements. The magnification is such that the entire length of the region to be scanned is imaged onto the length of one row on the array. This imaged line length has the full number of desired image resolution points, but these are not fully resolved by the detector array which has a smaller number of elements per line. To enhance the resolution, an opaque mask is placed over the detector array as shown in Figure 2b, which has small clear apertures in it which allow light from only one image resolution point to fall on each detector. As shown in Figure 2b, the positions of the holes in front of each detector are staggered so that each row of detectors sees a set of image resolution elements along one line, with the element positions staggered from line to line. As seen in the figure, each time the array is read out, the number of image samples taken is equal to the total number of detector elements in the area array, but they are spread out over a number of lines in the image. By providing a translation between the imaging system and the object in the cross scan direction, all image resolution elements along an image line will be detected once the image line has moved past the entire height of the array. The resolution elements along each line are obviously not detected sequentially and must thus be rearranged using an associated buffer memory. The combination of array, mask, and associated buffer memory is called a "staggered aperture scanner". In concept, it is somewhat related to a technique suggested years ago called "spatial pulse modulation" which is here adapted to make practical hardware.[1]

In a practical system the array and mask shown in Figure 2b would not work properly because the light from some apertures would fall exactly on detector boundaries. In this situation, the photoelectrons would be collected by two photosites, resulting in poor pixel definition. To alleviate this problem, a real system would use detectors which are also staggered from row to row as shown in Figure 2c, to allow each aperture to be centered on the appropriate detector.

One possible modification of the system described above makes use of anamorphic optics. In this case, shown in Figure 3a, the optics are designed to image square picture elements on the object as tall rectangular picture elements on the array. The mask for this case has tall rectangular apertures as shown in Figure 3b. The height of these apertures could extend anywhere in the range
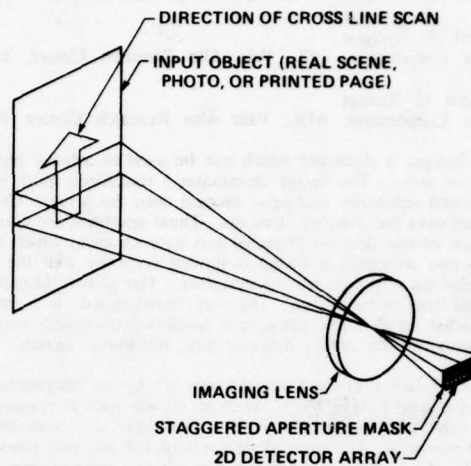
Fig. 2a.   Staggered aperture scanner

Fig. 2b.   Staggered aperture mask for 6 row detector array

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DIRECTION OF RELATIVE
OBJECT MOTION

CLEAR APERTURES

DETECTOR ELEMENTS
(STAGGERED)

■ SIZE OF IMAGE RESOLUTION ELEMENT
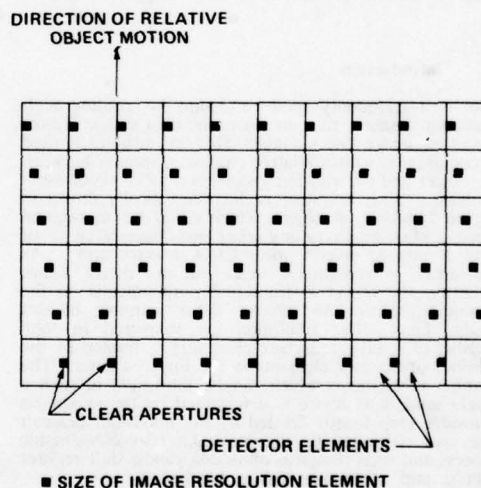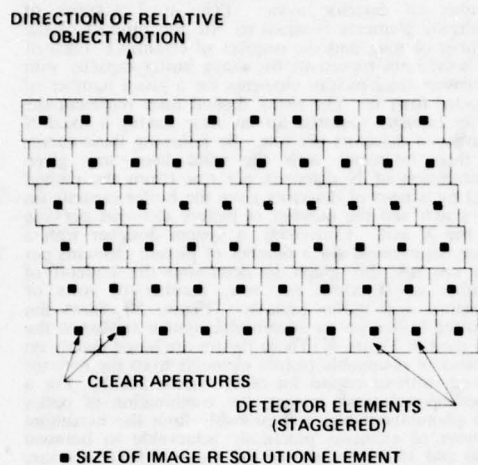
Fig. 2c. Staggered aperture mask for 6 row detector array showing optimum detector positions which are staggered sideways to line up with apertures.

from equal to the aperture width (conventional case) to equal to the height of the entire array. As the anamorphic ratio gets larger, however, the optics become difficult to build at the f/#'s required for high speed operation.

It is important to note that the total number of picture elements per line obtainable using any of these staggered aperture techniques is not affected in any way by the number of rows of detectors (which is presumed to be easily extendable to at least 32 or 64), but is instead affected only by the length of the array and the aperture spacing. If L is the length of the array and Λ is the aperture width (normally assumed equal to the pixel spacing), the total resolution capability of the array is given by L/Λ. This total number of resolution elements is thus limited by the achievable chip length L and the minimum aperture size Λ for a detector array with a superimposed mask. For larger numbers of picture elements per line, the minimum aperture size producable by a given photo-lithographic process may thus determine the ultimate resolution capability. (As one example, if the chip length L were 28 mm and the aperture size Λ were 4 microns, a single chip staggered aperture scanner would have a net resolution of 7000 elements). To extend the technology further, a relay imaging system such as shown in Figure 4 may be used, where the mask is actually larger than the detector array, but is demagnified down onto the detector array. This allows for substantially greater extension of resolution

DIRECTION OF CROSS LINE SCAN

OBJECT

ANAMORPHIC OPTICS

ANAMORPHIC STAGGERED APERTURE MASK

AREA DETECTOR ARRAY
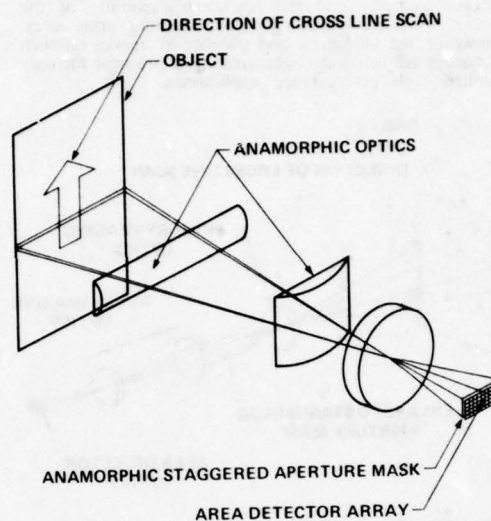
Fig. 3a. Staggered aperture scanner with anamorphic optics

DIRECTION OF RELATIVE
OBJECT MOTION

CLEAR APERTURES

DETECTOR ELEMENTS

▌ SIZE OF IMAGE RESOLUTION ELEMENT

Fig. 3 b. Anamorphic staggered aperture mask (anamorphic ratio equal 6).

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capability, since resolution is only limited by the mask photolithography and the resolution capability of the optics, with less concern for long detector array sizes. However, the alignment and stability tolerances on such a system are relatively tight, making it practical for only limited high performance applications.
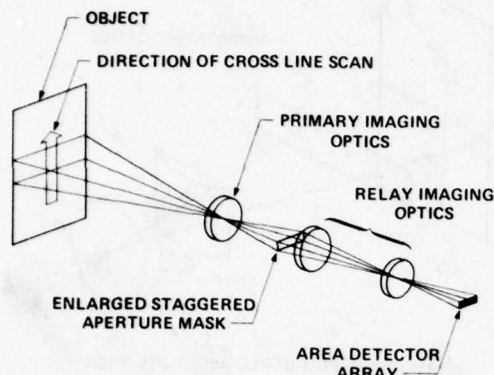
Fig. 4.   Staggered aperture scanner using relay optics

Destaggering

The required "destaggering" algorithm needed to rearrange the picture elements in the buffer memory is a very simple storage operation which is understood as follows.   Considering the image of a single line of data on the object, it is first translated into position under the bottom row of detectors. After readout, the image line is translated up where it is sequentially read out by each row of detectors. The destaggering algorithm is simply the following: the data read from the bottom row of detectors must be stored until the line has been translated to the top row, at which time all picture elements along the line have been read, and the line can be reconstructed. Picture elements detected with the row of detectors next to the bottom must also be stored until the line of input data is translated to the top row, but the storage time is less because the line elements read were detected by this row at a later time.

The complexity of the buffer required for this operation is determined primarily by its storage capacity, which is calculated as follows. If n is defined as the number of rows of detectors, N as the number of detectors per row, and n' as the number of picture lines between detector rows (which equals n-1 for a nonamorphic system and equals 0 for the anamorphic optics shown in Figure 3), then the required pixel storage capacity in picture elements is given by

$$\text{buffer size} = N[n' + 1] [(n-1) + (n-2) + \ldots + 1].$$

This formula can be used to calculate the capacity for a system using nonanamorphic pixel elements such as that shown in Figure 2. This capacity is plotted in Figure 5a as a function of the total number of resolution elements per line, for a number of different values of n, the number of detector rows.   (The total number of resolution elements is equal to Nn, the product of the number of rows and the number of columns.) Each of the solid lines represents the rising buffer capacity with increasing total picture elements for a given number of detector rows n. The rising dashed lines represent the buffer capacity required for an array having a fixed N number of detectors per row. By following these curves to their intercepts with the solid lines, any given combination of N detectors per row (from the dashed line) by n rows of detectors gives the buffer capacity on the y axis and the number of picture elements per line on the X axis. Conversely, a system designer with a given requirement for a number of picture elements per line can use this graph to determine the tradeoff of number of detectors per row, number of rows of detectors, and buffer capacity. Figure 5b shows the required buffer for an anamorphic system similar to the one used in F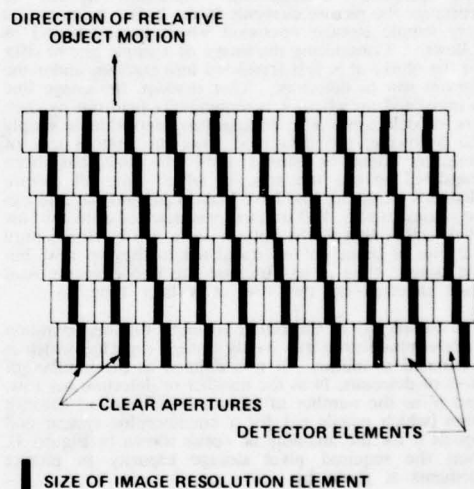igure 4. These figures are based simply on number of obtainable picture elements from the detector system, without regard for other system details. For a superimposed mask imager, the combination of optics and photolithography will probably limit the maximum number of elements practically achievable to between 5000 and 10000 because of the required small aperture size.   A more complicated relay setup such as shown in Figure 4 would enable extension to somewhere around 10,000 to 20,000, limited principally by the optics.

A range of other degrees of anamorphism are also possible, all the way from nonanamorphic to the extreme of optics which spread the picture elements vertically across all the detector elements and requires no buffer. The required electronics obviously decreases in complexity with decreasing number of detector rows, decreasing total number of picture elements per line, and increasing degree of anamorphism. The complexity of the optics increases with degree of anamorphism, generally resulting in lower working light levels because of system cost and complexity tradeoffs. The exact limit to which this anamorphism can be pushed without significant sacrifice of light depends upon the particular system magnification and cost constraints and is a detailed optical design problem.

Light Level Considerations

The signal level obtainable in a staggered aperture system is obviously dependent on light level, and should only be compared to a linear array system with the same resolution. If the linear array is to be implemented with a detector size equal to the aperture size in the staggered aperture system, then the light level for the two cases will be the same, since the detection areas are identical. The difference will be that due to the larger cell size, the staggered aperture system will exhibit a larger dark current and a larger charge handling capability. If the staggered aperture system is to be compared to a linear imager with the same detector size, then the staggered
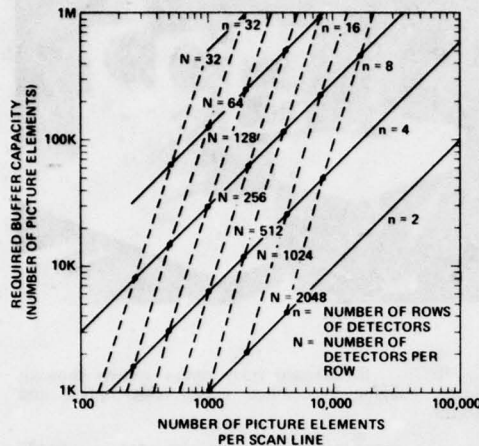
Fig. 5a.   Required buffer capacity in picture elements for a nonanamorphic staggered aperture scanner.
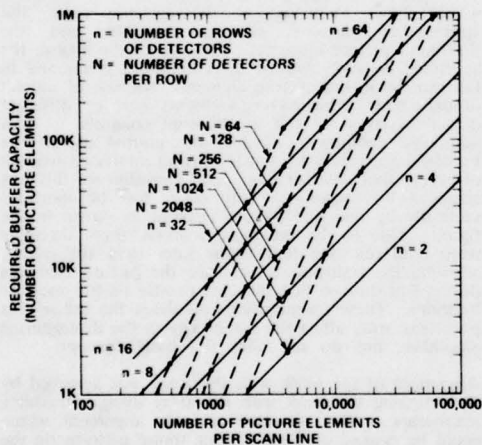
Fig. 5b.   Required buffer capacity in picture elements for an anamorphic staggered aperture scanner with an anamorphic ratio of n, where n is the number of rows of detectors.

aperture system will have less light by the ratio of aperture area to detector area. However, the linear array will also be n times longer, where n is the number of rows of detectors. In addition, since the optics become easier to build for the higher demagnification required in the staggered aperture system, it may be possible to work with lower f/# optics for the smaller pixel size, recovering some of the lost light. This is a qualitative judgment however, which can only be determined through a detailed lens design for a given system application.

Sampling Aperture

One interesting feature of the staggered aperture system is the ability to almost arbitrarily chose the sampling aperture size and shape. For a conventional linear imager, square or rectangular picture elements are used which basically abut each other at the detector edges. This provides for sampling at the Nyquist limit with moderate control of image aliasing. For a staggered aperture system, other aperture shapes which over sample could be used to give much finer control of aliasing. As an example, Figure 6 shows three possible pixel sizes and shapes and the resulting system MTF. Also shown are the well known foldback aliasing terms produced by convolution of the system response with the transform of the periodic sampling function.[2] The top curve in the figure shows a conventional set of abutting pixels with the foldback aliasing image terms going through zero at the low spatial frequencies. The middle figure shows a double width pixel having a 2-1 overlap. The foldback aliasing terms are obviously much less, but so is the MTF. The bottom curve shows an overlapped diamond which is a compromise MTF between the other two but has a dramatically reduced aliasing fold back term near the origin. This type of aperture controls aliasing extremely well along the horizontal and vertical picture axes.

Filtering Considerations

One significant aspect of a staggered aperture scanning system is that neighboring detectors sample light from every nth picture element. Because of this, destaggering must be performed before any filtering operations can be applied to the readout signal. In addition, this places a higher required value on the charge transfer efficiency of the readout register than would be required for a linear scanner.

III.   Experimental Breadboard

A simple laboratory experiment was set up to demonstrate the basic staggered aperture concept. A commercially available Fairchild array having 190 by 244 elements was used in a relay optics configuration similar to Figure 4. The top 15 rows of detectors in the CCD were used, resulting in a total system resolution of the 15 x 190 = 2850 elements. The magnification of the system was such that these resolution elements were spread across a 6.8 inch format resulting in an image

resolution of 420 bits per inch. The input was a black and white test pattern placed on a translating stage and illuminated with light from two florescent lamps. Light
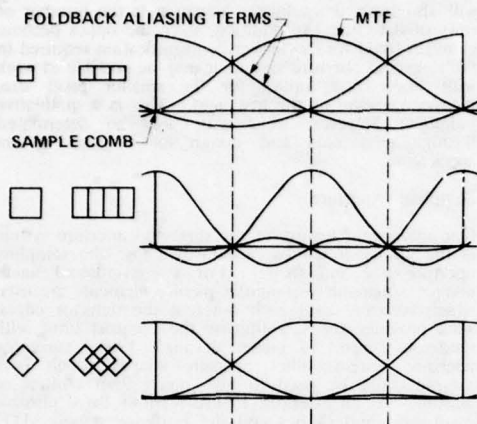
Fig. 6   System MTF and foldback aliasing response on the x-axis for three different aperture sizes and shapes.

from the illuminated region was reflected off a 45 degree mirror, traveled down an optical bench, and was imaged onto a metalized mask at 13.5 reduction. This mask was then relay imaged onto a commercially available area imager at 1: 2.25 demagnification. Figure 7a shows the basic system front end, with the metalized mask, imager, and relay optics shown in Figure 7b.
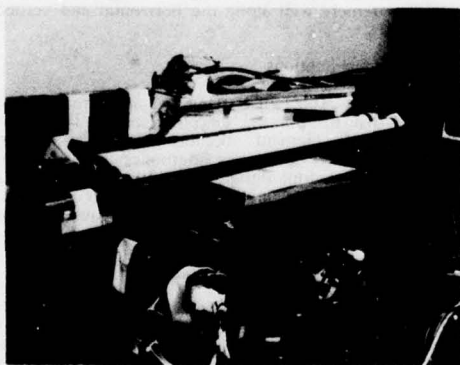
Fig. 7a.   Breadboard illumination system showing transport, fluorescent lamps, 45 degree fold mirror, and test pattern.
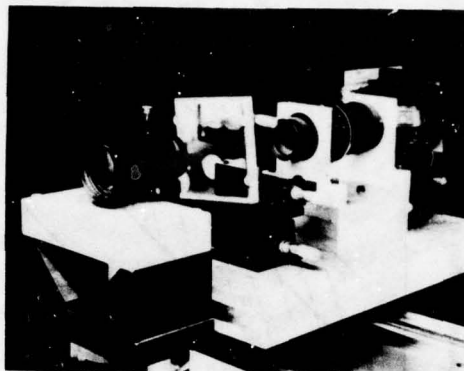
Fig. 7b.   Breadboard relay optics system showing primary imaging lens, tilted mask, relay optics, and detector

Since the geometry of the array was not specifically designed for this type of application, it has detectors arranged on a rectangular format such as Figure 2b, rather than the optimum format shown in Figure 2c. To account for this, and still allow the light from each aperture in the mask to fall in the approximate center of its appropriate detector, the mask and array were tilted with respect to the direction of document transport by 6.3 degrees. The effect this has is shown in Figure 8 which shows a picture of the aperture mask, the approximate detector sensing elements, and the document picture elements. As seen in the figure, the apertures on each row of detectors were positioned to fall exactly on one picture element. Because of the tilt of the array, these picture elements were on different document rows as well as different columns. An additional complexity involves the normal use of the Fairchild array as a TV sensor, having interlaced readout of every other detector row. Compensation for this was achieved by displacing every other row of apertures vertically by one half picture element as shown in the figure. Due to the interlaced readout, these detectors were read out one half frame later than the others, allowing the transport to displace the picture elements during this time so that they fell exactly on the aperture locations. These complications involving the use of this particular array affect the complexity of the destaggering algorithm, but do not alter the basic concept.

Alignment of the mask with the array was achieved by first aligning the mask with the array using a traveling microscope. This provided a crude alignment which could be peaked up by observing moire patterns on the detector array output which were caused by interaction between mask aperture structure and the detector element structrue. With uniform illumination at the mask this moire show up as a cyclical variation of the detector output, a sample of which is shown in figure 9a.
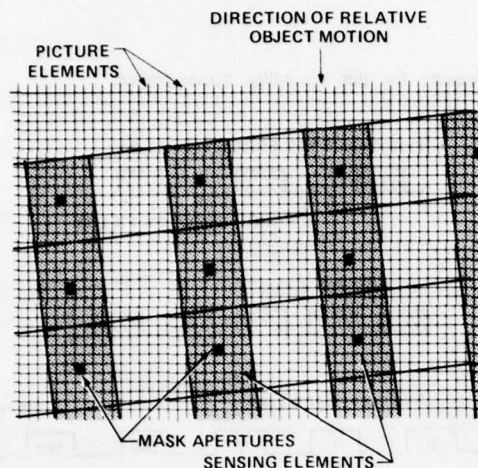
Fig. 8   Diagram of tilted mask configuration used in breadboard showing overlapping picture elements, mask apertures, and detector elements.

This cyclical variation showed maximum contrast when the mask was in focus on the array. This contrast was thus used for mean focus setting and for mask tilt (in focus) adjustments. Optimum magnification was determined by measuring the cycle length of this moire pattern as the magnification was changed and setting it to give an infinite cycle length (i.e. when one moire cycle covered the entire length of the array). Final lateral translational adjustment of the mask was achieved by peaking up the entire output signal. Vertical translational adjustment was achieved by making sure that the top row of apertures in the mask fell on the first row of detectors read out. Final alignment was achieved by illuminating one aperture at a time and checking for isolated detector output as shown in Figure 9b.

The Fairchild CCD211 array used for this experiment is organized as an interline transfer system with 190 interline transfer registers of 122 elements.[3] It is operated in the normal TV mode with two interlaced fields. For readout, charge packets from alternate sets of sensing elements are transferred horizontally to vertical interline registers, as shown in Figure 10. Each interline register accesses 244 sensing elements in two fields of 122. There are 190 interline registers for the 190 columns of the array.

The interline shift registers are clocked in parallel so that for each vertical clock cycle, one charge packet from each interline register is presented to the output or horizontal register. It can be seen that for each field the entire contents of the vertical interline registers must be

shifted into the output register before the next field is accessed to avoid superimposing charge-packets from one field onto charge-packets from the next field. In our experiment 10 rows from each field are read out. (The 15 rows of data actually used are selected from these 20 read out rows by the line counter electronics.)
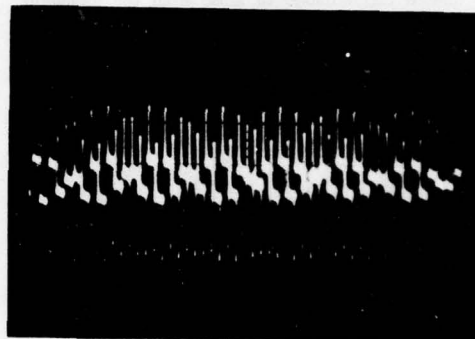
Fig. 9a   Typical array output used to adjust array alignment showing moire fringes due to improper magnification.
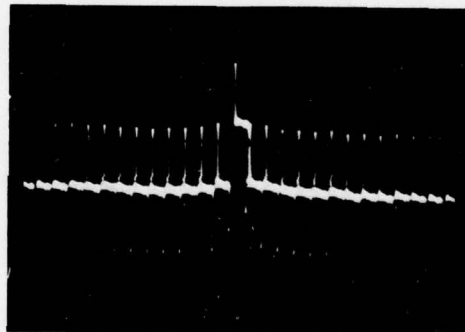
Fig. 9b   Array output with single aperture illuminated.

The timing sequence used to operate the array is shown in Figure 11. The horizontal output register contains 200 elements and receives the charge-packets from the interline transfer registers at each vertical shift. Charge packets are shifted out of the horizontal register at 5 MHz. A total of 256 shift times are used for each line: 200 to empty the horizontal register and 56 to wait while the next line is shifted in from the interline transfer registers, resulting in a total line time of 51 μsec. For this experiment, 10 of the 122 rows of sensing elements in each field are read out. It is thus necessary to purge the unused accumulation of noise from the remaining

registers, resulting in a total line time of 51 μsec. For this experiment, 10 of the 122 rows of sensing elements in each field are read out. It is thus necessary to purge the unused accumulation of noise from the remaining
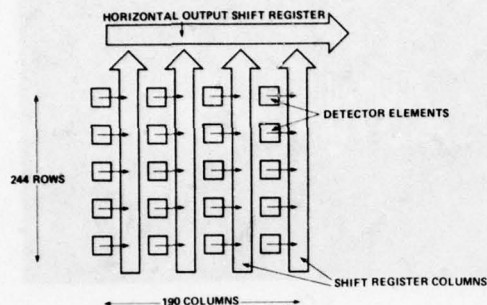
Fig. 10. Interline transfer array organization

rows of the vertical registers before a new field can be accessed. This is accomplished by increasing the shift rate of the interline transfer registers from 51.2 μsec per row to 6.4 μsec per row. This vertical shift rate of 160 KHz will empty the interline transfer registers in 717 microseconds. The total time to receive the entire frame of 20 lines is then 2.5 milliseconds. During the time that unused charge packets are being purged from the array, the horizontal output shift rate is maintained at 5 MHz even though the vertical shift rate has been increased by a factor of 8. This results in the charge-packets being superimposed on previous charge-packets at an 8 to 1 rate. Since the unused data consist only of dark current and background illumination, saturation of the output register is not reached with the 8 to 1 multiplication of the charge.

The output signal from the array is threshold detected and converted into a TTL logic signal indicating either black or white information. A sample and hold circuit has also been provided so that more accurate measurements of signal amplitude can be made.

In order to implement destaggering for this breadboard system, including the complexities of multiple lines, multiple columns, and frame interlace, an off line concept was chosen for destaggering as shown in Figure 12. The data was read from the CCD array, single level thresholded for 1 bit detection, and read in real time into a 1.5 Mbit FIFO at a data rate of 5 MHz. This data was later taken from the FIFO, destaggered with a Fortran program in a NOVA 800 mini computer, and displayed on a CRT. Although this procedure is much too time consuming for most practical systems, it was

adequate for this feasibility demonstration.
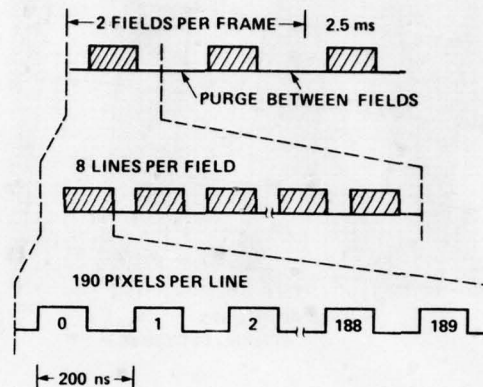
Fig. 11. Data format for staggered aperture breadboard
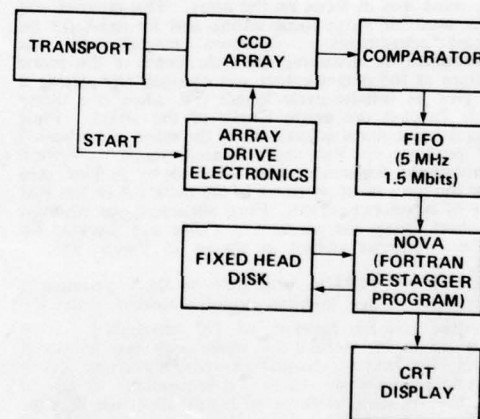
Fig. 12 Breadboard electronic system used for destaggering.

Figure 13a shows an example of data read in from a text test pattern, with output data printed on a laser printer to show the full 2850 element capability. The data file was limited in size by the FIFO to a tilted region commensurate with the tilted array. The data at the top and bottom shows incomplete data lines where the

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Fig. 13a   Sample output of full resolution scanner showing 2850 bit resolution. Top and bottom rows of data are incomplete because data rows were imaged in middle (vertically) of detector rows when data taking started or stopped. Spacing of vertical black lines indicates spacing of detectors on array.

Fig. 13b.   Magnified view of data in Figure 13a.

Fig. 13c.   Output for input halftone pattern. Comb function at edge of picture is incomplete data. Spacing of comb function shows spacing of detectors in detector array. (Background is black for this picture because the test pattern was negative and the data has been inverted.)
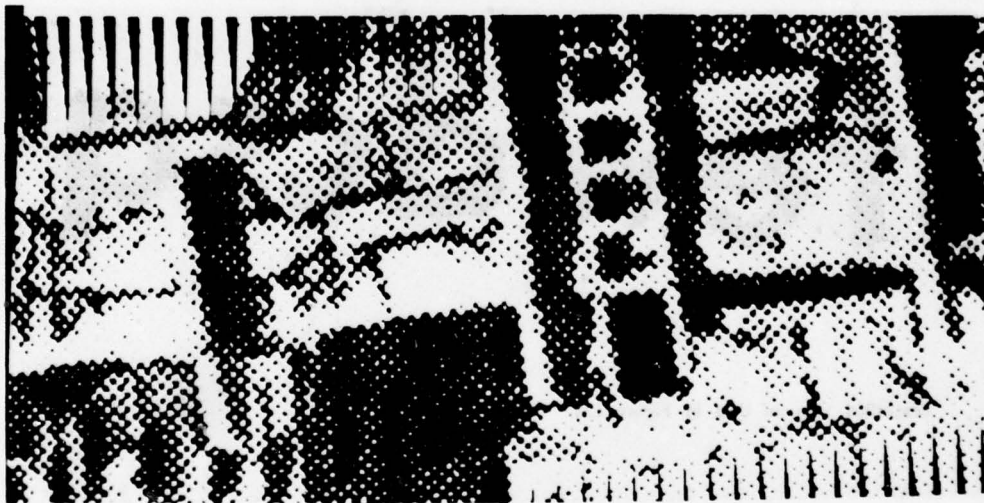
Fig. 13d.   Expanded view of data in Figure 13c.

document line was imaged inside the region of the area imager when data taking commenced or when it finished. As expected, the incomplete data shows up as a triangular comb function, since data points nearer the center were sampled by more detector rows than those at the edge. Figure 13b shows an enlargement of some of the textural detail, showing no significant noticeable affect of the destaggering procedure. Some black dots are seen in the background region which were caused by noise in the electronics which were not fully optimized. Figure 13c and d show similar results for an input halftone picture with a screen frequency of 85 cells per inch. In this case, the test pattern was a negative and the picture has been inverted to clearly show the comb function at the edge of the field. The spacing of the teeth in the comb indicates the spacing of the actual detectors in the array.

Conclusion

A technique has been demonstrated for achieving high resolution line scanning of a two dimensional image by using an area detector array. This technique uses a metalized aperture mask on the optical input and a computer buffer memory on the array output to achieve higher resolution performance than possible from a single linear array. A sample breadboard system was built to demonstrate the high resolution data can be taken in this way and reconstructed without artifacts.

Acknowledgments

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A HIGH RESOLUTION BUTTABLE TIME DELAY
AND INTEGRATE IMAGING CCD

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ABSTRACT. The design and fabrication of a CCD buttable 256 x 96 element TDI chip was undertaken by BNR and ITEK; as a vehicle to prove the development of a 2048 x 96 element buttable TDI. In both of these designs the time delay operation is in the 96 elements Y direction. The TDI imager was fabricated using BNR's two-level polysilicon buried channel CCD process. High resolution of 13 μm in the X and Y direction was achieved through the use of ripple clocking and a novel interlaced readout scheme. The TDI is also buttable with only 2 sensor elements gap between adjacent devices. The device offers some blooming control capability by electronic selection of 1, 8, or 96 rows of element. Device characterization results will be presented together with sample imagery taken with the imaging chip.

1.0 INTRODUCTION

Developments in reconnaissance area imaging systems over the last few years have emphasized the use of solid state imaging arrays. CCDs are natural candidates for this role. Various analysis have scoped the requirements for such CCD arrays (2,3).

Itek Corp., Lexington, Mass., U.S.A., and Bell-Northern Research Ltd., Ottawa, Ontario, Canada have been working since 1976 on the development of a family of CCD imaging devices intended for application in military reconnaissance systems (1). The purpose of this paper is to describe the design, operation and performance of the first TDI of this family. The TDI, designated Itek/BNR 719A, was designed to be buttable with less than two pixel spacings between chips. The resolution in both X and Y direction was 13 μm. The high resolution was achieved by using some novel design approaches. Test results reflect the high performance of these devices in the area of noise and dynamic range which are needed for military applications. This paper will describe the architecture and fabrication of the chip, and present test results including imagery of simulated

moving scenery. Finally, we will briefly discuss the application of the chip to military reconnaissance systems.

2.0 DEVICE ARCHITECTURE AND FABRICATION

A block diagram of the buttable 719A TDI is shown in Fig. 1. The imaging area, parallel to serial interface, and serial shift register are the main functional blocks of the TDI. There are 3 basic operations in a TDI imager:

(i) The electronic imager formed on the TDI imaging areas is clocked from one row of sensors to adjacent row of sensors in synchronism with the optical image motion.

(ii) When a line of the electron image reaches the bottom row of sensors of the TDI, it is transferred into the serial shift register via the parallel to serial interface.

(iii) The data transferred into the serial shift register is read out serially by the output circuit located at the end of the shift register.

The option middle output tap is a destructive output which doubles both the TDI line rate and output data rate without increasing the serial shift register

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clock frequency. When not required, it can be disabled by a transfer gate and all charge packets are transferred to the end output circuit. Electrical inputs are provided for the TDI array and serial shift register for convenience of testing and characterization.

The high resolution of the 719A in both X and Y directions is the result of the following two novel design approaches.

(i)   Odd-even channel interlaced transfer into the serial shift register.
(ii)   A 8-phase ripple clock scheme for the TDI array.

A detailed description of these two techniques will follow:

(i)   In the X direction, the resolution of a conventional TDI is limited by the stage length ΔX of the serial shift register (see Figure 2). A novel way out of this limitation is to perform the charge transfer operation from the TDI to the serial shift register in two stages. This odd-even channel interlaced readout scheme runs as follows. In the first stage of the readout, charge from the odd channels is transferred to the serial shift register, and charge from the even channels is stored in a buffer register. Then data in the shift register is read out serially. In the second stage of the readout operation, charge from the even channel is transferred and clocked out. This is formally equivalent to multiplexing the serial shift register. Figure 3 shows that the CCD channels within the TDI array can be spaced to half the stage length of the CCD shift register, or $\Delta X/2$ (13 μm). Thus, at the expense of a slightly more complicated readout scheme, the resolution in the X direction is doubled.

(ii)   In the Y direction, the normal 2 phase (or 3 phase or 4 phase) CCD structure is replaced with an 8-phase ripple clocking structure. The advantage of an n-phase ripple clocking system is that charge can be stored in n-1 consecutive pairs of CCD electrodes. Only 1-phase need to be reserved for charge transfer purposes. Figure 4 shows the

clocking waveform for an eight phase ripple clock scheme. The resolution of a ripple clock TDI is not limited by the stage length $2\Delta Y$ (2 pairs of electrodes) of the CCD. Instead, it is exactly the same as the length of one pair of CCD electrodes, or ΔY. Actually, there is a certain amount of charge sharing involved during the charge transfer operation, which causes MTF degradation. The Y axis MTF degradation in a ripple clock TDI is given by:

$$(MTF)Y = \frac{\mathrm{Sin}\, \dfrac{n}{n-1}\, \P f\Delta Y}{\dfrac{n}{n-1}\, \P f\Delta Y}$$

where ΔY = stage length of CCD (2 pairs of electrodes)

  f = spatial frequency in cycles/mm

  n = # of ripple clocking phases

It can be seen that in order for the ripple clock to be effective (i.e., without suffering crippling MTF loss), it has to be significantly larger than 2.

The total MTF loss due to finite aperture size, discrete charge motion and charge sharing is then:

$$(MTF)Y = \underbrace{\frac{\mathrm{Sin}(\P \Delta y f)}{(\P \Delta y f)}}_{\text{aperature MTF}}\underbrace{\frac{\mathrm{Sin}\, \dfrac{n}{n-1}\, \Delta f \P y}{\dfrac{n}{n-1}\, \P f\Delta y}}_{\text{Ripple Clocking MTF}}$$

In a buttable TDI, the ripple clocking of the 96 pairs of electrodes poses some formidable problems. There are 3 basic system constraints:

(a)   Since it was decided to adopt 8 phase ripple clocking, the 96 electrodes have to be connected in 12 blocks of 8 pairs of electrodes each.
(b)   The buttability requirement precludes running the clock lines alongside the circuit and connected to the different set of electrodes in a matrix fashion.
(c)   It was decided to make provisions allowing the selection of all 96 rows of sensors, the first eight rows of sensors or the first row of sensors only.

These 3 requirements are met by partition-
ing the imaging part of the B^2TDI into
8 segments (see Fig. 3) in the X direction.
The use of two level metallization allows
the implementation of these features.

The dimensional requirement for buttability
was that the separation between two dies
would be only 2 equivalent pixels as
shown in Fig. 4. The edges were prepared
by a chemical etching technique developed
at BNR. Fig. 14 shows a picture of the
prepared edges of the buttable 719A TDI.

In operation the photo-generated charge
in the pixels is moved in the Y direction
of the TDI by an 8-phase ripple clock
scheme (Fig. 5) which is in synchronizism
with the imagery scene motion. Once the
charge reaches the bottom of the TDI,
it is transferred in the serial shift
register via the parallel to serial
interface.

The clock timing for both interface scheme
and shift register is shown in Fig. 6.

The output sensing circuitry of the serial
shift register is shown in Fig. 8. It
consists of a presettable floating diffus-
ion connected to an on chip pre-amplifier
(depletion type MOST source follower).
The photocharge is sensed as a voltage
change at the output of the source follow-
er.

The imagers were fabricated using BNR's two
levels polysilicon gate buried channel
technology. The process allows the on-
chip incorporation of enhancement and
depletion (ion implanted) MOST structurers.
This attractive feature contributed to
the low noise performance of the output
pre-amplifier. The process uses three
ion implants steps plus n+ diffusion for
source and drain. It also features iso-
planar oxide isolation and two levels of
aluminum interconnects.

3.0 TEST PROCEDURE AND EXPERIMENTAL RESULTS

3.1 General Information

The devices were evaluated on two
levels; normal device characterization
tests such as transfer efficiency,
spectral response, pre-amplifier
gain and noise measurements performed
at BNR, and extensive testing at Itek

to characterize the device as an image
transducer in a situation comparable
to a high quality reconnaissance system
application.

3.2 Examination and Imaging Testing of the Itek/BNR 719 CCD Chip

High quality airborne military elect-
ronic reconnaissance camera systems
are rather complicated, with the data
stream from the CCD or other solid
state array typically undergoing
sophisticated signal processing in the
aircraft, digital transmission or
recording, and digital data processing
on the ground before display. In order
to fairly characterize a CCD array for
this application, we must duplicate
most of these functions with test gear
such that the final displayed output
is limited in its quality by the device
under test, rather than be the test
equipment. In the case of imaging
CCD's, this is a difficult problem due
to the low noise and high dynamic
range of the Itek/BNR 719 chips.

Figure 9 is a block diagram of the
Electro-Optical Imaging Laboratory
used at Itek for the characterization
testing of the Itek/BNR 719 CCD. It
shows the image producing process from
the input scene to the final output,
which may be a hard-copy print of the
image seen by the CCD or a computer
printout representing the analysis of
some properties of the image. At the
left side, we show the various input
possibilities for a CCD under test. We
may choose among real scenes, model
scenes, photographic reproductions of
real scenes, or standard test charts.
Most of the routine characterization
testing that we perform is done using
moving belts of film with reproductions
of aerial photography and test charts.
This test input is imaged on the TDI
chip by a lens whose imaging perfor-
mance is known. The image transducer
in our situation is a CCD under test
with its operating electronics. In
order to simulate high quality data
recording, we use a Data General
Eclipse S-230 mini-computer with a
customized set of peripheral equipment.
The pixel stream from the CCD is dig-
itized by a high quality A/D converter
capable of 10^7 conversions per second
with 13 bit resolution and fed into a

semiconductor memory which can store up to 10^7 bits. This is sufficient to reproduce frames of imagery large enough for display and characterization. The S-230 can then retrieve the data from the semiconductor memory, perform manipulations of the data, and write it onto tape for more detailed analysis in the Itek IBM 370-158 computer, which is a general purpose off-line machine. That computer can perform data manipulations of several types. It can perform image enhancement (such as calibrating out the element-to-element variations that exist in virtually all arrays) for the purpose of presenting hard-copy image display. It can perform a number of statistical analysis of the imagery such as signal-to-noise ratio calculations. It can also alter the recorded data to simulate the effect of other system components so that complete systems may be simulated for system design purposes. Finally, we have available as output peripherals, a choice among a laser writer (for hard-copy imagery), a line printer for tabular data, a plotter for graphical data, or a tape deck for tapes to be stored or transmitted to other organizations.

3.3 Test Results

The best demonstration of an imaging CCD is imagery produced by it. Fig. 10 shows two examples of imagery from the Itek/BNR 719 chip, recorded in the Itek EO Imaging Laboratory just discussed and printed out on the Laser Scanner. The images are of the USAF 1951 Resolving Power Test Target and the Itek 1975 MTF Test Target. The test conditions for these images are as follows:

Line rate	4 KHz
Pixel rate	1 MHz
Readout	End Tap
Exposure	50,000 e^-/pixel
	4,800 K Blackbody
Temperature	35ºC

The imagery was reconstructed by properly interlacing the pixels with a software operation in the data gathering process.

For the MTF Test Target, the optical magnification was 0.1, so 40 lp/mm,

the nominal Nyquist limit, is the 0 element of the 2 group. In a), the right portion of the printout is a 2X blowup of the last five groups in the left portion. In both cases, the Nyquist limit is resolved, and the uniformity and high quality of the imagery may be seen.

A summary of the measured properties of a typical sample is given in Table I. It is shown that an excellent imaging performance with high sensitivity and low noise was obtained. The dynamic range at 4 KHz line rate and 1 MHz pixel rate is 5,000, with the saturation level being limited by the small pixel size to about 125,000 e^-/pixel as an image sensor.

The MTF data are shown in details in Figure 11. Three curves shown in order to indicate the separate effects of CCD design and the charge diffusion in operation. Curve one is the calculated geometric MTF of the finite cell area and the motion error caused by continuous scene motion and discrete charge motion. For the eight phase ripple clock scheme used, that MTF component (for "short pulse clocking; that is, the phase clock pulses are shorter than the phase duration") is

$$MTF = \frac{Sin(\pi f \Delta y)}{\pi f \Delta y} \quad \frac{Sin \frac{n}{n-1} \pi f \Delta y}{\frac{n}{n-1} \pi f \Delta y}$$

where n = 8 for the Itek/BNR 719 chip.

Curve 2 is a measured MTF with an incandescent source filter to remove light beyond 0.75 μm. Curve three is a measured MTF taken with light having approximately a 4800K blackbody spectrum. The previously discussed (4) effect of deep absorption of red and near infrared light and subsequent diffusion of charge to nearby pixels is evident. The effect was accentuated here, because the chip measured response peak at about 0.9 μm. This effect is a significant limiting factor to the performance of small CCDs in cases where both sensitivity and resolution are desired (3).

Signal and noise transfer are shown in Figure 12, as a function of exposure.

At a pixel rate of 5×10^6 per second, the dynamic range is from 0.4×10^{-6} j/m^2 to 0.9×10^{-3} j/m^2. Since the noise is predominantly flat, the extrapolated noise level with 10^6 pixels per second and a 2 MHz filter is 0.18×10^{-6} j/m^2.

Spectral response of this chip is shown in Figure 13. It shows the expected general form, with light at wavelengths less than about 0.5 µm absorbed in the overlying layers of polysilicon and also due to light at wavelengths longer than about 1.1 µm passing through the active region without being absorbed. The peak at 0.9 µm is a combination of high quantum continuation (photons per joule) at longer wavelengths and an optical feature. The peak quantum efficiency is 55%. The measurements were made with a monochrometer having $\Delta\lambda = 0.05$ µm, and power measurement was made by substituting a radiometer in the CCD image plane.

3.4 Testing of Buttable (Edge Etched) CCD

In this section the operation of the Itek/BNR 719 chip is demonstrated. Figure 14 is a set of photomicrographs of the etched edges of a chip. By measurement, it may be seen that the two chips may be placed such that the center to center spacing of the two extreme TDI columns would be 37 µm. Since the goal was to have two chips buttable with two missing columns of data, the goal is satisfied if the extreme columns can be placed with a center-center spacing. Other work (4) has demonstrated the ability to place the CCD chips on a common substrate and register them to within about 5 µm of specified locations.

Figure 15 is a reproduced image of the USAF 1951 Resolving Power Test Target taken with the same chip appearing in Figure 14. In this picture, the display shows the pixels in the order they are read out of the chip, with the left half of the picture containing the even numbered pixels and the right half the odd numbered pixels. Since the optical magnification was 0.1, the Nyquist limit in the direction occurs at the 0 element of group 2.

Because of the pixel interlace the Nyquist limit in the orthogonal direction is the 0 element of the 1 group.

As may be seen by examining the photo, the edge etching process has not introduced any artifacts into the imagery. The edge columns do not exhibit dark current or sensitivity noticeably different from the neighboring elements. The goal of a gap of two pixels was set based of a simulation using samples imagery. The imagery was processed to simulate a typical system MTF at the Nyquist limit. Gaps in the sensing array were then simulated by eliminating columns of video and replacing the pixel values with linear interpolations of the video on the closest remaining pixels. Gaps of from 1 to 10 pixels were simulated in this manner. A typical picture containing fairly busy imagery on which this procedure has been carried out is shown in Figure 16. Most observers can find the 10 pixel gap and the 5 pixel gap, but cannot find the 1 or two pixel gaps until they have found the wider ones for reference. (The gaps extend the vertical length of the pictures and all begin with the same horizontal pixel).

3.5 Demonstration of Operation of Intermediate Tap

One of the design features which is critical for successful operation at very high line rates is the tap at the 128th element. Operation of this tap is shown in Figure 17. There, a) shows the entire pixels read through the end tap with the center tap bypassed. In b) the output from the end tap is shown on the transfer gate adjusted at an intermediate value to demonstrate the partial extraction of signal charge by the middle tap. In c) and d), the outputs from the two taps are shown separately, having been recorded under identical conditions. There is no visible leak-through of data from the left half of the chip when the center tap operating voltages are set correctly.

The operating speed for these pictures was 20,000 lines per second. Operation up to 40,000 lines per second has been demonstrated.

The significance of successful tap operation becomes evident when considering the design of chips with 2,000 TDI columns to operate at 50,000 or more lines per second. This would require an output tap to operate at 100,000,000 pixels per second, unless intermediate taps are used. Such high operating rates, present problems in chip design, data handling design, and high output preamplifier noise due to the high bandwidth.

4.0 SUMMARY

To summarize, a prototype buttable TDI imaging chip was developed characterized and tested in a system context by BNR and Itek. The chip is capable of high dynamic range and low noise operation. It is buttable with less than two pixels spacing between chips. A middle output tap is provided for increased line rate readout. The chip has been tested thoroughly with sophisticated optical data processing set up and is shown to be useful for aerial reconnaisance application. A further 2048 x 96 TDI chip having the same features is being fabricated.

ACKNOWLEDGEMENT

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(3) Bradley, W., "Small Geometry Charge Coupled Devices for Aerial Imagery", Vol. 137, Proceedings of SPIE, Washington, D.C., 1978.

(4) Goldfarb, S., and Coluin, D., "Precise Mounting of Semiconductor Chips for Electro-optical Arrays", Proceedings for ISHM78.

TABLE I: SUMMARY – PROPERTIES OF ITEK/BNR 719 CCD

Array Size	256 pixels x 96
Operation	TDI (96 element direction)
Spacing (ripple clocking)	13 μm x 12 μm
(2 Ø clocking)	26 μm x 24 μm
Buttable	2 pixel gap
Tap (use optional)	128th element
Sensitivity	0.15 a/w
MTF (40 lp/mm; TDI direction)	0.2
Saturation Level	
Signal	125,000 e⁻/pixel
Exposure (5500K Blackbody)	0.9×10^{-3} j/m²
Noise Level (dark) -5×10^5 pixels/sec	
Signal	70 e⁻/pixel rms
Equivalent Exposure	0.4×10^{-6} j/m²
Noise Level (dark) -1×10^6 pixels/sec	
Signal	30 e⁻/pixel rms
Equivalent Exposure	0.18×10^{-6} j/m²
Dark Current (20°C)	2 na/cm²
Uniformity	
Sensitivity	∼1% p-p
Dark Current	<1% of saturation
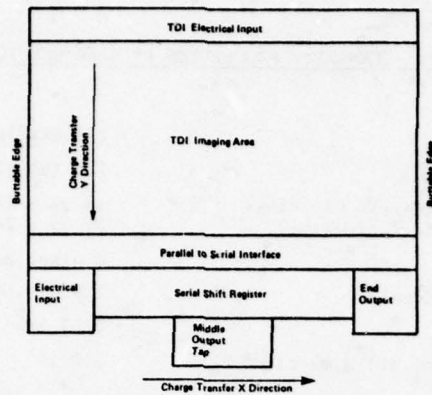
FIGURE 1   Block Diagram of 719A Buttable TDI
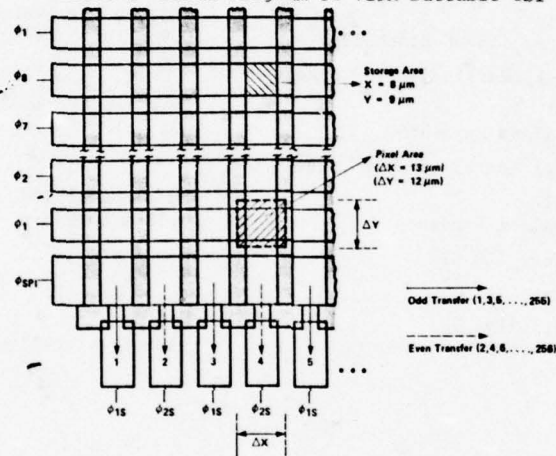
FIGURE 2   719A TDI High Resolution Cell Design
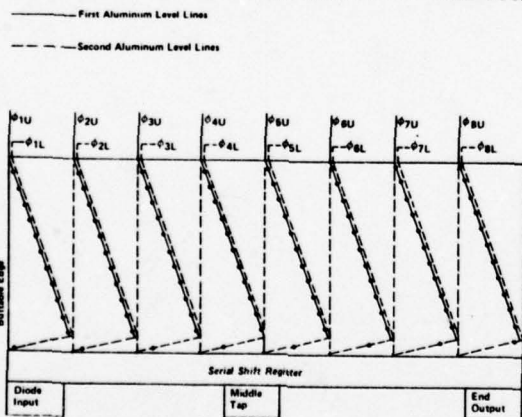
FIGURE 3   Electrode Contact Scheme on Buttable TDI

Scribe Channel Convention
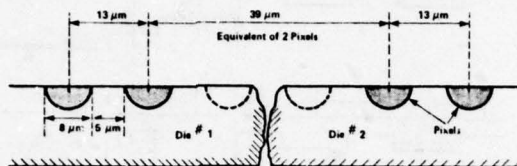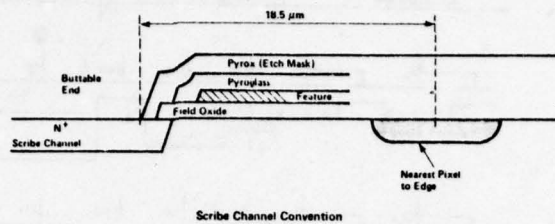
FIGURE 4 Butting Requirements of 719A TDI
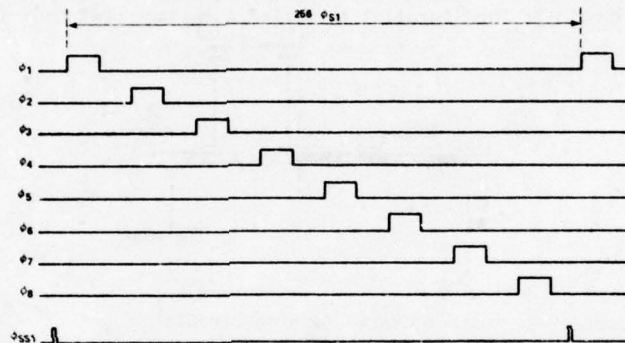
FIGURE 5 TDI 8-Phase Ripple Clocks
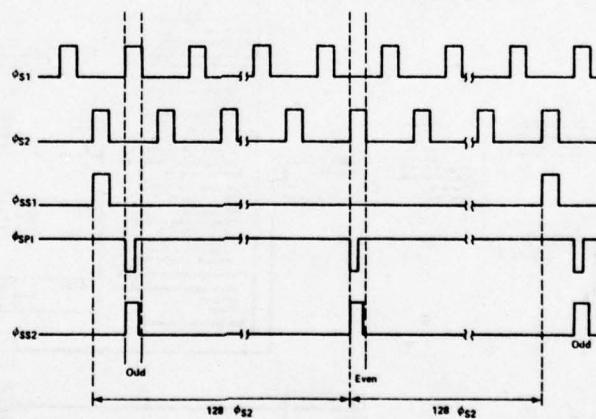
FIGURE 6 Serial Shift Register and Interface Electrodes Clocking
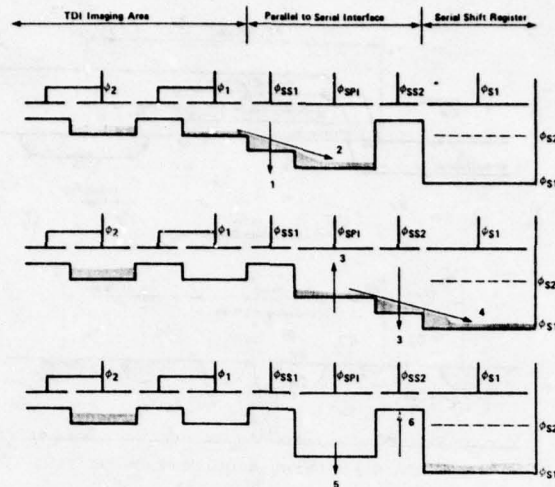
FIGURE 7   TDI Parallel to Serial Interface Operation (Odd Field)
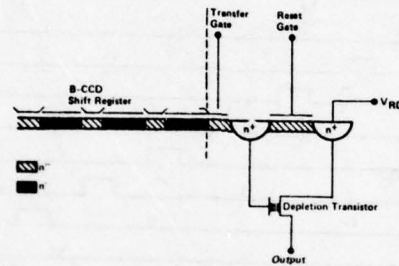
FIGURE 8   Output Charge Sensing Circuit
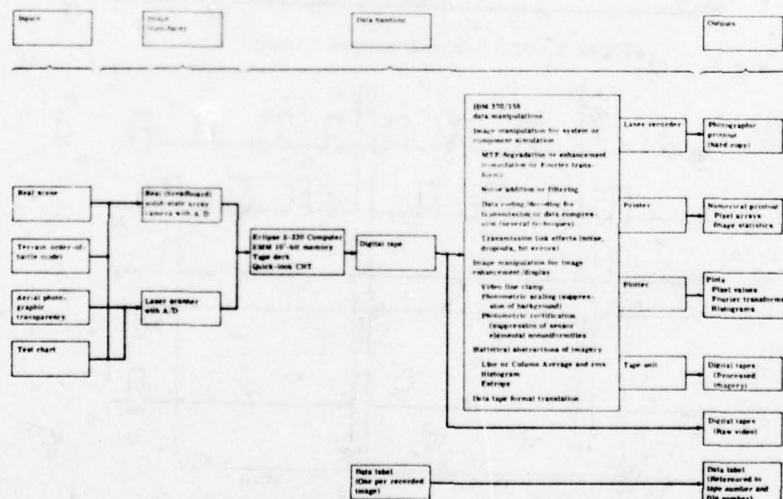
FIGURE 9   Production of Real or Simulated EO Imagery with Itek
Electro-Optical Imaging Laboratory (block diagram)

Frequency
(1μ/mm)

	10
2	14/18
3.4	22/26
6	30/34
10	38/42
14/18	
22/26	
30/34	
38/42	
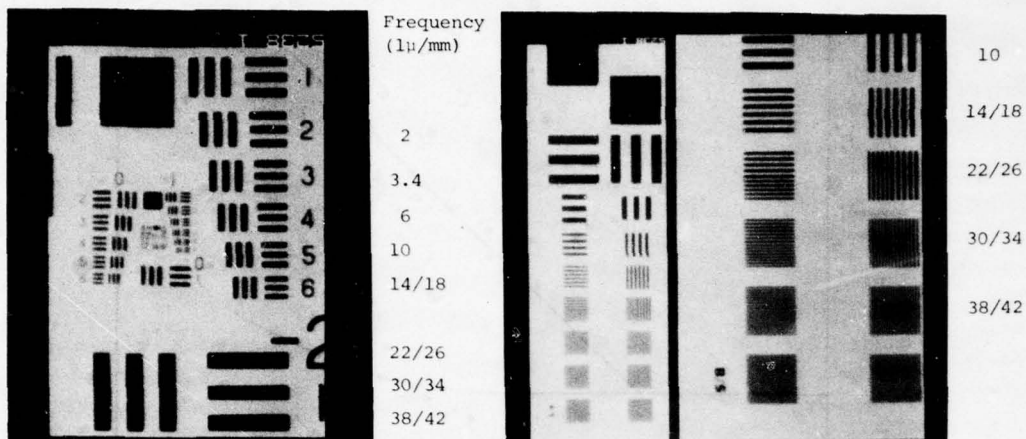
a) USAF 1951 Resolving Power Test Target   b) Itek 1975 MTF Test Target

FIGURE 10   Samples of Imagery from an Itek / BNR 719 CCD Chip
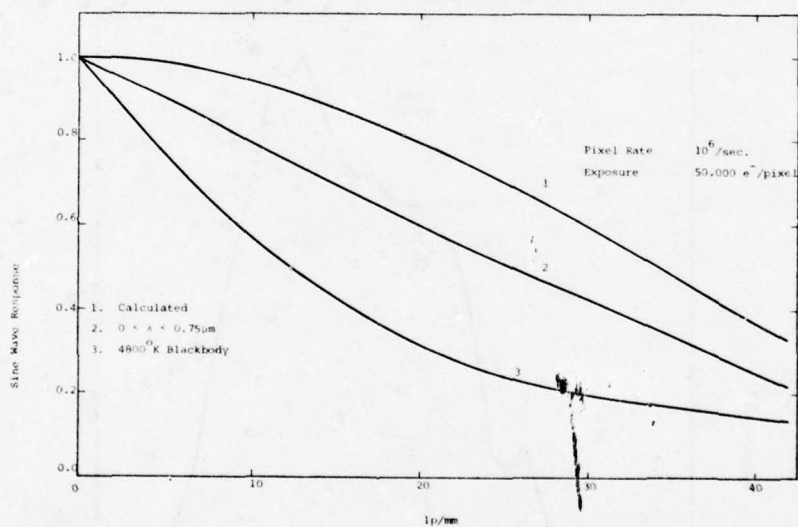
FIGURE 11   Modulation Transfer Function

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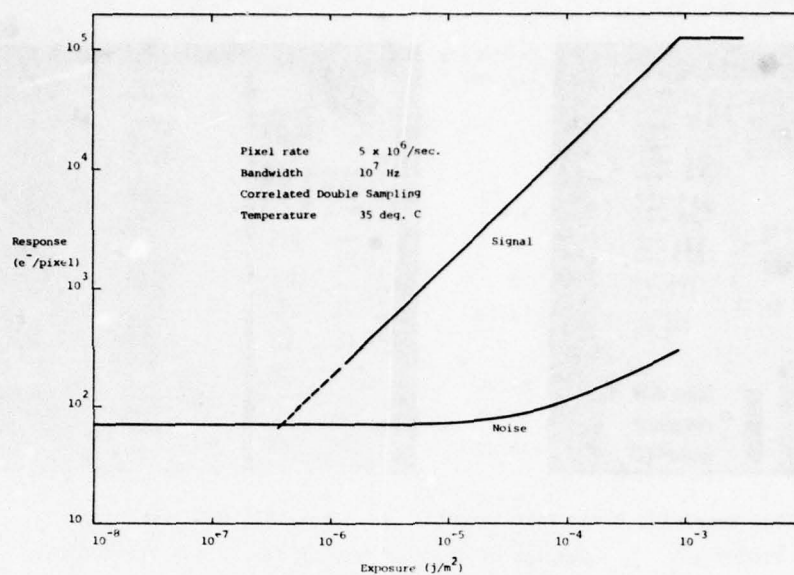
FIGURE 12   Signal and Noise vs. Exposure
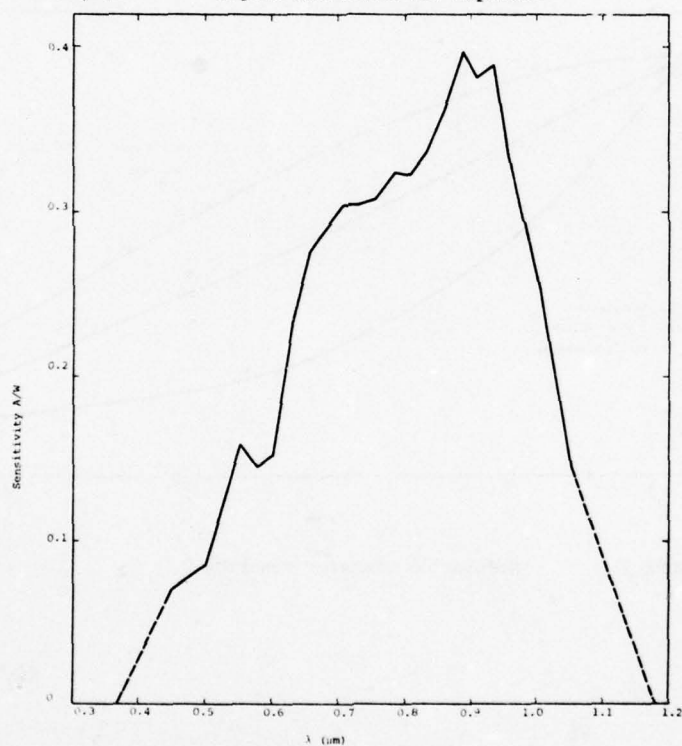
FIGURE 13   Spectral Response
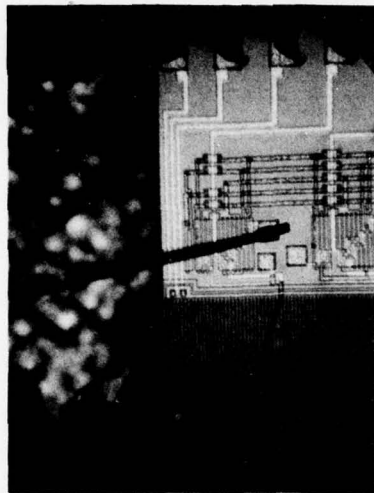
a) Top Left
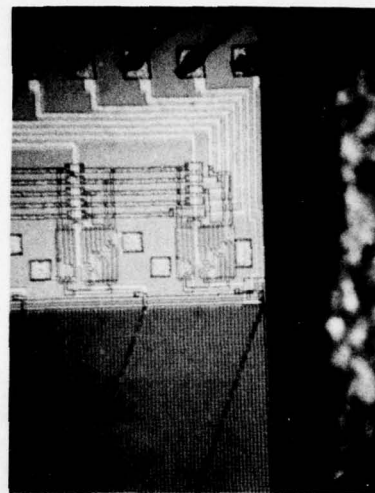
b) Top Right
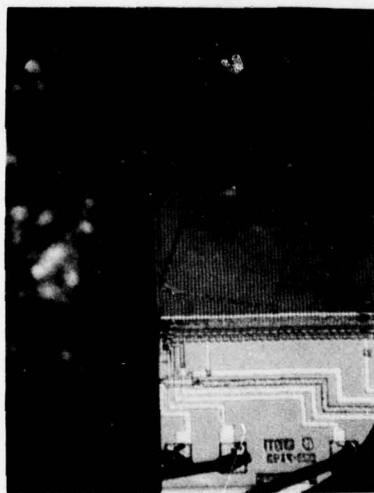
c) Bottom Left

d) Bottom Right

FIGURE 14   Photomicrographs of 719 CCD Buttable with 2 Pixel Gap
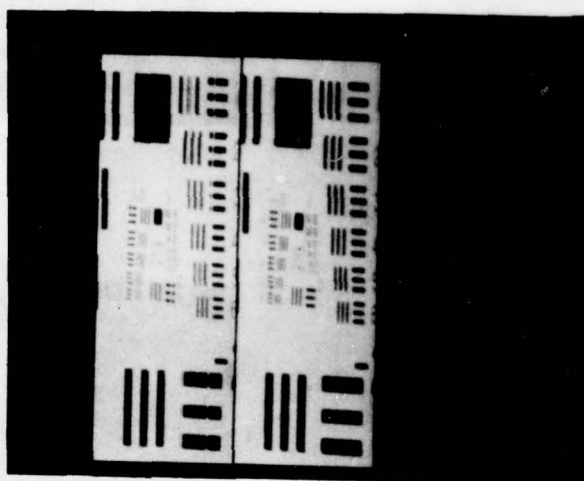
FIGURE 15   Imagery Recorded with Buttable
Edge Etched 719 CCD
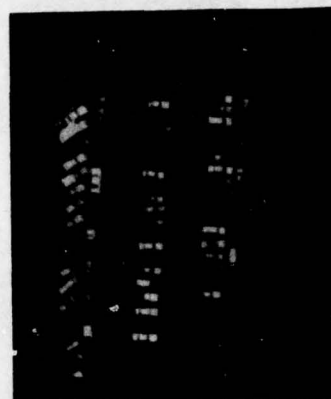
a) One Pixel Gap   b) Two Pixel Gap
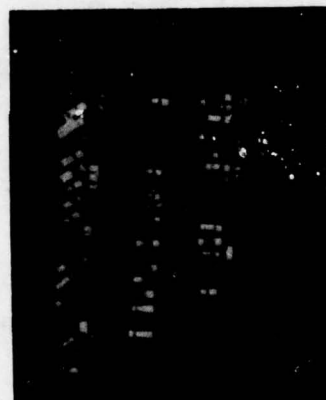
c) Five Pixel Gap   d) Ten Pixel Gap

FIGURE 16   Simulation of Effect on Imagery of Gaps
in CCD Focal Planes

a) Data from End Tap
   Center Tap Bypassed

b) Data from End Tap
   Center Tap Partially Activated
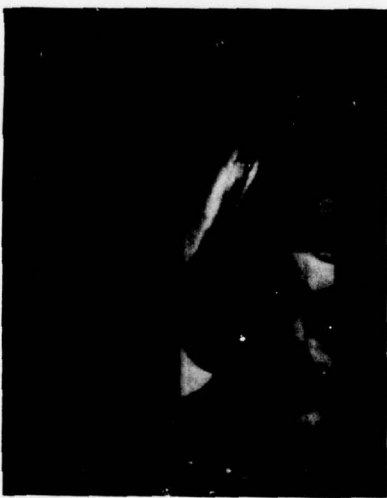
c) Data from Center Tap
   Center Tap Activated

d) Data from End Tap
   Center Tap Activated

FIGURE 17   Demonstration of Operation of Tap in Middle of
                              CCD Register

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CCD Imager Processing for Backside Illumination Applications*

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ABSTRACT

The backside illumination of CCD ima-
gers is finding application in the fields
of image intensification (for low light
level imaging and photon counting), for X-
ray imaging, and for optical imaging. Back-
side illumination requires special chip
processing not required otherwise. This
processing includes thinning to a 10 mic-
ron membrane thickness, boron accumulation
at the backside, specialized headers, and
specialized bonding techniques. Intensi-
fication adds the additional processing
associated with vacuum tube and photocathode
fabrication. This paper will discuss this
processing, presenting data on parameters
of interest for each of the above applica-
tions.

I.   Introduction

The backside illumination of CCD ima-
gers is finding application in the fields
of image intensification (for low light
level imaging[1] and photon counting[2,3]), for
X-ray imaging[4], and for optical imaging[5].
Backside illumination allows the incident
radiation to impinge directly onto the sili-
con. This avoids losses associated with
the frontside electrode structure. In ad-
dition, it allows the imaging of radiation
which otherwise would damage the frontside
CCD structure. Backside illumination re-
quires special chip processing not required
otherwise.

The fabrication of thinned CCD imagers
begins with slices of silicon and progress-
es through a standard set of processing
steps involving photolithography, oxida-
tion, diffusions, metallizations, and etch-
es. The fabrication of a slice of CCD im-

agers varies little in fundamental detail
from the fabrication of other MOS semi-
conductor devices. However, the remaining
processing steps required to produce the
final thinned device are nonstandard and
require development specifically for back-
side-illuminated arrays. These remaining
processing steps are: (1) thinning, (2)
accumulation, and (3) bonding to backside-
compatible header. Discussion of these pro-
cesses follows.

(1) Thinning. CCD imagers are back-
side illuminated to improve spectral re-
sponse and to allow electron-bombarded or
X-ray operation. These backside-illumina-
ted imagers must be thinned to provide ade-
quate resolution. Resolution is degraded
when charge carriers diffuse laterally while
diffusing toward the CCD storage wells. The
degradation is maximum for radiations ab-
sorbed near the silicon surface. Thinning
brings this surface near the CCD wells and
minimizes the extent of lateral diffusion.
This increases MTF and decreases crosstalk
between pixels. Thinning, however, lowers
the responsivity for wavelengths greater
than about 0.8μ.

(2) Accumulation. An unoxidized sili-
con surface is a region of rapid electron
recombination. Signal electrons that re-
combine at the back surface are not detect-
ed by the CCD. Since most signal electrons
generated by energetic radiation are crea-
ted near the back surface, this recombina-
tion must be inhibited to achieve adequate
response. This is accomplished by building
into the silicon substrate an electric field
that forces signal electrons away from the
back surface. The electric field is gene-
rated by enhancing the boron doping density
of the silicon at the surface compared to

the bulk doping density. Since boron atoms in silicon are negatively charged, this accumulation of boron introduces a fixed space charge that repels signal electrons from the silicon surface.

The magnitude E of this field is given by:

$$E = \frac{kT}{q} \frac{d}{dx} [\ln N_B(x)] \qquad (1)$$

where k = Boltzman's constant

T = temperature (°K)

q = electronic charge

$N_B(x)$ = boron concentration profile

(3) <u>Bonding</u>. Backside illumination requires a header which provides for frontside bonding and backside imaging. For intensification applications, the header must be compatible with vacuum processing and with photocathode formation.

This paper discusses the results of the processing developed to meet these requirements.

II. Analysis

Prior to discussion of the processing results, an analysis of the backside structure will be given for the case of photon illumination. In order to simplify the analysis, several assumptions about the structure will be made. It will be assumed that:

(1) The bare silicon surface is a region of high electron-hole recombination, characterized by a surface recombination velocity, S ;

(2) the boron accumulation layer produces a uniform electric field extending from the surface to the edge of the depletion region; and

(3) the minority carrier diffusion length in the bulk away from the surface is sufficiently long that recombination (R) in the bulk can be neglected compared to surface recombination. These assumptions are summarized in Figure 1.

The quantum efficiency and dark current

characteristics of this structure can be calculated by solving the continuity equation for electrons,

$$D\frac{d^2n}{dx^2} + \mu E\frac{dn}{dx} + \alpha N e^{-\alpha x} - \frac{n-n_0}{\tau} = 0 , \qquad (2)$$

where n = electron density,

D = electron diffusivity,

μ = electron mobility,

E = electric field,

α = silicon absorption coefficient,

N = incident photon flux,

n_0 = equilibrium electron concentration, and

τ = electron lifetime.

For this analysis it will be assumed that E is a constant. Although E is actually a function of x unless $N \sim e^{\pm x}$, the additional mathematical complexity does not add to the basic understanding. The actual value of E used will be an average for the entire accumulation region. The spatial variation of n_0 will be ignored.
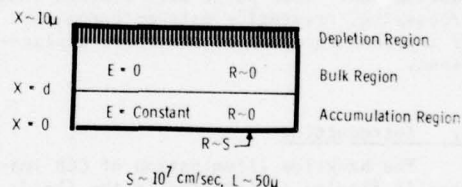
Figure 1

Similar analyses have been reported[6],[7], which employ the parameters of several layers within the silicon to describe the measured spectral response. The results presented here reproduce the wavelength dependence of this response using a single measured device parameter and the measured optical constants of silicon.

The boundary conditions needed to solve Equation (2) are determined by the recombination at the back surface and by the diffusion of electrons into the CCD depletion region at the front side. The first condition yields

$$D\frac{dn}{dx} = S(n-n_o) \quad \text{at } x = 0; \qquad (3)$$

the second yields

$$n = 0 \quad \text{at } x = d, \qquad (4)$$

where $x = 0$ is the back surface, and $x = d$ is the edge of the CCD accumulation region. This last equation is equivalent to assumption 3.

Equation (2) is easily solved subject to the boundary conditions (3) and (4). The electron current into the CCD is then obtained by adding the electron drift current and diffusion current at $x = d$:

$$I = D\frac{dn}{dx} - \mu En \quad \text{at } x = d. \qquad (5)$$

The quantum efficiency is the ratio of the photoelectron current to the photon flux, reduced by reflection losses:

$$QE = (1-r)(1/N)(1-I_D) \qquad (6)$$

where I_D is the dark current and r is the reflection coefficient.

The algebraic complexity of the resulting expressions is simplified by assuming an electric field magnitude such that

$$E > \frac{6kT}{q}\frac{1}{D\tau} \qquad (7)$$

For a 1 µs lifetime and $D = 5 \ cm^2/s$, this implies an electric field greater than 60V/cm.

From this assumption one obtains

$$I = \{q/(1 + S/\mu E)\}\{n_oS + [N/(D\alpha + \mu E - 1/\alpha\tau)]$$
$$[\mu E + S + D\alpha - e^{-\alpha d}(\mu E + S + \alpha D + S\alpha D/\mu E)]\} \qquad (8)$$

Additional simplification results from a comparison of the magnitude of each term. S is assumed to be a maximum equal to the electron thermal velocity of 10^7 cm/s. The diffusivity value and mobility were assumed to be high concentration values[9]. The absorption coefficients were obtained from published results[10]. For values of E less than 5000V/cm, it was found that $D\alpha < 4 \times 10^5$ cm/s, $\mu E < 1 \times 10^6$ cm/s, and $1/\alpha < 10^4$ cm/s. Therefore, neglecting the small terms, equa-

tion 8 becomes

$$I = q\{\mu En_o + N/(1 + D\alpha/\mu E) - Ne^{-\alpha d}\} \qquad (9)$$

Using the relationship $D = \mu kT/q$, one obtains

$$I = q\mu En_o + qN(1 + kT\alpha/qE) - qNe^{-\alpha d} \qquad (10)$$

The quantum efficiency predicted by Equation (10) is determined using Equation (6) with $I_D = \mu En_o$. The result is

$$Q.E. = [1 - r]\{[1/(1 + kT\alpha/qE)]-e^{-\alpha d}\} \qquad (11)$$

The quantum efficiency is seen to be limited by reflection losses $(1 - r)$, transmission losses $(e^{-\alpha d})$, and recombination losses. The recombination term involves the ratio of the thermal voltage, kT/q, and a voltage defined by the electric field and the absorption coefficient. This suggests the mechanism for the wavelength dependence of Equation (11). When an electron is generated at a distance x from the back surface, a potential difference of E times x exists between x and the back surface. If E times x is less than the thermal voltage, kT/q, significant recombination can occur. E times $1/\alpha$ represents an average potential difference.

For longer wavelengths, not all photons will be absorbed in the field region, $x < d$. The $e^{-\alpha d}$ term in equation (11) represents these photons. Some of these photons will be absorbed, however, in the region $x > d$ and will contribute to the quantum efficiency. To account for this it will be assumed that all of these photons are absorbed and that all resulting electrons are collected by the CCD. This, in effect, removes the $e^{-\alpha d}$ term from the quantum efficiency equation. This assumption will be valid for sufficiently high bulk lifetime and for wavelengths which are completely absorbed in ∿ 10 microns. This limits the validity of the assumption to wavelengths of less than 0.9µ. For longer wavelengths, multiple reflections occur which complicate the analysis.

Equation (11) is plotted in Figure 2 (with the $e^{-\alpha d}$ term deleted) with the field,

E, as a parameter. The quantum efficiency is strongly dependent on E for fields less than 5000V/cm. Above this value, reflection limited response is approached.

The dark current generated at the back surface can also be determined from Equation (8) by evaluating Equation (5) at $x = 0$ with $N = 0$ (no illumination). The results are:

$$I_{DC}(x = 0) = qn_o S/(1 + S/\mu E) \qquad (12)$$

For the case considered above, $S > \mu E$, this equation becomes

$$I_{DC}(x = 0) = q\mu n_o E \qquad (13)$$

In order not to degrade the CCD dark current characteristics, this current must be negligible.

At first glance the field dependence of the quantum efficiency (Equation 11) and the dark current (Equation 13) appear to be inconsistent; both Q.E. and dark current increase with E. However, the dark current is also proportional to n_o. Both n_o and E are related to the boron concentration at the surface:

Figure 2

$$n_o = n_i^2/N_B \qquad (14)$$

and

$$E = \frac{kT}{q} \frac{d}{dx}(\ln N_B) \sim \frac{kT}{q} \frac{1}{d} \qquad (15)$$

To first order, E is independent of N_B, while n_o decreases with N_B. This allows a proper choice of accumulation parameters so that the field can be maximized while n_o is reduced, resulting in high quantum efficiency without increased dark current.

The results of this analysis will be compared to experimental results in the following sections.

III. Processing Results

(A) Thinning. After completion of slice processing and multiprobe evaluation, the imagers are thinned to the desired membrane thickness. The thinning results are illustrated in Figure 3. This figure shows a two-inch silicon slice into which 0.4 inch square membranes have been etched. The membrane is approximately 10 microns thick, allowing the transmission of red light. The dark frames around each membrane are provided for support.

Thickness non-uniformities cannot be detected visually. The uniformity can best be determined by an optical interference technique. This employs infrared radiation which is only weakly absorbed by the silicon. Incoming and reflected radiations interfere, producing fringes in the imager response. This is illustrated in Figure 5, which shows the video display of the output of an imager illuminated from the rear with 1.1 micron narrow band ($\Delta\lambda = 16$Å) radiation. Each fringe represents a region of constant thickness. The thickness variation between adjacent fringes is given by

$$\Delta d = \frac{\lambda}{2N} \qquad (16)$$

where $\lambda = 1.1$ microns and $N = 3.4$. The thickness variation indicated in Figure 4 is about 0.3 micron. The active area of this imager is 0.9 cm x 0.7 cm. This thickness variation therefore corresponds to a taper of approximately 0.005 degrees.
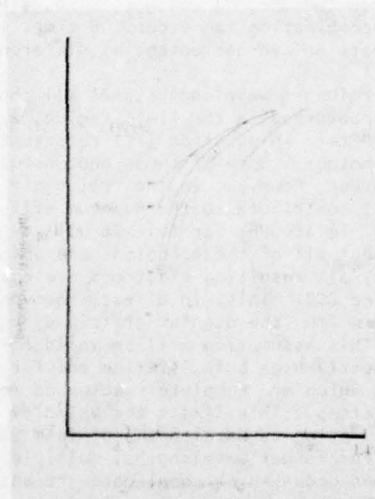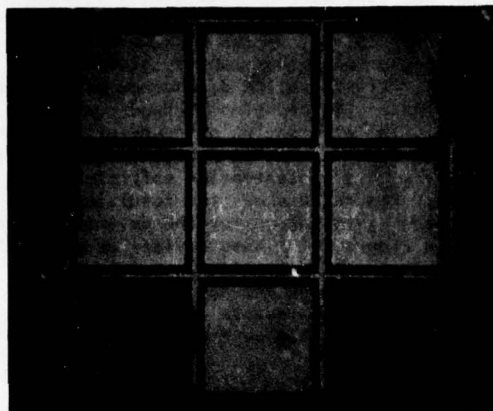
Figure 3
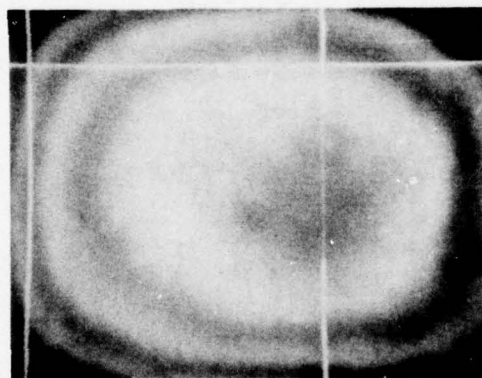
Figure 4

Membranes as large as 1.2 cm square have been produced without difficulty.

An imager parameter associated with the

membrane thickness is the modulation transfer function (MTF). MTF curves at 0.4 micron illumination for thinned imagers with 22.9 micron square pixels are shown in Figure 5.

(B) Accumulation. The results of the Texas Instruments accumulation process are illustrated in Figure 6. This shows the spectral response characteristics of sixteen 100 x 160 devices. The average and standard deviation at each wavelength is shown. These devices were not selected for high spectral response; the results indicate the normal spread in response obtained from the process.

Another parameter directly affected by the accumulation process is the electron gain during intensified operation. This is defined as the ratio of the CCD output current to the incoming accelerated electron current. The results of gain measurements on seven completed ICCDs are summarized in Figure 7. The reproducibility illustrated in Figure 6 is also evident here.
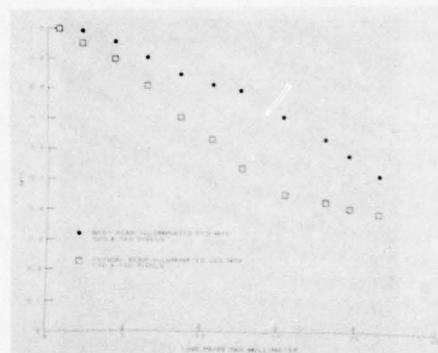
Figure 5

In order to compare the spectral response results to the analysis reported earlier, the average electric field in the accumulation region was determined by making boron concentration profile measurements. It was determined that the average field was approximately 400V/cm. Equation (11) was evaluated using this field for wavelengths from 0.4μ to 0.8μ. In Figure 8 the results are compared to the measured response. It can be seen that the analysis predicts the wavelength dependence rather well, but the

1-45
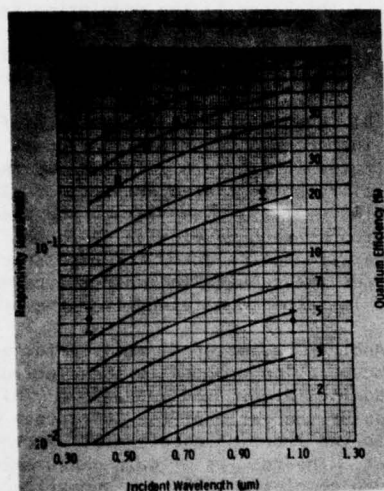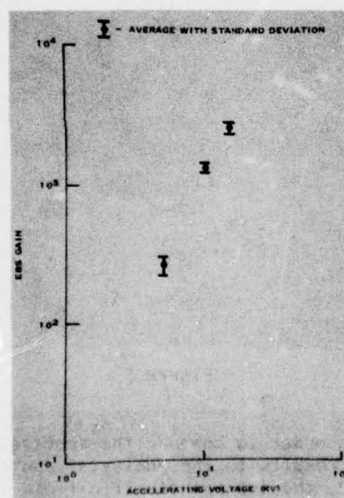
Figure 6

Figure 7

calculated magnitude is less than the measured response. The ratio of the calculated response to measured response is 81 percent plus or minus 6 percent from 0.5μ to 0.8μ. The source of this magnitude discrepancy is under investigation.

The dark current predictions of Equation 13 were verified by determining the CCD dark current versus back surface boron concentration. The results, given in Figure 9, illustrate the dependence of the dark current on the backside surface concentration. The elimination of rear-surface-generated dark current can be achieved by maintaining this concentration sufficiently high. Figure 10 shows the resulting dark current distribution for the devices reported in Figure 5. (These devices were selected from a set of completed devices on the basis of dark current magnitude; the data presents the achievable dark current magnitude and its relative frequency of occurrence.

(C) Packaging. Thinned imager arrays require special packages which allow frontside bonding and backside illumination. Figure 11 illustrates a package employed in intensified charge coupled device operation. Several problems were initially encountered in implementing these packages:

1. low package fabrication yield;

2. chip attachment to the package can cause membrane buckling or fracture;

3. gold wire bonding to aluminum bond pads leads to "purple plaque."

Figure 8

shows a completed imager beam-lead bonded to a flat ceramic substrate.
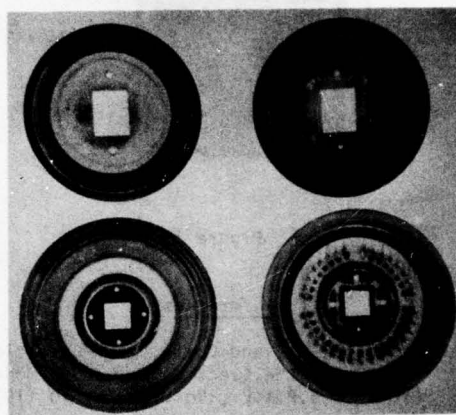
Figure 9

Figure 11

Figure 10

III. Conclusion

The processing of imagers for backside illumination has been developed to the point that reproducible spectral response, EBS gain, and dark current results are obtained. A simple theory has been developed which predicts the wavelength dependence of the spectral response using only measured parameters. The theory also predicts the observed dependence of the dark current on the backside surface concentration. The resultant understanding of the process effects on the spectral response (and EBS gain) allows further development toward reflection-limited quantum efficiency.

To eliminate some of these problems, gold beam lead bonding has been developed for thinned imagers. This allows the bonding of imagers with the frontside down--significantly reducing the required complexity of the package. In addition the beam leads tend to isolate the membrane from the thermal stresses introduced by the package, eliminating buckling. Figure 12 shows an imager with beams added to the bond pads. Figure 13

Figure 12

Figure 13

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List of Figures

Performance Evaluation of CCD Imagers

C. R. Monro

Introduction

The Naval Electronics Systems Command recently supported a program to develop CCD photosensor imaging arrays under a contract with Fairchild Camera and Instrument Corporation. The development effort resulted in two versions of CCD imagers, a 190(H) x 244(V) element array and a 380(H) x 488(V) element array utilizing interline transfer, buried channel technology. Two camera systems were fabricated to demonstrate sensor performance. This report details tests which were performed on these systems at the Naval Air Development Center in Warminster, Pennsylvania.

Test Conditions

A collimator was used to generate test imagery. A collimator is essentially a high quality lens with an illuminated transparency located at the focal distance of the lens. Thus, a camera system's lens looking into the collimator sees an image at infinity.

Test patterns were illuminated with a 2854K tungsten source operated without an infrared blocking filter. Light level variations were made with aperture type filters to permit use of the camera lens at a single aperture and to avoid color temperature changes. Wavelength dependent tests were made with a high intensity incandescent source and narrow band color filters. No corrections were made for lens performance.

Light value calibrations were made with a Spectra-Pritchard Model 1980 photometer for 2854K measurements and with a Molectron PR200 radiometer for the wavelength dependent measurements. Photographs were made from a CONRAC Model RQA 17-inch TV monitor, on Polaroid type 57 film. A more detailed discussion of evaluation techniques for solid state imagers may be found in reference 1, where the measurement problems peculiar to the CCD and CID structures are described.

Sensitivity

Using a 100% contrast USAF resolution slide in the collimator, monitor photographs were taken with the sensor surface illumination varied from 1.4×10^{-1} down to 1.7×10^{-5} fc (foot-candles). These tests were made with the 380 x 488 camera, and with the sensor array maintained at 0° C. As light level was reduced, amplifier gain was increased as required to maintain a constant video output (equal to the 80% saturation value at high light level) or until no usable improvement was obtained (low light level, fixed pattern disturbance limit reached). Controls were also available for adjustment of clock voltages on the sensor. The horizontal readout clock controls were initially optimized for maximum signal amplitude (display contrast) at each light level. The results obtained are illustrated in figure 1. Note that the lowest light level for perception of the image is limited primarily by the fixed pattern interference, not by random electrical noise.

A more practical adjustment of the clock controls is a single setting for all light levels. Here, the clock adjustments were set for the best compromise between good resolution and minimum fixed pattern interference over the entire range of

light levels. The result, illustrated in figure 2, was improved resolution and a more limited low light range as compared to figure 1.

Note in both illustrations that the dynamic range for quite usable picture information extends over a 75:1 ratio. The difference in resolution noted probably indicates that the increased sensitivity of figure 1 was due to incomplete charge transfer. For a 30% contrast pictorial target (a "real world" scene), minimum discernable pictures were limited to a higher light level. This is illustrated in figures 3 and 4.

Limiting Resolution

At the same time that the photographs of figures 1 and 2 were taken, a close visual inspection of the monitor screen was made to obtain readings of limiting resolution. Figure 5 illustrates the measurements made with a white background (black bars) slide. Note that the element size in both of the arrays is 0.030(H) x 0.018(V) mm, resulting in Nyquist points of 16.7 and 27.7 line pairs per millimeter, respectively. For the 8.8 mm vertical size of the 380 x 488 array, this corresponds to values of 294 and 488 TV lines per picture height, respectively.
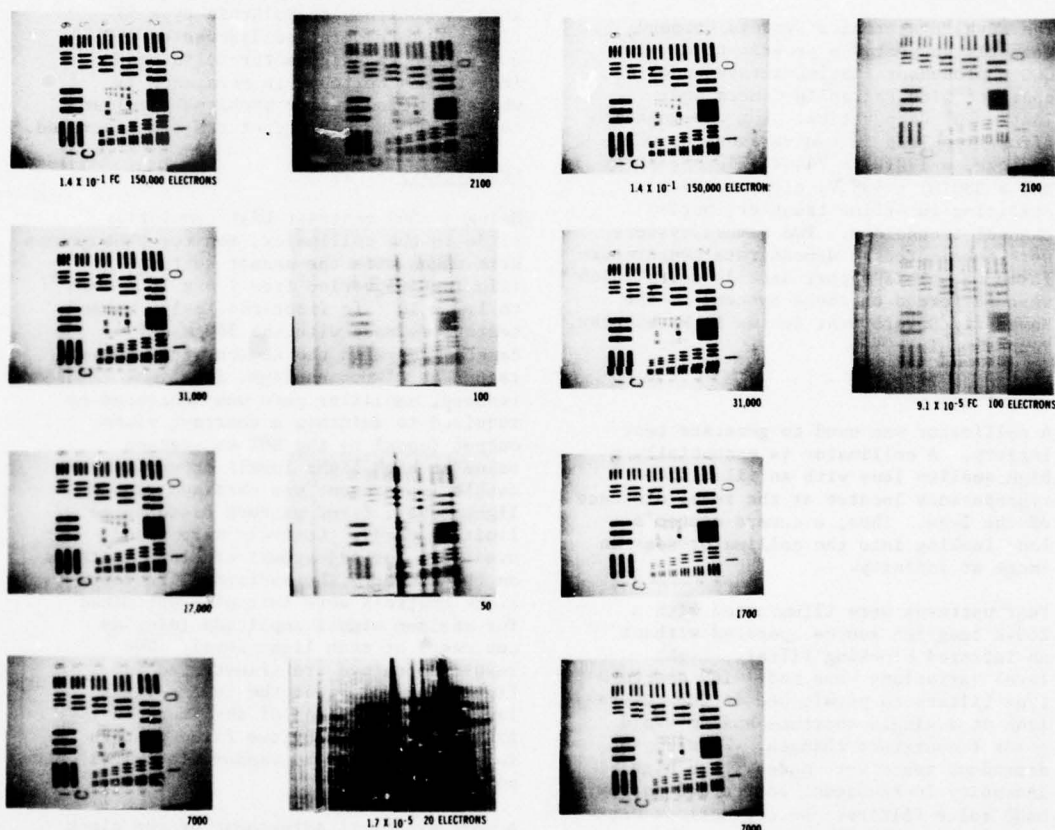
FIGURE 1 - USAF Test Pattern (100% Contrast) H Clocks Set for Maximum Contrast at Each Level

FIGURE 2 - USAF Test Pattern (100% Contrast) Normal H Clock Adjustments

1-50
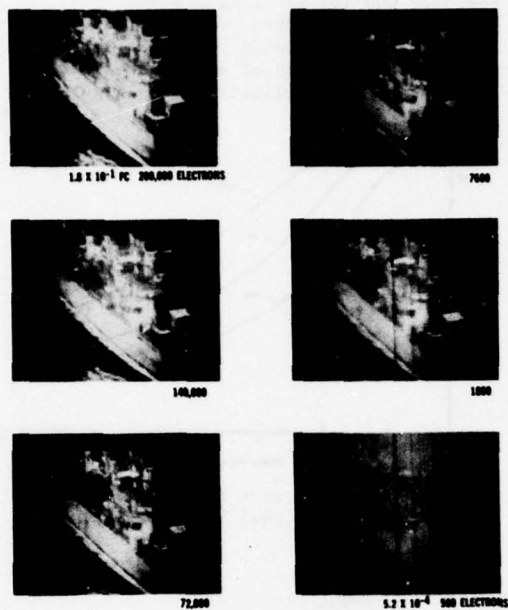
FIGURE 3 - Ship Scene (30% Contrast)
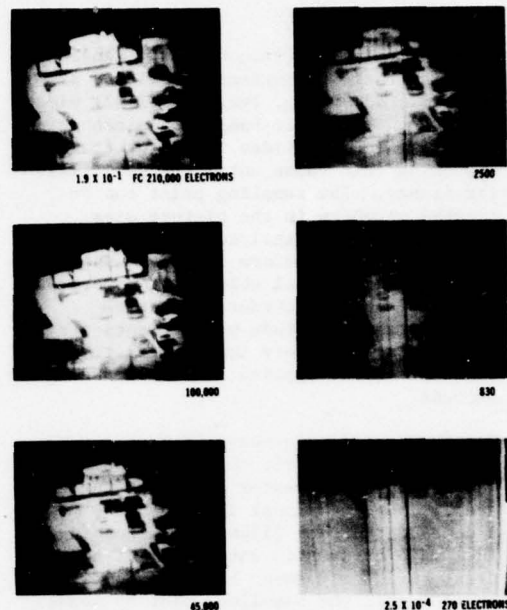
FIGURE 4 - Dock Scene (29% Contrast)

As shown in the photographs of figures 1 and 2, pattern information may only be seen, at low light levels, in small areas amid large fixed pattern and shading disturbances. Measurements were therefore made by moving the test pattern until bars just at the limit of resolution were located in such an optimum area.

Additional data points, obtained with *low contrast slides, were plotted in figure 6* to show the effect of contrast variation upon resolution. Note that limiting resolution does not fall until contrast is below 20%.
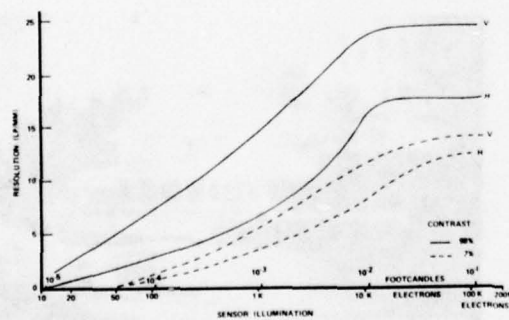
FIGURE 5 - Resolution Versus Light Level
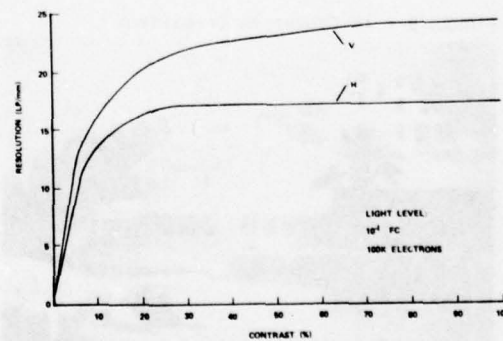
FIGURE 6 - Resolution Versus Contrast

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Square Wave Response

Video sampling for response and signal-to-noise ratio measurements utilized a CVI (Colorado Video, Inc.) Model 321 video analyzer. This unit samples a given point on a line in each video field (or frame) and holds that value until the next field (or frame). The sampling point can be located anywhere in the picture area. The output of the analyzer represents a high frequency waveform converted into a low frequency signal which may be recorded on an X-Y chart recorder. Accurate waveform and amplitude measurements are possible since a very long filter time constant may be applied in the recording process.

For the square wave response measurements noted in this report, the sample point was fixed at the center of the picture area. Thus the signal amplitude was independent of any illumination shading. The image of a SAYCE pattern (100% contrast, frequency sweep bars) was optically moved across the sampling point by means of a translatable slide carriage. Measurement of signal amplitude versus spatial frequency were taken from an X-Y recording of the sampled CVI output.

Figure 7 shows the effect of white light level variation on square wave response. Figure 8 shows the wavelength dependent performance. Focus was optimized for each wavelength.

For light levels near saturation, horizontal square wave response was measured to be 65% at the Nyquist point of 16.7 lp/mm. Figure 8 shows that square wave

FIGURE 9 - IR Crosstalk Comparison

response was lowest at long wavelengths. This was also observed as an increase in apparent sharpness of a pictorial subject with the application of an infrared cut-off filter, as is illustrated in figure 9.
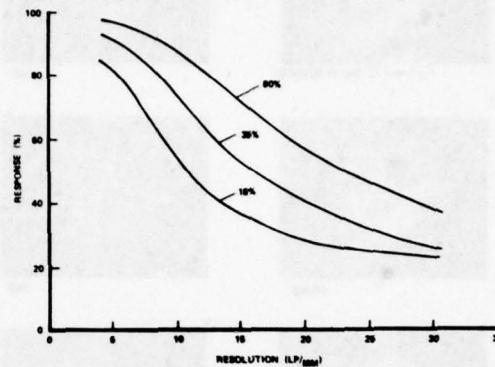
FIGURE 7 - Square Wave Response Versus Light Level (% of Saturation)
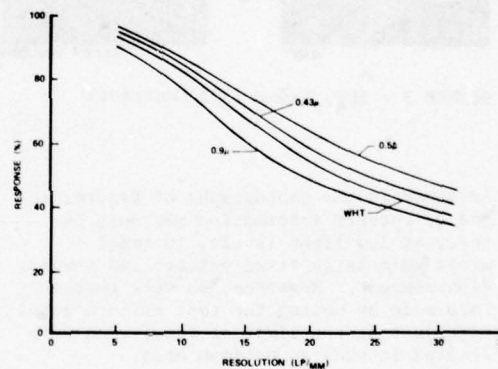
FIGURE 8 - Square Wave Response Versus Wavelength

NO FILTER

IR CUTOFF FILTER
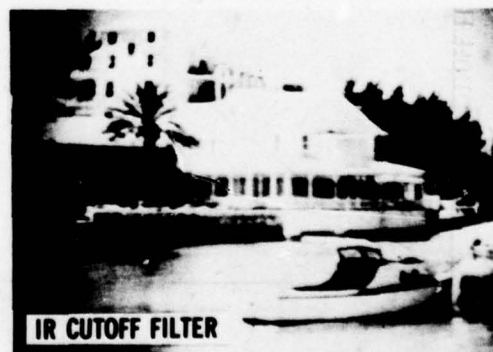
Signal-to-Noise Ratio

For SNR (Signal-to-Noise Ratio) measurements, the sampled output of the CVI unit was processed in an Intronics R301 RMS module to derive the AC noise component over a long averaging period.

Using a simple low frequency bar pattern, readings of white and black signal amplitudes were taken while at the same time the noise level in the white area was measured. The difference between white and black amplitudes, divided by the rms noise level in the white area, is defined as the SNR. The test results are shown in figure 10. The highest light value represents a point just below saturation.

The reproduced image was remarkably free of the familiar random noise effect even down to the light level where picture information was obscured by fixed pattern disturbances (below 10^{-3} fc). At 10^{-2} fc the SNR was 60 (36 dB).
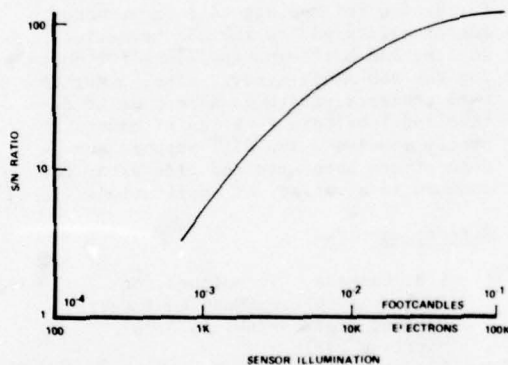
FIGURE 10 - Signal to Noise Ratio Versus Light Level

Image Spreading

Image spreading was measured by placing a very small light source in a long focal length collimator. This provided a spot of light approximately the size of a single CCD element, on the sensor surface. Neutral density filters were used to control the intensity.

The photographs in figure 11 illustrate the results. The light intensity for the "normal" condition was adjusted to be just below saturation. Note that there are two white spots visible in the center area of the picture. The upper left one is the light spot while the lower right one is a defect in the sensor. Subsequent photographs in the sequence illustrate the light spot image spreading as the light spot intensity was increased.
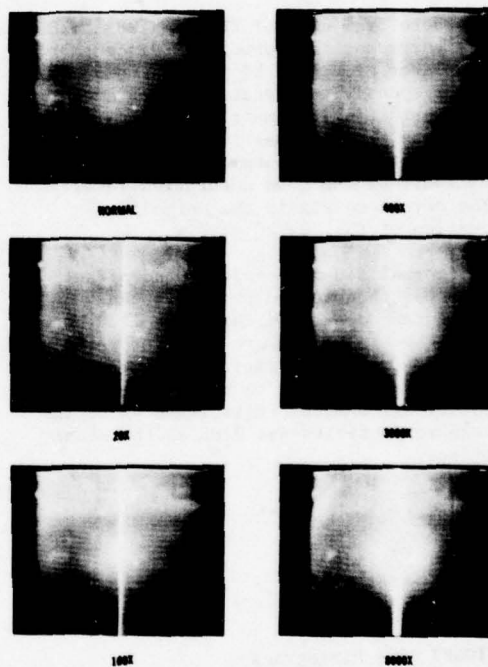
FIGURE 11 - Image Spreading

A qualitative measure of the spreading was made by recording the output of the CVI line sweep sampling function on the X-Y recorder. At a 20:1 light overload a spread of the displayed spot to three elements and the appearance of a two element wide saturated vertical line was noted. At an extreme (8000:1) overload, the resulting display spot was 26 elements wide with 6 columns saturated.

Uniformity

The degree of variation of responsivity and offset level was assessed using a 128 x 128 element subarray central to the 380 x 488 element sensor. A Biomations Model 8100 transient recorder under control of a Varian Model 72 minicomputer was used to sample voltage levels at each of 128 contiguous pixels or 128 contiguous lines of video. The process was done once with the array uniformly illuminated near the saturation level, and once in complete darkness.

The data from each of the two 128 x 128 element scans is stored on a disc memory and later processed by the minicomputer. The responsivity signature is obtained by subtracting the matrix sampled in darkness from the matrix sampled at full illumination, and normalizing to an estimate of the mean saturation level. The offset matrix is the normalized version of the "dark" matrix.

The normalized responsivity and offset data was then sorted to derive the histograms presented in figure 12. Note that the bin widths are 0.5% for responsivity and 0.2% for offset. The standard deviation was found to be 1.4% for offset. 99% of all samples fell within 4% of the mean responsivity and 0.8% of the mean offset.

FIGURE 12 - Histograms
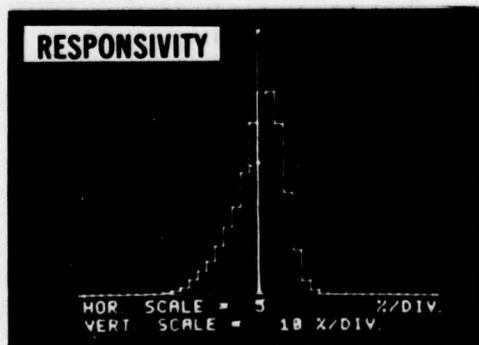
Conclusion

To sum up, excellent performance was demonstrated in many test parameters. Square Wave response measured 65% at the Nyquist point (294 TVL), SNR was 60 at 10^{-2} fc (36 dB), and limiting resolution was almost constant down to 20% contrast.

Imagery at a high light level was remarkably free of spot and column blemishes. However, the arrays tested did not produce a usable overall image at very low light levels, because of the severe fixed pattern and shading disturbances which appeared. Although performance readings were taken over a 10,000:1 range (1.9×10^{-1} to 2×10^{-5} fc) on the sensor, a more practical range was a 75:1 range (1.5×10^{-1} to 2×10^{-3} fc).

The low light level performance values, therefore, must be considered as an indication of possible performance if the "cosmetic" defects can be controlled in future production.

A follow-up contract is currently underway for design refinements to improve manufacturability and to include hermetic sealing and built-in provisions for cooling the 380 x 488 array. Also, under the same contract, there is a program to define and fabricate a series of camera system modules which will support and demonstrate both area and line array CCD sensors in a variety of applications.

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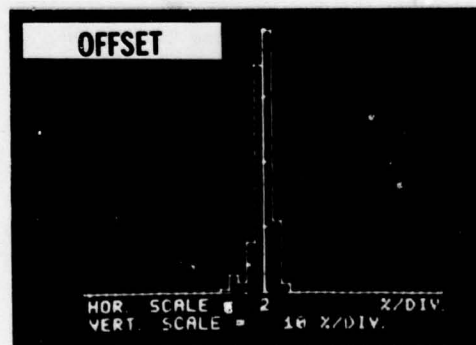
EFFECTS OF OPTICAL CROSSTALK IN CCD IMAGE SENSORS

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ABSTRACT/INTRODUCTION

It is a well-known phenomenon in silicon
image sensors that a significant level of
optical crosstalk occurs at wavelengths
longer than approximately 750nm and that
this crosstalk is due to the lateral dif-
fusion of minority carriers generated below
the depleted portion of the silicon substrate.
In addition, a low level of optical crosstalk
can occur at all wavelengths due to scatter-
ing and light-piping in the thin film portion
of the device. This paper describes these
effects quantitatively as they occur in
several different types of image sensors
produced at Fairchild. Comparisons with
predicted values are also made. Finally,
the impact of these effects on device per-
formance in practical applications is dis-
cussed.

THE MODEL FOR INTERNAL SPECTRAL RESPONSE

Before describing the crosstalk model used
for the various predictions, it is instruc-
tive to look at the basic model for internal
spectral response, i.e., for the response of
the silicon device assuming 100% transmittance
at the surface. This is a one dimensional
model consisting simply of a depletion layer
at the surface and, below this, a semi-infi-
nite neutral region of uniform minority
carrier diffusion length. Figure 1 shows
the general equation and a resulting spectral
response for particular values of the deple-
tion depth (L_D) and the diffusion length
(L_N, for an n-channel device). Also shown
in the figure is the portion of the response
due to diffusion. It is this portion of the
response that gives rise to virtually all of
the crosstalk observed in silicon imaging
devices. The diffusion response is predom-
inant in the infrared because the absorption
length (α^{-1}) is the greatest at these wave-
lengths. Depletion depths of 7 to 10μm are

typical in Fairchild charge-coupled imaging
devices. In general in CCD's, this deple-
tion depth is modulated by the gate potential
as it is clocked; a time average is then
assumed. Diffusion lengths of 50 to 100μm
are also typical, judging from the response
values typically observed. (Because of back-
contact recombination and a typical substrate
thickness of 200μm, longer diffusion lengths
do not change the response much.

MODEL FOR DIFFUSION CROSSTALK

Consider an infinitesimal diameter beam of
collimated monochromatic radiation at normal
incidence on a large area imaging device.
Photoelectrons generated in the neutral re-
gion will, on the average, diffuse laterally
a distance comparable with the depth of gen-
eration measured from the top of the neutral
region and then be collected in the depletion
region at the nearest potential minimum.
Figure 2 depicts this process; it is the bas-
is of the crosstalk model. The model neglects
any reduction of the depletion depth or ab-
sence of depletion at the channel-stop bound-
aries between elements. The assumption of
normal incidence can be made because even with
small f/no. optics the high refractive index
in silicon (>3.5) results in substantial in-
ternal collimation normal to the surface.

The most generally useful form of the charac-
terization of this crosstalk is the modulation
transfer function (MTF) factor (output mod-
ulation/input modulation). This is obtained
by integrating the above spreading process
over a sine-wave modulated large area of irra-
diation. The mathematical treatment of this
problem has been given by Seib, (Ref. 1).

An example result is shown in Figure 3 for
the case of L_D = 10μm and L_N = 100μm. From
this example one can see the most prominent

feature of the optical crosstalk character-
istic of most silicon imaging devices, namely
a large decrease in MTF as the wavelength is
increased from approximately 800nm to approx-
imately 900nm. This large decrease occurs at
spatial frequencies as low as approximately
10 line pairs/mm. (Because the absorption
coefficient increases slightly with tempera-
ture, these curves should be corrected for
large departures from room temperature; see
Table.)

The MTF is also affected by the optical aper-
ture of the elements. Thus, if the inte-
grated response of the array is uniform over
the entire area; i.e., if there is no loss
of response between the elements, and if the
boundary region is negligibly small, the MTF
is given by

$$\frac{\sin X}{X} \quad \text{where } X = \frac{\pi}{2} \frac{f}{f_N}$$

and where f_N is the Nyquist frequency---the
maximum resolvable frequency. In this ideal-
ized case the MTF is 0.637 at f_N. If the
boundary region is finite, there will be a
further reduction in the MTF. An example of
a resultant family of MTF curves for one de-
vice is shown in Figure 4; this is for a line-
scan device with a 13μm element spacing and
with 5μm neutral channel stop regions between
the primary depleted portions of the elements,
(Ref. 2). In these channel stop regions the
carriers are virtually all collected at one
or the other of the two adjacent depletion
regions and the partitioning of the response
is proportional to the distance from the far
side of the channel stop. (The data in the
figure is discussed later in this paper.)

MAJOR EFFECT OF DIFFUSION CROSSTALK
IN DIFFERENT IMAGE SENSORS

In area image sensors of the frame-transfer
type and the time-delay and integration (TDI)
type, the only effect of diffusion crosstalk
is on MTF. In line-scan image sensors a
second effect is significant, namely, infrared
response in the opaqued CCD readout regis-
ter(s). In normal operation this produces
a uniform black-level offset in the output
signal that is modulated by the integrated
image intensity. Thus, the black level will
be relatively accurate when only a small
fraction of the elements are exposed to a
high illumination level, but may have a sig-
nificant error when most of the elements are
exposed to the high illumination level.
Associated with this register response is

a loss of infrared response at the photo-
elements. A typical predicted photoelement
response, with the corresponding predicted
total response for the one-dimensional model,
is shown in Figure 5. The maximum shift
register crosstalk occurs when most of the
array is irradiated at the highlight level.

In interline-transfer (ILT) area imagers
(Ref. 3), there are opaqued vertical regis-
ters interdigitated with columns of sensor
elements; crosstalk into these registers
leads to an analogous effect, namely, verti-
cal image smearing. For example, crosstalk
from an intense spot image will, because of
the way the device is clocked, result in a
uniform increase in signal in all the charge-
packets moving through the adjacent shift
registers. At the display this increase in
signal will appear as a vertical smear which
is uniform over the full height of the pic-
ture. Figure 6 shows a schematic cross-
section of the device. Whereas in the line-
scan device described above, the metal ex-
tends from the opaqued registers over the
photoelements by 11μm, in ILT area imagers
it is necessary to employ much smaller dimens-
ions of 2μm to 6μm. The reason for holding
this dimension small is that it directly
affects the responsivity of the device and/or
the cell size. In the Fairchild CCD211, a
244 X 190 element ILT image sensor with a
horizontal cell dimension of 30μm and a hori-
zontal aperture of 14μm, an increase of over-
lap from 2μm to 6μm would result in a decrease
in responsivity of more than 50 percent.
Figure 7 shows how the level of the smear
signal in the CCD211 varies with wavelength.
Here a parameter called the charging ratio (r),
is plotted; the inset in the figure shows how
the smear signal varies with this ratio and
the size of the bright spot causing the smear.
The charging ratio is the ratio of the shift
register photocurrent, caused by crosstalk, to
the photoelement current.

The predicted curve in Figure 7 shows that at
600nm the charging ratio should be less than
one percent. However, as shown in the figure,
typical devices have a charging ratio of
approximately two percent. This excess is
also seen to be more or less independent of
wavelength. This excess crosstalk is attri-
buted to optical scattering in the polysilicon
gate; the scattering could occur both at oxidi-
zed grain boundaries and at sloped edges of any
of the exposed polysilicon layers.

METHODS OF MEASUREMENT

Crosstalk measurements with a light spot image and with bar-pattern images have been made with a B&L metallurgical trinocular microscope head mounted on rails over a large mechanical stage. The device and socket are mounted rigidly to the stage. The third eyepiece tube holds either the light spot source or a small projector box equipped with lamp, diffusers, filter holders and the mask holder.

The spot source is a Sylvania C2T lamp with a circular incandescent source of approximately $100\mu m$ diameter. Small-aperture baffles at several points along the optical path minimize flare. Intensity is controlled with a pair of crossed polarizers. Both B&L and Nikon 20X objectives have been used successfully to obtain crosstalk values on $13\mu m$-pitch-arrays of approximately 3% for the nearest neighbor element. This low level of crosstalk (at short wavelengths) establishes the quality of the optical system.

Only narrow-band and medium-band measurements are considered definitive with this system, no attempt has been made to achieve a spectrally flat system as would be required with calibrated broadband sources. For each filter the system is refocused when using refractive objectives.

For characterization of device crosstalk vs. wavelength, it is desirable to have optics that are not affected by wavelength; that is, to have a reflective objective. A Beck-Ealing 15X reflective objective was used for such measurements. For best results care should be taken that the reflective elements have been properly aligned. In the measurements described here, using a light spot that would ideally have had a diameter of approximately $5\mu m$, and making a short wavelength ($\leq 600nm$) measurement on a $13\mu m$-pitch array, the nearest-neighbor signal read 7% instead of the 3% obtained with the best refractive objective, and the second nearest neighbor read 2% instead of <0.5%.

In all of the data presented here, those taken with the reflective objective were corrected while those taken with the refractive objectives are assumed not to need correction.

All data were taken on photoelements near the preamplifier of the device so that charge transfer inefficiency was negligible.

MTF CHARACTERIZATION OF THE CCD121H AND CCD131

In order to make MTF measurements, one should ideally have a sine-wave modulated image of known amplitude. However, such a source was not available for the measurements described here. Instead, it was decided to use a chrome mask (which would ideally produce a square-wave modulated image) and then determine at what spatial frequency the 15X reflective objective would blur this into approximately sine-wave modulation. Since light spot measurements showed that the image sensor was operating within a few percent of ideal performance at short wavelenghts ($\leq 600nm$), the problem became one of finding the spatial frequency where the measured data matched the predicted performance. This was found to occur at 0.67 f_N (25 lp/mm) within experimental accuracy. Next the output modulations were measured at the longer wavelengths at this one spatial frequency. The ranges of the data for several typical devices are shown in Figure 4. The agreement with theory is not as good as the estimated precision of measurement which is $\pm 10\%$; in the 700-800nm range, the experimental values of MTF are lower than predicted; at 1000nm they are higher.

In a previously published paper, Vicars-Harris (Ref. 4), presents square-wave response (CTF) data for a sample device of this same type, i.e., a Fairchild line-scan CCD image sensor with $13\mu m$ elements. It is of interest to compare the two sets of data. The Vicars-Harris data includes the losses due to the lens and, even though the lens is recognized for its high resolution---it is a 3 inch B&L Super Baltar--- the relative response is significantly lower. For example, in a 700-800nm band, the Vicars-Harris CTF value at 25 lp/mm (0.67 f_N) is 53%, while our corresponding MTF value (the average of 700nm and 800nm values) is 63%.

LIGHT SPOT CHARACTERIZATION OF THE CCD121H AND CCD131

While it is possible in principle to use MTF data to compute the spread function for a light spot, it is of interest to measure some directly. Figure 8 shows light spot data for light spot diameters significantly less than the element size; the spot diameters are only approximate. From this data it may be seen, for example, that at 900nm the second-nearest neighbors receive a signal which is 7.5% of that of the center element.

PREDICTED PERFORMANCE FOR AN ADVANCED ILT IMAGE SENSOR

As described above (see Figure 7), the ILT type of image sensor exhibits vertical smearing due to crosstalk into the vertical registers. Given that the CCD211 in Figure 7 has a charging ratio of 15% at 800nm, it is desirable to improve the design so as to reduce this value to the order of one percent or less. Increasing the metal overlap over the photoelements should help somewhat, but the largest gain should come by increasing the depletion depth. Unfortunately, current material and processing constraints on substrate doping for good manufacturability limit the minimim doping level to approximately $1 \times 10^{14}/cm^3$ (130Ω-cm). Similarly the voltage that can be applied across the depletion layer is limited by considerations of manufacturability; a realistic goal is 20V. The result is an increase in depletion depth from 7μm to 17μm. In a new design, which also includes an antiblooming sink stripe adjacent to each column of photoelements, the predicted charging ratio at 800nm is reduced approximately three fold---not as much as desired, but nevertheless a significant decrease. The improvement is shown in Figure 9 where, instead of showing monochromatic data, we show broadband data as a function of long-wavelength cutoff, achieved with an external filter. Characterized this way at a cutoff wavelength of 800nm, the charging ratio is decreased in the new design from 4% to approximately 1%. Thus, a bright spot with a diameter of 1% of picture height would cause a smear signal of 1×10^{-4} times the spot signal.

SUMMARY

Diffusion crosstalk can severely limit the performance of CCD image sensors at wavelengths beyond approximately 850nm. This performance limitation has been discussed in detail for several imaging devices. Both the crosstalk to neighboring photoelements and that to adjacent shift registers can be significant.

REFERENCES

1. D. H. Seib, "Carrier Diffusion Degradation of Modulation Transfer Function in Charge Coupled Imagers", IEEE Trans. El, Devices ED-21, March, 1974, pp. 210-17.

2. The CCD121H and CCD131 are two-register line-scan devices with 1728 elements and 1024 elements, respectively.

3. For a detailed description of an ILT device, see the paper by W. Steffe, L. Walsh, and C. K. Kim, "A High Performance 190 X 244 CCD Area Image Sensor Array", Proc. of the 1975 International Conference on the Application of CCD's, NELC, San Diego, October 29-31, 1975, pp. 101-108.

4. M. Vicars-Harris, "Slow Scan Operation of Long Linear CCD Arrays", Proc. of the Symposium on CCD Technology for Scientific Imaging Applications, JPL, Pasadena, March 6-7, 1975, pp. 175-85.

ACKNOWLEDGEMENTS

TABLE: ABSORPTION LENGTH OF SILICON AT TWO TEMPERATURES

α^{-1} (um)	λ (nm)	
	300°K	77°K
2.5	600	540
5	705	605
10	795	715
25	880	815
50	940	870
200	1000	940
1000	1060	980
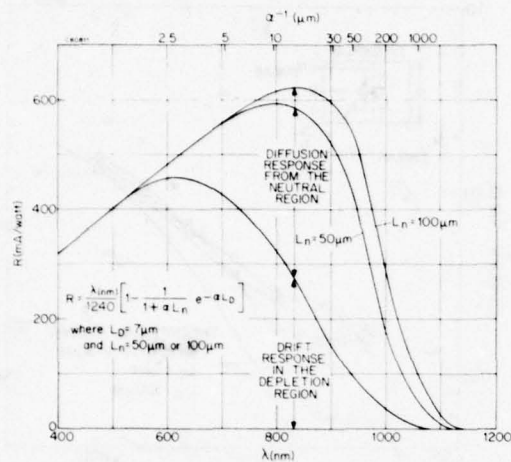
Fig. 1 Theoretical internal spectral response based on a one-dimensional model
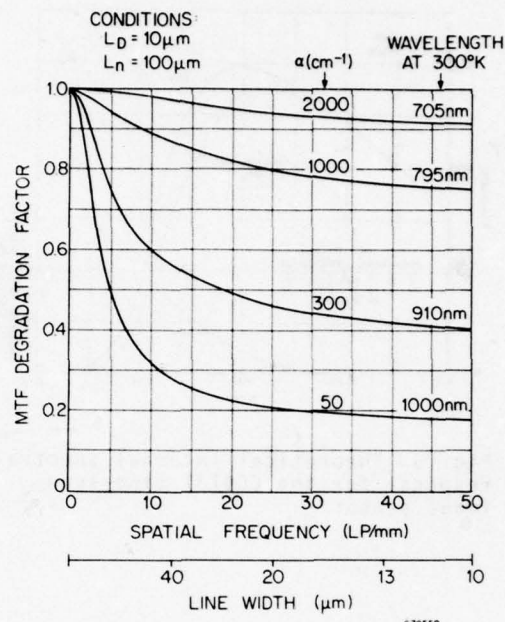
Fig. 3 Calculated MTF degradation factor vs. spatial frequency and wavelength
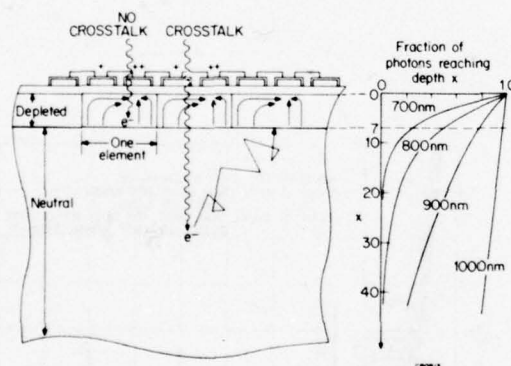
Fig. 2 The optical crosstalk process
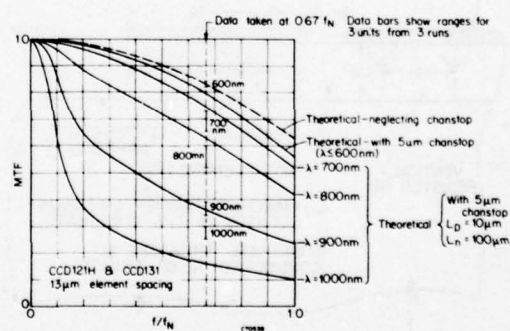
Fig. 4 In-phase MTF vs f/f$_N$ for a line-scan image sensor
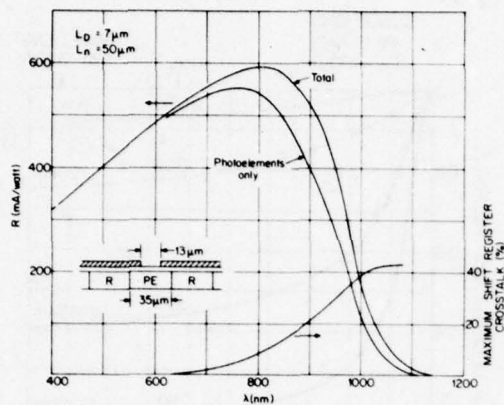
Fig. 5 Theoretical internal spectral response for the CCD131 line-scan image sensor
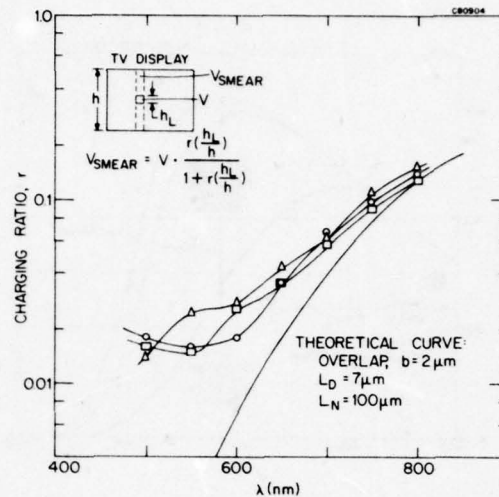
Fig. 7 Charging ratio vs. wavelength for three typical CCD211 ILT image sensors
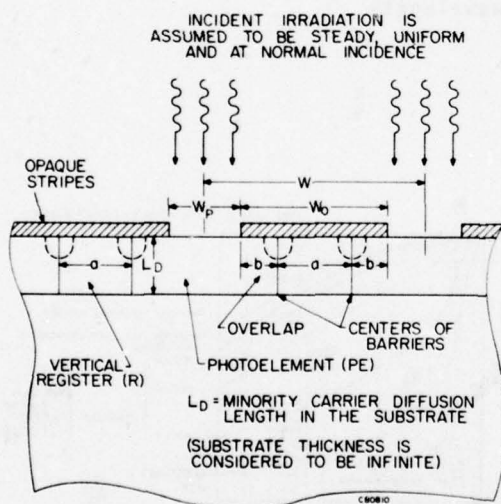
Fig. 6 Model for the calculation of deep carrier crosstalk in an ILT image sensor
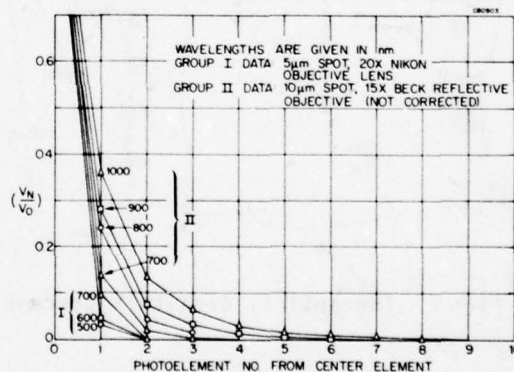
Fig. 8 Optical crosstalk of a typical CCD121H line-scan image sensor characterized using a light spot
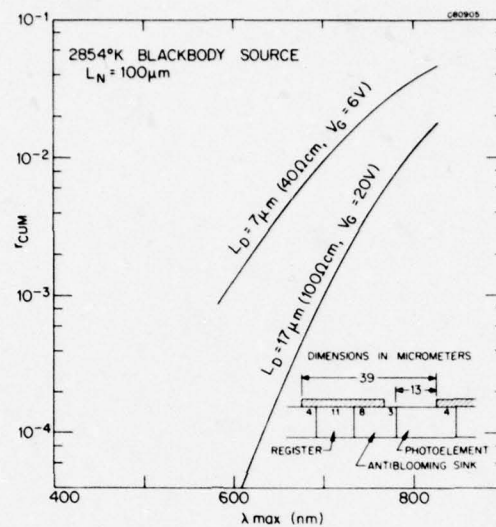
Fig. 9 Cumulative charging ratio
vs. cut-off wavelength

"MINIATURE CCD CAMERAS"

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ABSTRACT

Texas Instruments has developed a series of miniature charge coupled device (CCD) cameras. The motivation behind and application of each camera has been different. Described here are two cameras from this series, which demonstrates the broad range of TI camera technology. Discussed first is a 327 x 490 pixel TV compatible camera which can be used for applications requiring a TV format. Described next is a 48 x 24 pixel time delay integration (TDI) camera which can be used for scanning applications. Although some of the cameras in this series have utilized 3-phase, backside illuminated CCDs, both cameras described here utilize 2-phase, buried channel, frontside illuminated CCDs which were designed and fabricated specifically for these cameras.

Special features of these cameras include:

- Two-phase, frontside illumination
- Buried channel technology
- High charge transfer efficiencies in excess of 0.9999
- Antiblooming control (TIC-5)
- High resolution
- Standard 525-line TV format (TIC-5)
- Time-delayed-integration operation (TIC-7)
- No residual imaging (image lag)
- No microphonics
- Single voltage and low power requirements
- Small size

- High resistance to image burn-in
- High uniformity
- No residual bias (fat zero) required

TIC-5: A TV Compatible CCD Camera

The TV compatible camera, which is called TIC-5, is shown in Figure 1. As shown, the camera can quickly be adapted for use in either of two configurations. Figure 1a shows the camera as it is used for standard TV applications; Figure 1b shows the camera configured with a remote sensor head for applications requiring an ultra-small sensor.

Figure 1a.   Standard Configuration TIC-5 Camera
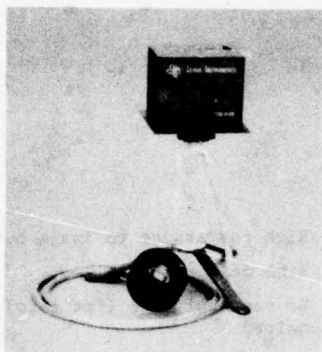
Figure 1b. Remote Head Configuration
TIC-5 Camera

General Discussion

The TIC-5 camera utilizes a 327 x 490 (160,230 pixels) CCD as a 327 x 245 imager operating in the frame-store mode to generate standard 525-line TV pictures. The CCD employs two-phase, bur.ed channel, frontside illuminated techniques to achieve very high charge transfer efficiencies. An antiblooming structure is also included to prevent the stored charge from spreading while viewing brightly illuminated objects. This structure has demonstrated blooming control at overloads greater than 10,000. However, frame-store architecture limits effective control to approximately 1,000X overloads due to streaking.

Basically, a CCD imager is a device which integrates photons for a given time period, allowing photon generated charge to build up in the well, and then reads the charge out. On the other hand the standard TV format requires that dat be continuously read out except for a short vertical blanking period (1250 μsec), during each field, when the monitor is retracing. The frame-store mode of operating a CCD is one way to overcome this incompatibility.

In the frame-store mode of operation, the CCD is divided into two equal areas (as shown in Figure 2): one, a 327 x 245 imaging area which is exposed to the incoming photon

irradiation, and the other, an identical 327 x 245 memory area which is opaque to the incoming irradiation. During operation the image area integrates photons for one TV field (1/60 second). Then during vertical blanking of the TV monitor, the entire image area is quickly dumped into the memory area. While data for the next field is being collected in the image area, the data from the previous field is read out, line by line, by shifting down into the horizontal serial register and out through an onchip output amplifier.
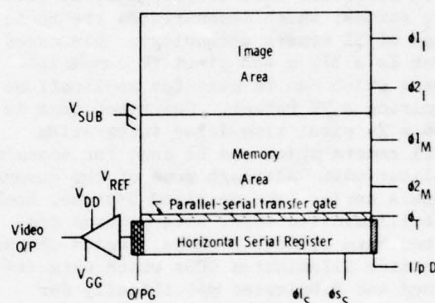
Figure 2. Frame-Store Mode CCD

Parallel Array Description

Both the image area and memory area consist of 80,115 MOS capacitors, each arranged into a matrix of 245 rows and 327 columns. The number of elements required in each area is determined as follows: a TV field consists of $262\frac{1}{2}$ lines ($242\frac{1}{2}$ readout lines and 20 retrace lines). Therefore, a minimum of 242 lines are required, and the number 245 was chosen. Since this CCD has square 0.96 mil by 0.96 mil picture elements (pixels), it follows that the number of pixels per line to give a four to three aspect ratio (TV standard) is 327. Each individual pixel has boundaries. consisting of built-in barriers in the horizontal direction and gate-controlled channel stops in the vertical direction as seen in Figure 3.
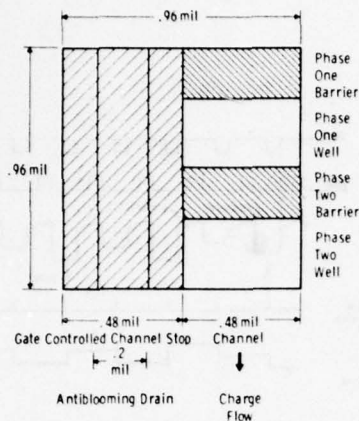
Figure 3. CCD Unit Cell

The method of interlacing used in this camera is accomplished by electronically shifting the centroid of integration for each well by half a cell dimension. This technique provides very little improvement in the vertical modulation transfer function (MTF), but does effectively double the vertical spatial sampling frequency. This tends to reduce the aliasing properties of the camera and improves the useful vertical resolution. Electronically, this method of interlacing is accomplished by biasing parallel phase electrode $\emptyset1_1$ on during field A and then biasing parallel phase electrode $\emptyset2_1$ on during field B. However, because in TIC-5 one electrode is polysilicon and the other is aluminum, there is a noticeable difference in the response between the two fields, and therefore the camera is most often operated in the non-interlace mode. By using a polysilicon version of the sensor, this problem is overcome.

Horizontal Serial Register

The horizontal serial register is used to shift the data, one line at a time, out of the CCD. This register sits idle for 10.9 μ-seconds during each horizontal blanking period while a new line of data is loaded into it and then clocks out serially at a 6.2 MHz data rate in order to be TV compatible. The data rate is determined as follows: a TV line readout is 63.5 μsec with a 10.9 μsec horizontal blanking period. Therefore the actual clocking time is:

$$t_{clocking} = 63.5 \ \mu sec - 10.9 \ \mu sec = 52.6 \ \mu sec$$

and the time to read one pixel is:

$$t_{pix} = \frac{52.6 \ \mu sec/line}{327 \ pixels/line} = 0.1609 \ \mu sec$$

The serial data rate then is:

$$f_{data \ rate} = \frac{1}{t_{pix}} = \frac{1}{0.1609 \mu sec} = 6.2 \ MHz$$

Timing Diagram

A timing diagram for the TIC-5 camera is shown in Figure 4. As shown, both the imager and memory clocks, $\emptyset1_1$, $\emptyset2_1$, $\emptyset1_M$, and $\emptyset2_M$, are clocked together, during vertical blanking (dump), for 245 times in order to load a new frame of data into memory. Then one of the image area clocks ($\emptyset1_1$ shown) is biased on to allow charge to accumulate during the integration period. The data stored in the memory section is read out by clocking the memory area clock $\emptyset1_M$ and $\emptyset2_M$, one cycle during each horizontal blanking period to reload the serial register. Then the serial register simply clocks 327 cycles to read the data out.
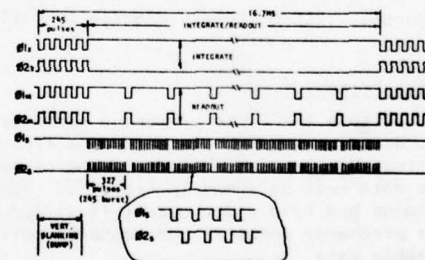
Figure 4. TIC-5 Camera Timing Diagram

An on-chip pre-charge, double-source follower amplifier is used to provide the

voltage waveform that is transmitted to the video processor circuitry. A diagram for this amplifier is shown in Figure 5. It functions as a resettable electrometer for detecting extremely small quantities of charge (down to fractions of femtocoulombs). The circuit consists of five MOSFETs, one (Q1) of which precharges the output diode of the CCD to a fixed reference voltage, V_{REF}, prior to the arrival of each charge packet. Two MOSFETs (Q2 and Q4) are used as source followers: the first to maximize the detection of charge, and the second to minimize output load impedances. MOSFETs Q3 and Q5 are on-chip loads for the corresponding source-followers.

Figure 6
TIC-5 Output Sampling and Timing Diagram

Figure 5. CCD On-Chip Precharge Amplifier

Video Processor

Within the video processor circuitry, the data are sampled and held at a time corresponding to approximately the center of the data well as shown in Figure 6. This sampled and held video output is stripped of the precharge pedestal and contains only desirable data.

Also, television sync signals are superimposed onto the sample and hold video to provide composite video, in accordance with the timing and synchronization portions of EIA RS-170 specifications, capable of operating into any standard TV monitor or commercial video tape recorder.

Physical Parameters

The TIC-5 camera is small; for example, in the remote sensor head configuration the main camera body occupies 10.5 in^3, and the sensor head occupies only 1.6 in^3. Although the camera is very small, it is constructed using basically standard discrete components. The rather dense packaging is largely attributable to using flat-pack integrated circuits and a technique known as hot-electrode welding. As shown in Figure 7, this is a method of interconnecting electronic circuitry by point-to-point wiring. As shown, on the back side of the printed circuit board, nickel wire with polyurethane insulation is welded to pure nickel pins in a point-to-point fashion. One of the welder electrodes heats up and melts the polyurethane insulation away just prior to making the spot weld. The flat-pack integrated circuits are then soldered to the front side of the board.

The TIC-5 camera dissipates three watts of power and requires only a single +12V DC voltage input. Drawing only 250 mA of current, the camera can be operated from a relatively small battery pack for up to two hours per charge.

Typical imaging pictures taken from the operating camera are shown in Figure 8. The black vertical line near the lower left corner of the image is caused by a blocked channel in the CCD parallel array.

Figure 7
Hot Electrode Welding Packaging Technique

Figure 8
TIC-5 Typical Imaging Pictures

The camera specifications are listed below:

Electrical Parameters

Typical operating voltage	+12 ± 1V
Typical operating power	3 watts
Data rate	6.2 MHz
Horizontal video bandwidth	3.1 MHz
Integration time	16.7 ms
Output voltage - composite	1.0 V

Optical Parameters
(327 x 490 CCD)

Image cell size	0.96 mils x 0.96 mils
Aspect ratio	4 x 3
Image area size	0.314 in x 0.235 in
Spectral response	0.40 μm to 1.1 μm
Blooming control above saturation	>1000 times saturation level-test device
Charge transfer efficiency, CTE	>0.9999
Resolution: Vertical	$\sim$ 170 TVL/ph
Horizontal	$\sim$ 250 TVL/ph
Dynamic range	60

TIC-7: A Time-Delay-Integration Scanning Camera

Although the TIC-7 camera, shown in Figure 9, is primarily a time-delay-integration scanning camera, it can be operated in a secondary mode as a full-frame imager. The sensor for this camera is a 48 x 24 (1152 pixels) two-phase, frontside illuminated CCD. This device is similar to the 327 x 490 CCD discussed earlier except for its smaller size and the fact that no anti-blooming structure is included. Figure 10 illustrates the operation of a CCD in both the full-frame and time-delay-integration modes. When operating in the full-frame or stare mode, the imager sits idle for an integration period and then is clocked out

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by shifting data down, one line at a time, into the serial register where it is then read out serially through an on-chip amplifier. In the primary time-delay-integration or scan mode, the imager is continuously read out in full-frame fashion as though the integration time is zero. However, the entire imager is scanned across the scene at the exact same rate at which the CCD is clocked out so that a pixel in the CCD field locks onto and tracks a point in the scene, until read out, to provide an effective integration period.

Camera Operation

The TIC-7 camera is designed to operate with a variable frequency with a master clock ranging from 384 kHz to 2.35 MHz. Table 1 shows the integration time range and required illumination level range for both the scanning and starring modes.

Mode	Master Clock	Integration Time	Minimum Illum. Level (2854°K Source)
Scan	384 kHz	6 msec	2.5 $\mu w/cm^2$
Scan	2.35 MHz	1 msec	15 $\mu w/cm^2$
Stare	384 kHz	31 msec	0.5 $\mu w/cm^2$
Stare	2.35 MHz	5.9 msec	2.5 $\mu w/cm^2$

A flow diagram illustrating the sequential operation of the camera is shown in Figure 11. In this diagram, X represents the number of counts in the pix/line counter, and Y represents the number of counts in the line counter. The X counter is 8 bits and therefore has a capacity of 256 counts while the Y counter is 5 bits and has a capacity of 32 counts. Initially, the X and Y counters are set to 208 and 8 counts, respectively. This represents the 48 pixels per line (256 - 208 = 48) and 24 lines (32 - 8 = 24) which ocrresponds to the TIC-7 sensor. In the scan mode only the pix/line counter loop is required. The circuit cycles around this loop, making a serial shift for each loop, 48 times until the serial register is read out. Then a parallel shift is made, loading a new line of data into the serial register. X and Y are reloaded and the cycle is repeated.

In the stare mode, the line counter loop is added so that after each line has been read out the line counter is increased by one count. After this counter indicates that one frame (24 lines) of data has been read out, the camera then enters the integration state. Here, additional loops are added to form an integration timer used to time out the integration period during which time the CCD sits idle. At the end of the integration period, the circuitry is reset, and the entire cycle repeated.
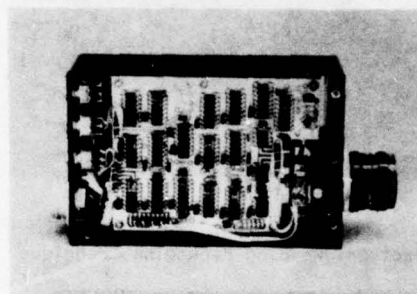
Figure 9. TIC-7 Camera

Full-Frame Mode
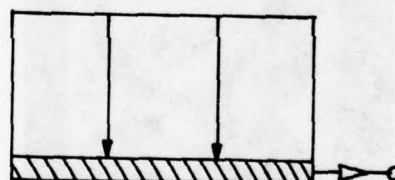
Integrate - Readout

Time-Delay-Integration Mode
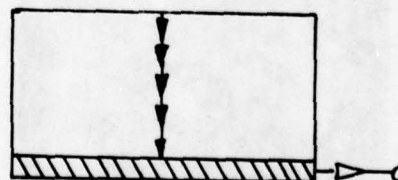
Shift continuously
Readout continuously

Figure 10. TIC-7 Modes of Operation
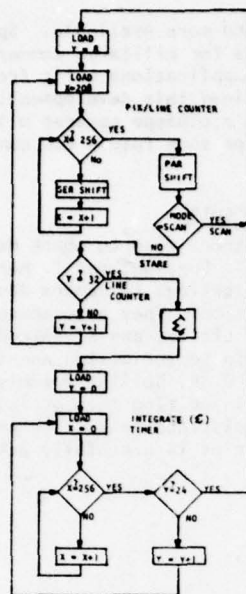
Figure 11. TIC-7 Flow Diagram

Figures 12 and 13 show an imaging picture and a uniform illumination picture, respectively, for the operating camera.
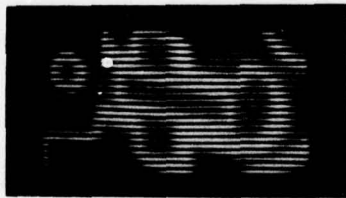
Figure 12. TIC-7 Imaging Picture

Physical Parameters

The TIC-7 camera measures 2"W x 4"H x 6"L and has a volume of 48 in3. Although the camera is somewhat larger, it is built
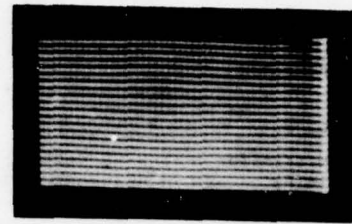
Figure 13
TIC-7 Signature-Uniform Illumination

in a modular fashion so that individual circuit cards can be quickly removed for repair and/or testing. The construction uses dual-in-line (DIP) packages interconnected using the hot-electrode welding technique discussed earlier. The TIC-7 camera, which includes an automatic gain control in its video circuitry, dissipates 4.3 watts of power and also requires only a single +12V DC voltage input.

A picture of the 48 x 24 CCD sensor is shown in Figure 14.
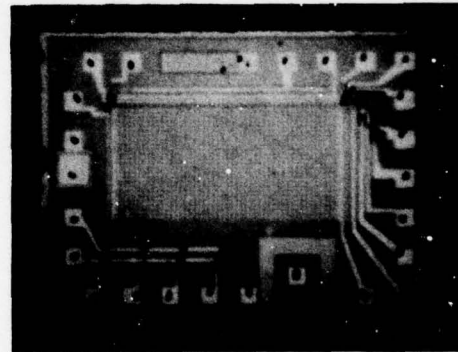
Figure 14. 48 x 24 CCD

Optical specifications for the TIC-7 camera are shown below:

Optical Parameters (48 x 24 CCD)

Image cell size	0.96 mil x 0.96
Aspect ratio	2 x 1

Optical Parameters (con't)

Image area size	0.046 inch x 0.023
Spectral response	0.4 μm to 1.1 μm
Dynamic range	300
Modulation transfer function (MTF)	∿30% at Nyquist limit

Spectral Response

Finally, the spectral response is shown in Figure 15 for typical CCDs with a built-in antiblooming structure. The three curves shown represent polysilicon-aluminum electrodes, polysilicon-polysilicon electrodes, and thinned backside illuminated devices, respectively.
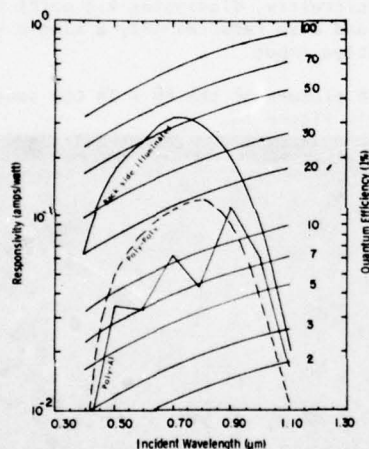
Figure 15. CCD Spectral Response

Summary

The two CCD cameras discussed here are representative of those which have been developed at TI. Although these cameras are only prototypes, built mostly from standard components, they demonstrate what is ahead on the CCD camera horizon. As large CCDs become available in quantity, very small and stable high resolution TV cameras will be-

come more and more available. Special purpose cameras for military, commercial, and industrial applications built from modular units will lead this development. The variety of TI's prototype cameras will form the basis for such future CCD cameras.

HgCdTe CHARGE-COUPLED DEVICES*

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ABSTRACT

This paper provides a review of progress on the technology and performance of HgCdTe CCD structures under development for infrared image sensors. First emphasis has been placed on infrared sensitive time delay and integrate (TDI) registers operating at 50 KHz and 77K temperature with long wavelength cutoff in the 3-5 μm range. Charge transfer efficiencies greater than 0.999 have been obtained for 16-stage shift registers. Infrared response with 48% quantum efficiency and detectivity in TDI of 2.8×10^{12} cm $Hz^{1/2}$/watt have been obtained in a 16-stage CCD with 4.3 μm long wavelength cutoff. Initial results on 32-stage shift registers are described.

I. INTRODUCTION

This paper will review progress on charge coupled devices fabricated on HgCdTe alloys at Texas Instruments Incorporated. The first report of CCD action in HgCdTe demonstrated a charge transfer efficiency of 0.996 for an eight-bit four-phase CCD shift register fabricated on $Hg_{.7}Cd_{.3}Te$.[1] These results were obtained for a temperature between 77K and 140K and for clock frequencies below 100 KHz. The first results on 16-stage CCD shift registers with charge transfer efficiency of 0.9995 and near theoretical infrared detectivity in a time-delay-and-integrate mode were reported in mid-1978.[2] These promising results on CCDs were preceded by MIS studies [3,4,5] and knowledge of HgCdTe bulk properties.[6,7,8] The present paper will detail the results on 16-stage CCD shift register and present initial results on 32-stage CCD shift registers.

The choice of HgCdTe for the fabrication of charge transfer devices has a number of advantages. Unlike the III-V alloys such as $Ga_{1-x}In_xSb$, the $Hg_{1-x}Cd_xTe$ alloy compositions can provide a bandgap approaching zero and a large range of band gap energy for only a small variation in lattice constant.[8] In comparison to the IV-VI alloys such as $Pb_{1-x}Sn_xTe$, the $Hg_{1-x}Cd_xTe$ alloys have a native oxide with excellent insulator properties and a much smaller thermal expansion coefficient [8] facilitating the design and packaging of the CCD.

HgCdTe alloys are presently used to fabricate arrays of photoconductive infrared detectors for use in infrared imaging systems operating in the 3-5 μm and 8-12 μm wavelength bands. The bias current for photoconductive detectors causes an excessive power requirement for the use of thousands of these detectors on a cooled focal plane. Photovoltaic detectors are under development for these wavelength bands and have merit in some applications, but have the disadvantage of requiring individual leads or bonds for each detector unless the detectors are fabricated on the same HgCdTe chip with a HgCdTe CCD multiplexer. For these reasons HgCdTe CCDs for infrared sensing and output multiplexing are desirable choices for an advanced infrared image sensor monolithic chip if charge transfer efficiency greater than 0.999 is obtained. Other HgCdTe devices such as charge-injection-devices and equilibrium MIS photocapacitors [4] are other possible choices with merit, but these approaches do not have the low output capacitance necessary for high voltage-responsivity and sensitivity nor the long integration times for on-chip time-delay-and-integration in an imager using a mechan-

ical scan; both advantages are inherent in the use of CCDs.

Section II of this paper will discuss the requirements placed on HgCdTe CCDs by the infrared imager application. Foremost among these requirements are (1) the need for a large charge storage capacity to store the charge generated by the ambient infrared back-ground and (2) the need for sufficently small dark currents. Section III will review the capability of HgCdTe MIS devices to meet these requirements; additional details on MIS properties will also be presented in later sections to explain the CCD test results.

The basic elements of the HgCdTe CCD design will be given in Section IV. Although the CCD design is intended for use as either p-channel or n-channel, all results to be presented are for p-channel operation. Sections V-VII will detail the operation of the HgCdTe CCDs as shift registers and as infrared sensors.

By varying the choice of composition, the $Hg_{1-x}Cd_xTe$ alloys with various long wavelength cutoffs can be obtained such as 5 μm at 77K, 5 μm at 192K, and 12 μm at 77K. In this study, alloys have been chosen which have long wavelength cutoffs in the 3-5 μm band at 77K. The potential for operation at longer wavelengths will be discussed in Section VIII.

II. REQUIREMENTS FOR IR IMAGE SENSORS

The goal of this program is to demonstrate the device technology necessary for the development of area image sensor arrays and first stage signal processing (such as time-delay-and-integration and multiplexing) on an intrinsic-response semiconductor monolith. Excellent reviews of the application of charge transfer devices as image sensors are available. [7,10] Figure 1 shows a generalized layout for a type of area imager utilizing parallel detector columns. In principle, each IR sensitive element of the array could collect the charge generated by each corresponding image pixel and the data bits then be clocked out very rapidly. This concept presents a difficult challenge for the development of a new device technology because of the large number of CCD stages which must operate successfully at a very high data rate if high resolution imagery is to be obtained for real time TV display.

Most IR imagers use a mechanical scanner to provide an image scan in at least one direction across the detector array. The area array of Figure 1 can be used with the mechanical scanner (vertical scan in Figure 1) if the column shift registers are clocked to keep the motion of the column wells in synchronization with the motion of the infrared image down the columns (a version of time-delay-and-integration operation, TDI). As will be shown, CCD shift registers of up to 32-stages operated at 50 KHz clock frequency can provide significant improvement in imager performance when used in a TDI mode in the mechanically scanned system. Thus, the development of HgCdTe CCDs for TDI and output multiplexers are appropriate goals for the initial development of HgCdTe CCDs.

The HgCdTe CCD infrared imager must provide an improvement in imager performance. The overall imager performance is characterized by the minimum resolvable temperature difference MRT at a given spatial frequency. The MRT of a system is determined by the optics, scanner, sensor array, electronic processing, the display, and the observer. In this paper, only those factors determined by the sensor array will be discussed: the noise equivalent differential temperature (NEΔT) and the modulation transfer functions (MTF) of the detector structure, scan and transfer inefficiency.

The NEΔT is determined by the minimum detectable signal which is equal to the wide band noise. An NEΔT of 0.1 C for a 300°K background will be chosen. Typical optics design parameters are f/3.3 for the signal photon radiance Δφ and f/2.0 for the 300°K background photon radiance ϕ_{BG}. An overall atmospheric and system transmission, τ, of 0.7 will be assumed. A detector quantum efficiency, η, of 0.5 and detector area, A, of $(25.4 \text{ μm})^2$ will be taken as a goal. The equation for the minimum detectable signal-generated carriers in an integrating detector with Δt integration is given by

$$\tau\eta\Delta tA \ \Delta\phi \ \sin^2\left(\frac{\theta_{sig}}{2}\right) = \left[\eta\Delta tA\phi_{BG} \ \sin^2\left(\frac{\theta_{BG}}{2}\right)\right]^{\frac{1}{2}}$$

(1)

where θ_{sig} and θ_{BG} are the full angles associated with the signal and background f/#'s. The same equation would be obtained for voltage outputs.

Rather than develop a formula which ex-

2-2

plicitly shows the NEΔT, a $\Delta\phi$ corresponding to the NEΔT will be inserted into formula (1) and the Δt required for equality will be derived. For a 3-5 μm wavelength bandwidth, $\Delta\phi$ (0.1 C) = 4.72×10^{13} photons/cm^2/sec and ϕ_{BG} = 1.32×10^{16} photons/cm^2/sec for a 300 K background. Use of the above parameters requires a total integration time, Δt, of 435 μsec. In TDI operation, $\Delta t = N\Delta t_D$ can be defined where N is the number of CCD stages and Δt_D is the detector dwell time (time for an image element to traverse the detector) which for the CCD is equal to the inverse of the clock frequency. A value of Δt_D = 20 μsec will be assumed which is equivalent to 833 detector dwell times in a full 1/60 sec scan. Thus, the 3-5 μm TDI CCD will require 22 stages to obtain 0.1 C NEΔT. CCD shift registers with 32 stages have been fabricated and tested in the present study.

As suggested by the above analysis, infrared CCD imagers can have overall noise set by the background infrared irradiance. The infrared image sensors experience much larger background irradiance than do visible or near-infrared imagers (which consequently cannot be made radiation background noise limited). The CCD must have a charge storage capacity sufficient to store the carriers generated by this large background irradiance or provide a background subtraction mode of operation. In addition, dynamic range for large signals must be provided. For 60 dB of dynamic range in signal photon irradiance referenced to a 0.1 NEΔT, the photon irradiance of the focal plane is

$$(2) \quad \phi_{BG} \sin^2\left(\frac{\theta_{BG}}{2}\right) + 10^3 \, \tau \, \Delta\phi \, \sin^2\left(\frac{\theta_{sig}}{2}\right).$$

For the parameters assumed, the 3-5 μm background provides 7.73×10^{14} photons/cm^2/sec and a total of 1.51×10^{15} photons/cm^2/sec for equation (2). For a 435 μsec storage time or 22 TDIs, this requires the storage of 5.25×10^{-8} coulombs/(cm^2-of-pixel-area) or 7.64×10^{-8} coulombs/(cm^2-of-pixel-area) for 32 TDIs. If the charge storage MIS well area is 50% of the total stage or pixel area, then a maximum charge storage capacity of 1.05×10^{-7} coulombs/(cm^2-of-well-area) is required for 22 TDIs and 1.53×10^{-7} coulombs/cm^2 for 32 TDIs.

The CCD clock voltages must be large enough to provide the charge storage capacity with the dynamic range required. However, the dark current for 22-TDI 3-5 μm

CCD must be compared to the background generated current (61.8 μa amps/cm^2-of-pixel-area or 124 μa/cm^2-of-well-area for 50% quantum efficiency) rather than the total maximum photon generated current. A very conservative approach would be to require that the dark current be less than 10% of the background current or 12 μa/cm^2-of-well-area.

Finally, the effect of bit geometry and clocking on the modulation transfer function, MTF, must be considered. It is useful to remember the difference between (1) aperturing in space and time which determines the respective MTF values and (2) placing the sample (with these apertures) in space and time which can cause aliasing or sidebands. The spatial aperture of the CCD stage or pixel is given by the stage length (for quantum efficiency constant across the bit). The detector MTF is given by

$$(3) \quad MTF_D = (\pi \ell f_x)^{-1} * \sin(\pi \ell f_x)$$

where f_x is the image spatial frequency on the detector and ℓ is the stage length. For a square detector, this MTF_D applies to both the scan and cross scan directions.

There is also an MTF due to the fact that the CCD wells move discontinuously in steps while the infrared image moves continuously along the CCD. This MTF depends on the number of phases, p, which determine the number of times a CCD potential well steps in traversing one CCD stage; this integration time per phase is $\Delta t_D/p$ where Δt_D is the detector dwell time. The infrared image moves one stage or detector length ℓ in a detector dwell time ($\Delta t_D = \ell/v$) as related by the image velocity, v, on the focal plane. This $MTF_{\Delta t}$ due to time aperaturing during image motion is

$$(4) \quad MTF_{\Delta t} = (\pi v \Delta t_D \, f_x/p)^{-1} * \sin(\pi v \Delta t_D f_x/p)$$
$$= (\pi \ell f_x/p)^{-1} * \sin(\pi \ell f_x/p)$$

$MTF_{\Delta t}$ affects only the scanned TDI direction and has no effect on the cross scan direction. For spatial frequencies less than the first zero of MTF_D ($f_x = \ell^{-1}$), the effect of $MTF_{\Delta t}$ is not appreciable for four phase clocks (p=4) and is not large for two phase clocks.

The solid line in Figure 2 shows the product $MTF_D * MTF_{\Delta t}$ for a two phase CCD

with a 25.4 μm long detector/stage in the direction of scan. The sample frequency f_s in terms of sample pairs is shown by the vertical arrow at $f_s = \frac{1}{2\ell}$ in Figure 2. This is the case for a CCD with all its stages infrared active. For a CCD with isolation bits which are inactive or whose data is thrown away, $f_s = \frac{1}{4\ell}$. Image spatial frequencies above f_s will be aliased to lower frequencies and appear as false signal. The spatial frequencies passed by the optics MTF will make the total camera MTF (= MTF_D * $MTF_{\Delta t}$ * MTF_{optics}) considerably less than the 0.57 shown at f_s in Figure 2. A criterion that the total camera MTF be less than 0.4 at the sampling frequency (sample pairs) has been suggested as a guide.[11]

Finally there is an MTF_ϵ associated with charge transfer inefficiency in the CCD.[9,10] This MTF is given in terms of the charge transfer inefficiency, ϵ, by

(5) $MTF_\epsilon = \exp\,[-n\,(1-\cos\,2\pi\,\ell\,f_x)]$

where $n = 1/2\,Np$ with N being the number of stages in the CCD, p being the number of phases, and the factor 1/2 arising from the fact that signal charge is being added to each stage of the TDI rather than into the first stage as in a simple shift register. The various dashed curves in Figure 3 shows the product MTF_D * MTF_ϵ * $MTF_{\Delta t}$ (2-phase) as a function of nε. If $n\epsilon \leq 0.1$ is chosen as a goal for the maximum permissible MTF degradation for a 32-stage two phase TDI CCD, then $\epsilon \leq 3\times10^{-3}$ and CTE ≥ 0.997 are required. A CTE of 0.999 will therefore be adequate.

MTF in the cross scan direction depends on a number of design parameters which have not yet been fixed. Likewise, cross talk in the serial multiplexer depends on the number of columns to be multiplexed and whether isolation bits are to be used;[12] although these factors have not yet been fixed, a CTE = 0.999 would permit the fabrication of useful modules in which the output of a number of TDI columns could be combined on one signal output line. A complete discussion of topics is not warranted at this stage of development.

III. CAPABILITIES OF HgCdTe MIS DEVICES

This section will address those requirements set out in Section II and add further details on HgCdTe material and MIS

properties.

Dark current is the first major question. The four major dark current contributions are tunneling, depletion layer generation current, minority carrier diffusion current, and surface generation current.

Tunneling at the edge of a constant charge density depletion layer has been derived by W.W. Anderson.[13] In practical cases of interest, the Anderson result can be simplified to give

(6) $I\,(Tunnel) \cong \dfrac{q\epsilon_o\epsilon_s E_s^4}{\pi^4\hbar N\,E_G^2}\,\exp\left(-\dfrac{\pi}{2\sqrt{2}}\,\dfrac{\sqrt{3}}{\sqrt{2}}\,\dfrac{1}{P}\,\dfrac{E_G^2}{E_s}\right)$

where E_s is the electric field at the edge of the depletion layer, E_G is the bandgap, N is the carrier concentration, ϵ_s is the HgCdTe dielectric constant, and P is the interband matrix element in the k·p model and is 8.0×10^{-8} eV-cm for HgCdTe. The approximations of surface potential much larger than bandgap and the exponential coefficient larger than 14 (current slightly above threshold) have been used. All calculations to be reported utilize the more complete formula of Anderson.

The generation of dark current density in the depletion layer in a strongly depleted MIS well is given by

(7) $I\,(w) = \dfrac{q\,n_i\,w}{2\tau_g}$

where n_i is the intrinsic carrier concentration, w is the depletion layer width, and τ_g is an effective lifetime.

The minority carrier diffusion current density for thick samples is given by

(8) $I\,(D) = \dfrac{q\,n_i^2}{N}\,\sqrt{\dfrac{kT}{q}\,\dfrac{\mu}{\tau}}$

where N is the majority carrier concentration, μ is the mobility of minority carriers, and τ is the minority carrier lifetime in the neutral and quasi-neutral regions underneath the depletion layer. Because of the temperature dependence of the n_i^2 term, I(D) will be larger than I(w) at 190K for 5 μm HgCdTe, but I(w) will be larger than I(D) at 77K.

The surface generation current density is given by

$$(9) \qquad I(s) = \frac{q \, n_i \, s}{2}$$

where s is the effective surface recombination velocity in cm/sec.

In addition to the above terms, avalanching current multiplication will occur at high electric fields for moderately high doping concentrations.

Figure 3 shows the amount of charge collected in an MIS well as a function of the duration of the integration based on the depletion layer approximation. These predictions are for 5 μm HgCdTe at 77K and include the dominant terms of tunnel and depletion currents. The dashed line at the left shows charge collected from the $120/\mu a$ cm^2 infrared background requirement of Section II. The two cases in the middle of the figure are for two different carrier concentrations with MIS gate voltage adjusted to make the initial tunnel current 10% of the infrared background generated current. As can be seen, the rate at which charge is collected due to tunneling decreases with time as the electric field at the edge of the depletion layer decreases with buildup of inversion charge. At times much longer than the 400-600μsec system integration time required, the depletion layer current becomes dominant and determines storage time in the absence of infrared.

Although the sample with $2 \times 10^{15}/cm^3$ carrier concentration has a longer dark storage time as shown by the vertical arrows, the sample with $4 \times 10^{14}/cm^3$ carrier concentration is preferred because of larger charge storage capacity. The dotted curve at the right hand side shows that a reduction in gate voltage for the $4 \times 10^{14}/cm^3$ sample still leads to a storage time less than that for the $2 \times 10^{15}/cm^3$ sample. At 190K, all current components would be important at the initiation of the integration.

The requirement that the dark current be equal to 10% of the infrared background generated current can be used to predict the variation of maximum well capacity with ZnS insulator thickness and carrier concentration. Figure 4 shows the predictions for maximum well capacity based on tunnel current alone at 77K. A choice of 50% of the infrared current would not make a large change because of the exponential dependence of tunnel current on E_s. The vertical arrows in Figure 4 show

typical ZnS thicknesses for the first and second level gates. The horizontal line shows the charge capacity requirement (per-cm^2-of-well-area) for 32 TDIs. A carrier concentration of $1 \times 10^{15}/cm^3$ is sufficient to meet the requirements. Figure 5 shows the gate voltage required to attain the charge capacities of Figure 4.

The theoretical prediction of charge transfer inefficiency depends on a number of imperfectly known parameters for HgCdTe MIS devices. The 77K bulk mobilities for 5 μm HgCdTe are known from Hall measurements to be 400 and 40,000 cm^2/volt-sec for holes and electrons respectively, but the surface mobilities can only be estimated to be one-half these values. Fast surface state densities have been studied by various capacitance-voltage and conductance techniques. Typically, the conductance is too small for successful measurement on 5 μm HgCdTe devices at 77K. Likewise it is too difficult to reach quasi-static conditions [14] at this temperature. Measurements of dC/dV give no indication of any significant localized density of fast surface states, and the Amelio technique [15] implies a fast surface density of $2 \times 10^{11}/cm^2$-volt near flat band. However a comparison of high frequency and low frequency C-V curves made at temperatures above 77°K indicate that this density of fast surface states may be too high. Conductance measurements of depleted and weakly inverted surfaces at these elevated temperatures are also not consistent with the value of 2×10^{11} $cm^{-2} V^{-1}$. Indications are that the discrepancy is due to statistical fluctuations in the local density of fixed charge in the oxide.

The primary source of charge transfer loss and inefficiency at low frequencies in CCDs operating with a fat-zero charge is trapping in fast interface states at the edge of the CCD well. The near-horizontal lines in Figure 6 show the predictions of theory [16] for edge-induced fractional loss per transfer for p-channel HgCdTe. In addition to the parameters listed on the figure, the signal charge was assumed to be 0.8 full well and the surface state capture cross section for holes was assumed to be 10^{-17} cm^2. The calculation is for clock voltage of 5 volts riding on a substrate bias of 0.5 volts above threshold.

At higher frequencies with optimum design, the transit time across a CCD gate

is determined by fringing field drift. The near-vertical lines in Figure 6 show the predictions for charge transfer loss based on this theory. [17]

The best charge transfer efficiency of 0.9995 to be reported on a 16-stage 51 μm-wide CCD with 10.2 μm long electrodes can be fit with a fast surface state density of 6.3 x 10^{10}/cm^2-volt. This value is below the value measured by dC/dV techniques and supports the speculation that the dC/dV measure is too large because of statistical fluctuations in fixed charge in the oxide.

IV. HgCdTe CCD DESIGN, FABRICATION AND OPERATION

The HgCdTe used in this study was grown by the solid state recrystallization technique which normally gives ingots consisting of a few large crystallites with compositional homogeneity of 0.3 mole 0/0. The samples were annealed in a mercury-rich atmosphere to reduce the carrier concentration. $Hg_{1-x}Cd_xTe$ samples with 0.295 < x < 0.315 were selected for this study. Hall measurements indicated an n-type carrier concentration $1-2x10^{15}$/cm^3 and an electron mobility of $4x10^4$ cm^2/v-sec at 77K. The carrier concentration measured by MIS analysis using test capacitors on the MIS test bars also indicated $1-2x10^{15}$/cm^3.

All CCD designs utilized a four phase structure with tunnel (or avalanche) breakdown at an MIS-gate input and an MIS gate output. Figure 7 shows a photograph of two 16-stage HgCdTe CCD shift registers with transparent electrodes. The channel widths of the two CCDs are 127 μm and 50.8 μm as defined by the aluminum field plate for these two designs. The infrared active channel widths are 119 μm and 43.2 μm as defined for the two CCDs by the intersection of the thin nickel and thick aluminum metal layers on each gate. All phase wells are 10.2 μm long. The floating gate well is 20.4 μm long. The photomask design includes optional input and output diodes.

Figure 8 shows cross sectional views across and along the length of the CCD channel. In all cases, the first level insulator is a 700Å thick native oxide on the HgCdTe. Various designs with different thicknesses of evaporated ZnS have been used. The ZnS under the aluminum field plate is typically 1100Å thick. The ZnS under the

first level gates is typically 2600Å-2700Å thick. The total ZnS thickness under the second level gates has been varied from 5300Å to 8900Å.

Figure 9 shows the capacitance voltage characteristics for electrodes on a 16-stage CCD shift register which used all aluminum opaque electrodes. All insulators included 700Å of native oxide (dielectric constant = 17) plus the following ZnS (dielectric constant = 7.5) [3] thicknesses: 1100Å to the field plate, 2600Å to the first level gates (ϕ_2, ϕ_4, etc.) and 6800Å to the second level gates (ϕ_1, ϕ_3, etc.) The flatband voltages for these three levels are approximately -2.7V, -6.0V, and -13.0 volts respectively. These values are consistent with $7.3x10^{11}$/cm^2 fixed charge and -0.7 eV work function difference. Other devices have had fixed charge densities as low as $4x10^{11}$/cm^2. The capacitance voltage curves show a hysteresis of about 0.1 volts characteristic of charge trapping. Beyond flatband voltage these devices show the characteristics of deep depletion with storage. Other devices with good CTE action showed high frequency characteristics at 10 KHz (but with no storage).

Figure 10 shows a generalized schematic of a 16-stage CCD with the floating gate output circuitry. The gates denoted by IG-1 and OG-2 were kept dc accumulated. The four phases were driven with four phase clocks. The clock voltages could be adjusted so that the storage capacity of all wells were similar (true four-phase operation) or so that the second level wells had little storage capacity (a quasi-two phase mode.) In the shift register measurements, an input breakdown pulse about 0.2 μsec in duration was applied to IG-2. It is not known whether the input charge is due to tunnel current at very high bias or to avalanche breakdown. Electrode OG-1 was used as either a dc or a pulsed output gate. Figure 11 shows a clock sequence used for the shift registers. Most measurements were performed with 50 KHz clocks so that the on-time (negative-going pulses) is 10 μsec for all phase clocks. Although a 9 μsec wide injection pulse is shown, an injection pulse width of 2 μsec was more typical. As can be seen from Figure 11, the input signal occurs when both phase-one and phase-two are on. With infrared input, the CCD could be operated with the same waveforms with or without the shift register signal input. "Freeze clock" measurements were also performed in

which the clocks could be stopped for an adjustable duration with any one of the phase clocks on and the other phases off. In this format, dark current or infrared signal is integrated during the freeze duration. At the end of the freeze duration, the clocks begin operation in proper order and the integrated charge per stage is clocked out to the floating gate.

The floating gate was preset empty well before dumping the signal charge into the well from the phase-four well. Signal was usually detected by clamping before the injection pulse and sampling after the injection pulse. Signal detection was also performed on occasion using slosh of charge into or out of the floating gate well. The experimental node capacitance on the measurement node varied from 5 pF to 40 pF depending on the output circuit, injection capacitor value, and whether the first stage apmlifier was inside or outside of the sensor.

The signal voltage, ΔV_S, can be related to the charge transferred or injected, ΔQ_S, by an approximate relationship with stray capacitance C_p, insulator capacitance C_{INS}, and the average $\overline{C}_d$ of the depletion layer capacitance before and after injection.

$$(10) \quad \Delta V_S \cong \frac{\Delta Q_S}{\overline{C}_d + C_{INS} C_p / (C_{INS} + C_p)} \frac{C_{INS}}{C_{INS} + C_p}$$

Since the output is ac coupled, the ΔQ_S corresponds to the signal charge while dark current or fat zero is not measurable(but limits the size of ΔQ_S). Dark current could be measured with the freeze clocks. Approximate values of C_{INS} and $\overline{C}_d$ for the floating gate of the 127 μm wide CCD are 0.57 pF and 0.44 pF respectively which are both much smaller than the strong capacitance. Thus, the value of ΔV_S is given by

$$(11) \quad \Delta V_S \simeq \frac{\Delta Q_S}{C_p} \frac{C_{INS}}{\overline{C}_d + C_{INS}} \simeq \frac{\Delta Q_S}{1.8 \, C_p}$$

The charge ΔQ_S delivered to the floating gate is limited by the charge capacity of the phase-two or phase-four electrodes which are half the area of the floating gate. For a maximum charge density of 1×10^{-7} coulombs/cm^2 (Figure 3) and the 127 μm wide channel, the maximum voltage signal is 72 mV for the measured 20 pF stray capacitance.

A new CCD test bar is being tested with a number of new structures. Results will be reported on a 32-stage CCD with a 35.6 μm wide storage channel, 25.4 μm wide infrared active channel, and 25.4 μm bit length. For the measured 5 pF stray capacitance, the maximum output voltage with this device is 50 mV for 1×10^{-7} coulombs/cm^2 in the phase-two and phase-four wells.

V. SHIFT REGISTER EVALUATION

Study of the CCD structures has emphasized CTE determination by evalutaion of shift registers at 77K and with 50 KHz four-phase clocks using a tunnel (or avalanche) input. The first results obtained were 0.996 for an 8-stage shift register.[1] Many 16-stage shift registers have been evaluated with CTE results in this range. In many cases, these values were limited by the operation of the injection floating gate rather than the charge transfer efficiency of the shift register. The basic problem is injection-feedback: part of the charge injected into the substrate can diffuse back to the last stages of the shift register and be delivered a second time to the floating gate. Figure 12 shows the floating gate output when the charge is clocked out to an electrode more remote from the last stage of the shift register rather than being injected at the floating gate. A CTE of 0.9995 was obtained at 77K for 50 KHz clocks. The magnitude of the signal output is in agreement with theory for the measured 40 pF stray capacitance and the 4-volt voltages (beyond theshold) used on the phase-four and phase-two clocks. Similar CTE improvement could be obtained by providing a drift field in the substrate.

Figure 13 shows the result of Zerbst analysis[18,19] of a test capacitor (area= 6.45×10^{-4} cm^2) on the same CCD test bar used in the CTE test shown in Figure 12. The pulsed capacitance decay in this MIS lasted for over 80 seconds (this long storage time is consistent with predictions for 4.4 μm HgCdTe with the doping concentration observed - 1.5×10^{15}/cm^3). The initial decay (large C_F/C -1) shows a variable slope probably associated with a varying surface generation current.[19] According to Zerbst analysis, the linear region in this plot is dominated by depletion layer generation current with a constant surface generation rate. A least squares fit to the linear portion of the data yielded an effective generation lifetime of 6.8 μsec and a surface recombination of 1.30 cm/sec with a 0.993 correlation coefficient for the fit. Minority carrier lifetimes for the n-type bulk of 10-20 μsec have been measured for 5 μm

HgCdTe. A lifetime of 10 μsec yields a minority carrier diffusion length of 45 μm compared to the 30.5 μm distance from the floating gate well to the phase-two well which is on during injection.

Other CCD test bars had Zerbst generation lifetimes as short as 1.8 μsec. Figure 14 shows the results of CTE testing on one such 16-stage CCD which had CTE > 0.999 when operated in the standard floating gate detection mode using injection. Fat zero was provided by background radiation from an 11° field of view. The magnitude of the signal output is consistent with theory for the measured 12 pF parasitic capacitance for the clock voltages which were 5 volts beyond threshold.

In all the tests on HgCdTe CCD shift registers, some fat zero was supplied by dark current generation in the phase wells, infrared generation of carriers, or by fat zero intentionally supplied by a second 0.2 μsec-wide input pulse which occurred every clock cycle. n those cases where dark current contributions were reduced, a fat zero of less than 10% full well was sufficient to eliminate most leading edge fixed loss. The amount of fat zero (of any origin) required for best CTE varied from device to device.

Initial results from the tests on the 32-stage shift register described in Section IV are shown in Figure 15. A CTE of 0.997 was measured at 77K for 50 KHz clocks. A fat zero input pulse was required to obtain this result, and this input reduced the voltage output from 400 mV to 200 mV (gain X100). Due to excess dark current from 4-5 stages (seen in freeze clock measurements), the phase-two and phase-four gates were biased to only 2 volts beyond threshold. The small value of output is due to the excess dark current and fat zero. These results are encouraging in that these results are for the first 32-stage CCD tested in our laboratories.

VI. DARK CURRENT MEASUREMENTS

The standard shift register measurements described in the previous section provided only indirect knowledge about the magnitude of dark current and no knowledge on the origin of dark current from the various stages of the shift register. The freeze clock technique described in Section IV provides this knowledge. Defective opera-

tion of CCD shift registers could be explained by the freeze clock results which could show blockage due to inoperative phases or dark current spikes due to bad stages in the center of the CCD.

Figure 16a and 16b show freeze clock measurements on a transparent gate 16-stage CCD with no infrared radiation incident on the device (a cold cap on the device flat pack). During the 1 msec freeze only the phase-four wells were on and collecting dark current. The photographs show a readout of the dark current from the 16 stages of the CCD followed by a normal shift register output due to signal introduced at the far end of the shift register after the clocks opertion begins again after the freeze. Figure 16b shows a significant increase in dark current when the field plate is biased to be more heavily accumulated. These results suggest that this dark current is associated with the edge of the channel. One possible explanation under study for this excess current is tunnel or avalanche current at the field plate edge (enhancement of the electric field at the MIS well edge).

VII. INFRARED MEASUREMENTS

The major aims of the infrared portion of this study have been to (1) establish the infrared quantum efficiency for the CCD stages and the uniformity of this parameter and (2) demonstrate responsivity and detectivity gain due to the integration of signal and background irradiance as the potential wells transverse the stages of the CCD.

Quantum efficiency for infrared detection was studied using (1) the CCD output and (2) the conductance of MIS test capacitors on the test bar. The signal voltage at the output of the CCD in continuous clock operation is

$$(12) \quad V_S \cong \frac{q}{1.8 \, C_p} \, \eta \phi_S A_D N \Delta t_D$$

where C_p is the stray capacitance, η the quantum efficiency, ϕ_S the signal photons/cm^2/sec, A_D the detector area (the infrared active portion of each stage), N the number of stages, and Δt_D is the inverse of the clock frequency.

In the freeze clock mode of operation, the clocking of the potential wells is

stopped for a freeze period Δt_{FZ} with only one phase on and then clocking is resumed and all bits clocked out. This is a differential measurement in that all bits clocked out have experienced the infrared irradiance for at least $N\Delta t_D$ seconds, but the frozen data bits have in addition, experienced Δt_{FZ} seconds of irradiance. Thus, the differential signal voltage in the freeze clock measurement is

$$(13) \quad \Delta V_S \cong \frac{q}{1.8\ C_p}\ \eta \phi_S A_D \Delta t_{FZ}$$

Figure 17(a) shows freeze-clock-mode output for CCD 13AT8NR at 77K using 50 KHz clocks, phase-two and phase-four clock voltages -5 volts beyond threshold, a stray capacitance of 20 pF, and a gain of 100. The infrared irradiation is due to a 20° field of view for ambient 300K radiation. The first output (negative) to occur is that due to a 1.8 msec freeze with the phase-four wells on with consequent integration of the carriers generated by ambient radiation. Shortly after clocking is resumed after freeze, a tunnel (avalanche) signal is fed in from the input end of the CCD and the standard CCD shift register output (negative) is shown for four bits (not saturated).

Figure 17(b) shows the same type of data for a 4.0 msec freeze and with the shift register input voltage increased. Now both the freeze clock and the shift register outputs are saturated (full well). Comparison of Figures 17(a) and 17(b) show that the slight decrease in freeze clock output seen for freeze clock output bits 9, 10, and 11 disappear upon saturation. This phenomenon is due to the shadow of a gold bonding wire which passes above the CCD. The initial signal bits (1, 2, and 3) have larger outputs in both Figure 17(a) and 17(b) and are not due to a variation in quantum efficiency, but arise from preamp recovery after a large false signal during freeze. The variation in unsaturated output signal is considerably less than 10% for all uniformly irradiated true data bits indicating very little variation in quantum efficiency among the CCD stages. The average quantum efficiency derived from equation-13 is 46%. Similar measurements were made with smaller field-of-view and a 500K blockbody source and also with a 0°FOV using a GaAs near-infrared diode emitter.

The deviation of quantum efficiency from the CCD measurements requires the accurate knowledge of the stray capacitance at the measurement node. In a second measurement, a quantum efficiency of 48% was derived from analysis of the low frequency conductance of a large test capacitor on the same bar with 13AT8NR in a 20° field of view.

Spectral response was measured using the photoresponse of the test capacitor biased to near the minimum in the low frequency capacitance-voltage characteristic. Most test bars had long wavelength cutoffs (one-half-response wavelength) in the range 4.3 - 4.7 μm. One test bar (9A20) having a 16-stage CCD with 0.997 CTE had a long wavelength cutoff of 5.0 μm.

Signal integration as the potential wells are clocked along the 16-stages of the CCD is demonstrated by Figure 18 which shows the response of CCD 12AT3 (50 KHz clocks) to GaAs diode emitter pulse of 520 μsec duration. During the first 320 μsec of the non-infrared pulse, the CCD output increases in steps as the data bits experience one through sixteen clock periods of infrared illumination. During the next 200 μsec, all output bits experience sixteen clock periods of illumination. At the end of the illumination, there is a period of 320 μsec in which bits illuminated for sixteen to one periods of illumination are clocked out. The uniformity in the magnitude of the voltage steps between data bits is evidence for excellent uniformity in quantum efficiency.

Signal-to-noise in an infrared detector is characterized by its detectivity or D^* for blackbody irradiance (or monochromatic irradiance) in the presence of ambient irradiance. The experimental blackbody detectivity is derived by

$$(14) \quad D^*_{BB} = \frac{1}{H_S}\ \frac{V_S}{V_N}\ \left(\frac{B}{A_D}\right)^{1/2}$$

where H_S is the total signal irradiance (watts/cm^2) on the detector, V_S is the signal output voltage, V_N is the noise output voltage in frequency bandwidth B, and A_D is the detector/stage area. The theoretical conversion from D^*_{BB} is wavelength and temperature dependent and is x13 for a 4.3 μm cutoff and a 500K blackbody source.

Detectivity at 77K was measured for

several CCDs using a chopped 500 K blackbody source. The 500K source was chopped at a low frequency (100 Hz) to obtain good waveform reproduction using 50 KHz clocks for the CCD (see Figure 18). In these measurements, the stray capacitance was 15 pF and the 500K signal flux was 1.2×10^{-6} watts/cm^2 on the CCD. For a 20° field of view, the derived $D^*_{\lambda_p}$ was 2.8×10^{12} cm Hz$^{1/2}$/watt for CCD 13AT8NR which had a 4.3 µm long wavelength cutoff.

A theoretical maximum value for $D^*_{\lambda_p}$ can be obtained for infrared background limited performance by using equation (12) for signal and equation (15) for the narrow band uncorrelated noise $\langle V_f^2 \rangle^{1/2}$ for B = 1 from a time-delay-and-integrate detector integrating for $N \Delta t_D$ seconds and read out every Δt_D seconds.

$$(15) \quad \left\langle V_f^2 \right\rangle^{1/2} = \frac{q}{1.8 C_p} \quad \Delta t_D \sqrt{2 \eta \phi_{BG} A_D N}$$

where ϕ_{BG} is the ambient irradiance on the detecor due to the field-of-view. The theoretical value for $D^*_{\lambda_p}$ is

$$(16) \quad D^*_{\lambda_p} = \frac{\lambda}{hc} \left(\frac{N \eta}{2 \phi_{BG}} \right)^{1/2}$$

For 4.3 µm long wavelength cutoff, a 300°K ambient seen through a 20° field-of-view and a 46% quantum efficiency the theoretical value of $D^*_{\lambda_p}$ is 4.0×10^{12} cm Hz$^{1/2}$/watt.

The experimental value of $D^*_{\lambda_p}$ is 70% of the theoretical value. This discrepancy is due to the aliased white noise of the first stage amplifier [20] which consists of a cooled JFET operated as a source follower. The degree of aliasing was attenuated by use of a 1 µsec RC filter between the low noise post amplifier (gain X12) and the 50 KHz sampling circuit. The total amplifier noise referred to the input node was 30 nV/(Hz)$^{1/2}$ under the above test conditions. The total detector plus amplifier noise in the D* tests was 50 nV/(Hz)$^{1/2}$ referred to the input. Therefore, within experimental error, the amplifier noise which is dominated by the aliased buffer noise limits the present results on D*. The detector noise results were measured for a background which gave only 10% full well charge. Experimental detectivities closer to theory should result from the use of larger field of views and/or decreased white noise of the buffer amplifier.

VIII. POTENTIAL FOR 8-12 µm APPLICATIONS

As previously discussed, $Hg_{1-x}Cd_xTe$ alloys can be used to fabricate infrared detectors for 8-12 µm window. Both photoconductive and photovoltaic detectors have been demonstrated. The application of CCD (or CID) technology to HgCdTe with 12µm cutoff to imagers using large background field of view is a challenging task. Application of HgCdTe with 10 µm cutoff is more promising. The problem is two-fold: (1) the smaller bandgap of this material causes tunneling to occur at lower electric fields and (2) the 8-12 µm wavelength band contains considerably more radiation to be stored than does the 3-5 µm band. On the other hand, a much shorter integration time is needed to obtain 0.1° NEΔT.

Analyses for the same system parameters as used in Section II yield a requirement for 84 µsec integration time for 8-10 µm HgCdTe thus requiring only 4 TDI stages of 20 µsec each for 0.1°C NEΔT. The 60 dB dynamic range requirement plus the larger background requirement for the 8-10 µm band will require the storage of 1.6×10^{-7} Coulombs/cm^2-of-pixel-area for 4 TDI's and require a dark current density of less than 130 µa/cm^2-of-pixel-area. Actually, an 8-10 µm system would need to be cold shielded more efficiently than the above example potentially cancelling the bit-area/well-area ratio requirement of Section II. Furthermore, the above calaculation of NEΔT was based on identical atmospheric transmission for the 3-5 µm and 8-10 µm bands which improperly penalizes the 8-10 µm band. A precise comparison would depend on the atmospheric model utilized and thus is beyond the scope of this paper.

The requirement that the total tunnel current be less than 10% of the background current is shown for several wavelength bands in Figure 19. A ZnS insulator thickness of 1000Å has been assumed as a projection of present technology. It can be seen that 8-10 µm application will require HgCdTe material with carrier concentration less than 2×10^{14}/cm^3. Material with this carrier concentration is feasible.

Unlike the case shown for 5 µm material at 77K in Figure 5, both minority carrier diffusion and depletion layer currents can make significant contributions to the total dark current of a 10 µm MIS device

biased near the tunnel limit for $2\times10^{14}/cm^3$ material (about 0.95 volts/μm electric field.) Both mechanisms can give dark current contributions in the range of 30-60 μamps/cm². Both these contributions for 10 μm HgCdTe could be eliminated by reducing the focal plane temperature to a temperature similar to that proposed for 3-5 μm-response extrinsic silicon detectors.

The application of MIS technology to 8-10 μm applications appears feasible provided top quality material with carrier concentration in the $2\times10^{14}/cm^3$ range and depletion generation lifetime greater than 10 μsec is utilized. The importance of this application suggests that these challenges will be overcome.

IX. CONCLUSIONS

Excellent progress has been obtained on 3-5 μm wavelength HgCdTe CCDs operating at 77K. Charge transfer efficiency adequate for most anticipated applications has been demonstrated. Infrared detection with time-delay-and-integration enhancement of responsivity and detectivity has been demonstrated. Both 16-stage and 32-stage CCD shift registers have been tested at the 50 KHz clock frequencies required for time-delay-and-integration in an infrared imager with a 1/60 sec mechanical scan. Future studies will include multiplexer evaluation at higher frequencies and time-delay-and-integrate demonstration with mechanically scanned imagers.

Sufficient charge storage for the 8-10 μm wavelength band is within the range of possible design parameters and will necessitate the use of the highest quality material and innovative device design.

The device technology utilized for Hg CdTe CCDs has potential for application to other charge transfer device designs such as CIDs. Implementation of a large number (20-30) TDI stages is much more straightforward using CCD designs. The implementation of a few TDI stages for applications with storage time limitations could be performed with HgCdTe CIDs combined with silicon signal processing CCDs. Staring arrays could be implemented with either HgCdTe CCDs or CIDs depending on the application requirements.

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Figure 2. Modulation transfer function in the direction of transfer (shift register with 25.4 μm stage length.)

FIGURES

Figure 1. A generalized type of area CCD imager. When used as a TDI array, the infrared image is scanned from top to bottom of the figure.
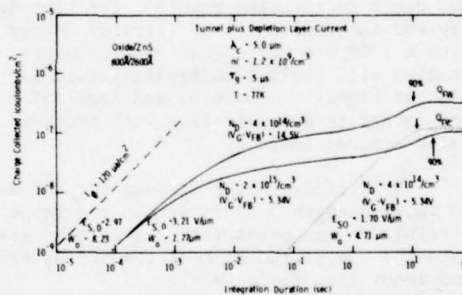
Figure 3. Charge collected versus time in an MIS showing that depletion layer current dominates storage time in 5 μm HgCdTe at 77K. Tunnel current is the dominant dark current for the <1 msec integration times anticipated.
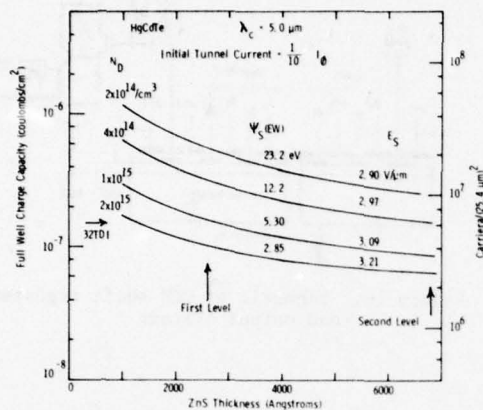
Figure 4. Predicted full well charge capacity as a function of ZnS insulator thickness with carrier concentration as a parameter. HgCdTe long-wavelength cutoff is 5 μm.

Figure 6. Theoretical CTE vs Frequency for p-channel 0.25 eV HgCdTe

Figure 5. Predicted gate voltage to obtain the full well capacities of Figure 4.
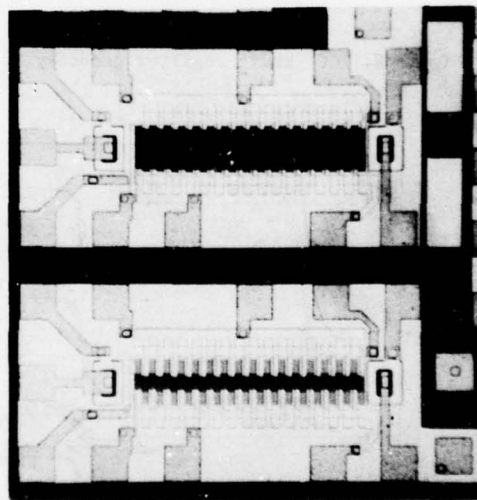
Figure 7. Two 16-stage HgCdTe CCD shift registers with transparent electrodes.

(a) CCD Longitudinal Section

(b) CCD Cross Section
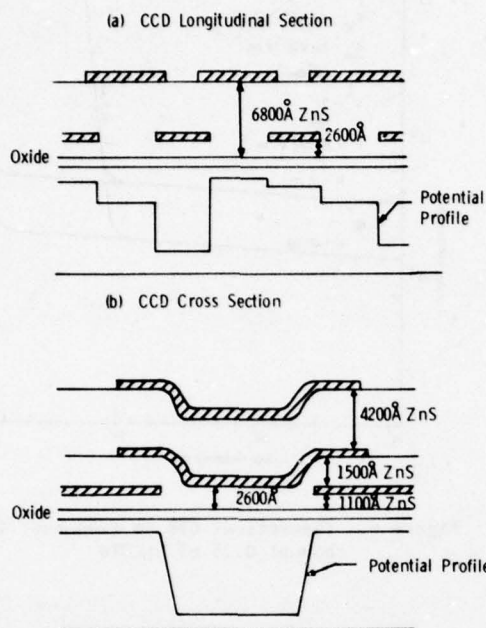
Figure 8. CCD shift register geometry (one type)
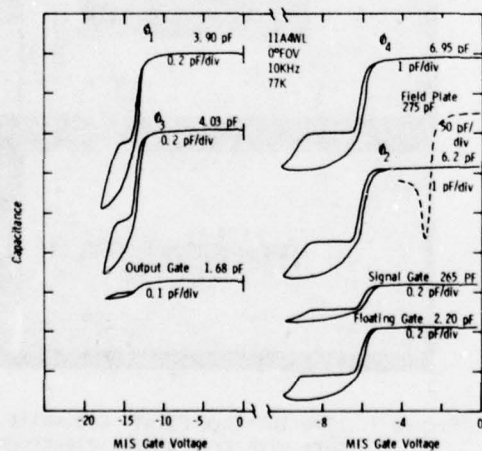
Figure 9. Capacitance-voltage characteristics for 16-stage CCD 11A4WL
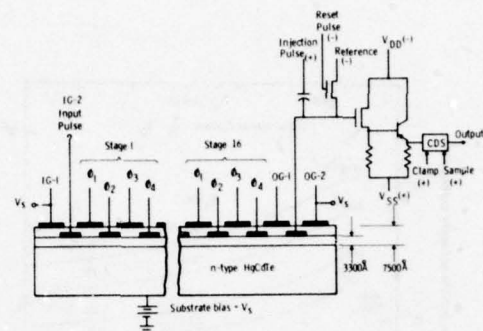
Figure 10. Schmatic of CCD shift register and output circuit
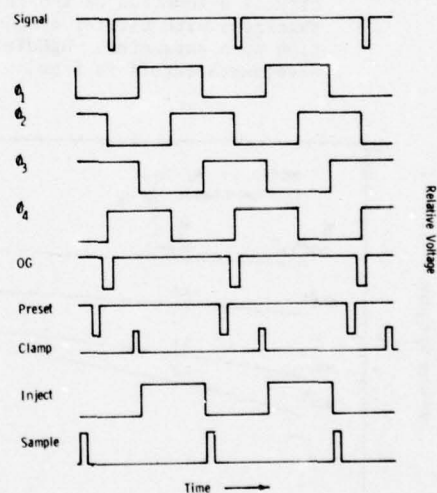
Figure 11. Clock sequence for 16-stage shift register
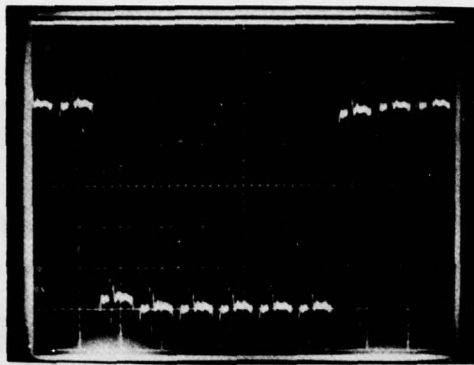
Figure 12. Output for 16-stage CCD 11A4WL showing CTE = 0.9995. Vertical 20mV/div. Horizontal 20 μs/div. Gain X70. Stray capacitance = 40pF
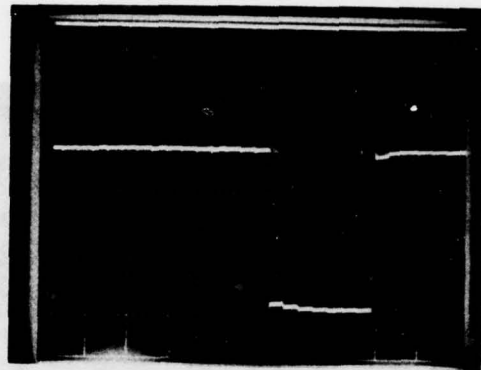
Figure 14. Output for 16-stage CCD 12AT3W. Upper: input at 5 volts/div. Lower: output at 0.5V/div. Both 50 μs/div. 77K temperature and 11° FOV. Stray capacitance = 12 pF.
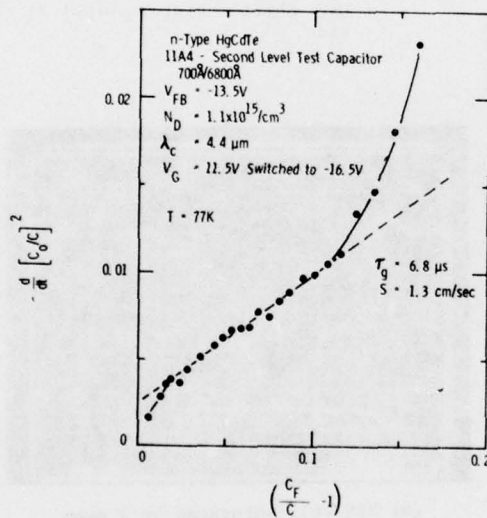
Figure 13. Zerbst plot for second level test capacitor on bar with 11A4WL. Indicated generation lifetime is 6.8μsec and surface generation rate is 1.3 cm/sec.
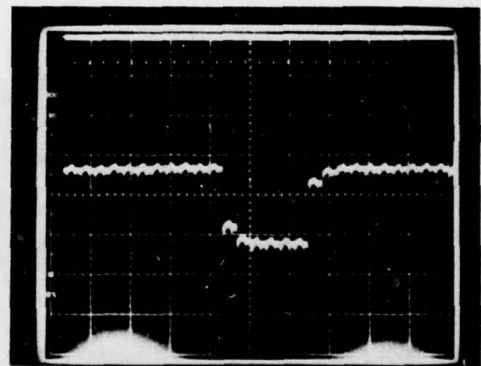
Figure 15. Output from a 32-stage CCD (15AT2) 100 mV/div and 50 μs/div. CTE = 0.997.
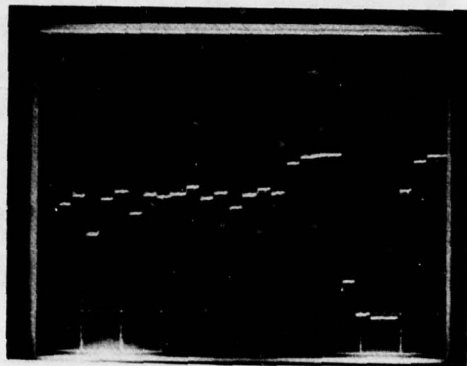
Figure 16. (a) Dark current collected after 1 msec freeze (field plate gate 1.1 volts in accumulation) for 16-stage. CCD-13AT8NR. 500 mV/div and 50 μs/div.
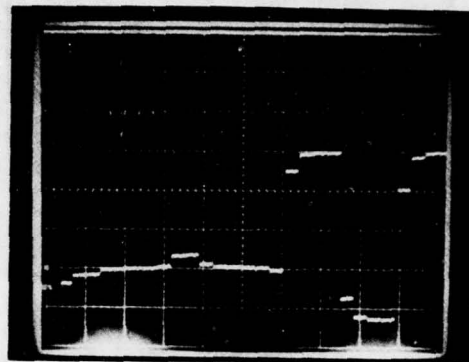
Figure 17. (a) 1.8 msec freeze clock with 20° FOV infrared background for 16-stage CCD-13AT8NR. 500 mV/div and 50 μs/div. Shadow of gold wire is on bits 9 & 10. Shift register output at right side.
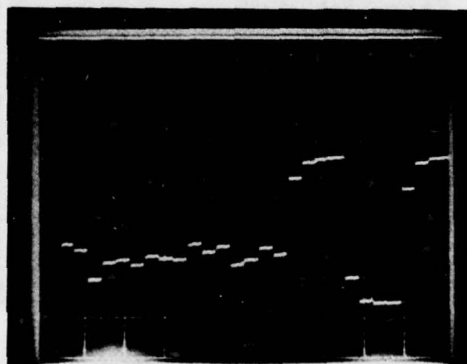
(b) Dark current for field plate gate 1.8 volts in accumulation.
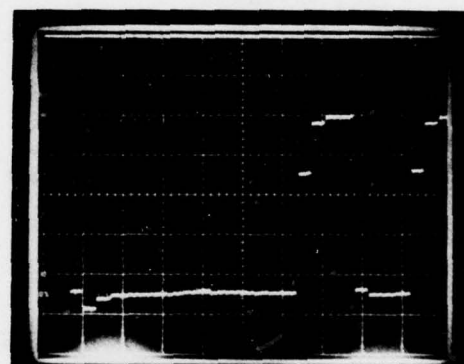
(b) MIS well saturated by 4 msec freeze and increased shift register input.
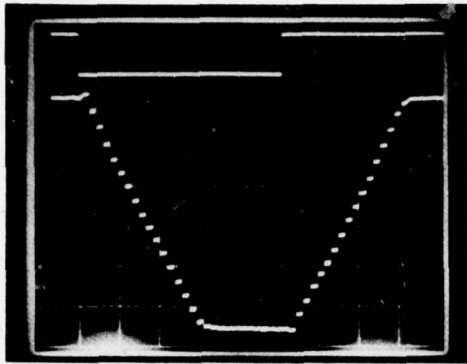
Figure 18. Time-delay-and-integrate operation
demonstrated for 16-stage CCD-12AT3
with 50 KHz clocks using a GaAs near-
IR diode emitter.
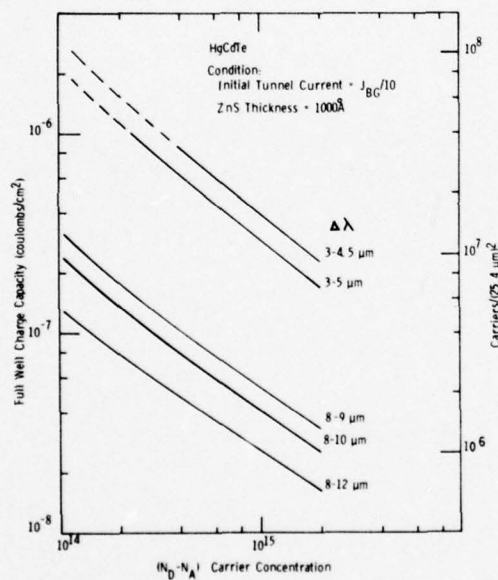
Figure 19. Full well charge predicted for var-
ious wavelength bands as a function
of carrier concentration.

2-17

A NEAR IR PIN/CCD DETECTOR ARRAY

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ABSTRACT. A PIN diode array to detect near IR radiation has been designed, fabricated and tested. The array uses a charge transfer device signal readout mechanism and is optimized for the 0.7 to 1.0 μm band. The array consists of 160 detectors. Data is presented in this paper on the design considerations and test results. Quantum efficiencies of better than 80 percent have been measured with antireflection coated devices. Measured crosstalk between detector elements on 1.65 mil centers was 4 percent and detector response was uniform within 10 percent. The device operated nominally at a 20 kHz frame rate with detector integration times variable from 0.5 to 50 μs. All measurements in this paper were performed at a temperature of 300°K.

I. INTRODUCTION

The need for high responsivity detectors in the near IR region of the spectrum has recently led to increased interest in intrinsic (ρ = 1000 to 20,000 ohm cm) silicon deep depletion devices. In particular, several 1.06 μm wavelength laser target designator systems are now utilizing silicon PIN detectors. Although the number of such applications have increased dramatically in the past two years, all the devices fabricated to date have been relatively simple structures, typically one to four PIN detectors per chip. The coupling of PIN detectors with a CCD type readout offers several advantages such as multiple detectors per chip, denser, higher resolution detector arrays, multiplexed readout structures and on chip signal processing. Our efforts have concentrated on developing a novel multi-detector staring array with CCD readout for application in the 0.7 to 1.0 μm wavelength region.

II. DESIGN CONSIDERATIONS

For most imaging applications, high resolution is desirable over the entire field of view, however, this leads in many cases to high bandwidth requirements. In

Table 1

Multi-Element Detector Chip Design Goals	
Spectral Region	0.7 to 1.0 μm
Responsivity	>0.4 amps/watt
Crosstalk	<10 percent
Cell Size	1.65 mils at center
Dynamic Range	$\geq 10^5$
BLOOM Protection	100X maximum signal
Individual Cell Sample Rate	20 kHz
Noise	<1 μV/$\sqrt{Hz}$
Total Array Diameter	148 mils

addition to the bandwidth considerations, for a staring detector array using charge integration devices the frame time also becomes important from a dynamic range standpoint. Higher frame rates (>30 Hz) are desired for higher dynamic range, but

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this increases the bandwidth required. For many imaging and tracking applications, high resolution is important only in the center of the field of view, thus the array design utilized high density, high resolution detector elements in the center and increasing larger, lower resolution detectors in the periphery. To allow good dynamic range, a frame rate of 20 kHz was chosen, while the bandwidth was kept very low (160 kHz) by using few number of detectors (160) and multiple readout lines (20). These parameters were chosen to be conservative due to the higher risk believed to be involved in the center unit cell layout. From design rule considerations this center array of high resolution detectors had a unit cell size of 1.65 x 1.65 mil.

This square array is surrounded by 6 annular rings which increase in size from the center to the periphery where high resolution is not required. Each ring contains 16 cells. The total of 160 cells are multiplexed onto 20 output busses, each buss having a separate output amplifier. The output buffers are located around the periphery of the chip. The use of 20 output amplifiers allows parallel off chip signal processing and consequently reduces the data rate of each line by a factor of 20. The total chip size is 198 x 198 mils which includes a large number of test devices in the 4 corners of the die as well as the 148 mil diameter main array.

Meeting the goals of high responsivity and low crosstalk for small cell size detectors is particularly difficult for the spectral region of interest (0.7 to 1.0 μm). This fact can best be appreciated by referring to Figure 1 which plots the normalized photon intensity versus penetration depth into a silicon detector for several wavelengths in the visible and near IR regions of the spectrum. At $\lambda = 0.9$ μm the photons penetrate deep into the substrate before being absorbed; e.g., 10 percent of the incident photons remain unabsorbed at a depth of 35 μm, 6 percent are unabsorbed at 45 μm. In order to maximize responsivity and minimize crosstalk, it is desirable to have the majority of the photons absorbed in the depletion region. Hence, the photon generated electron-hole pairs are immediately separated by the electric field and the appropriate carrier is collected to the detector. Photons penetrating
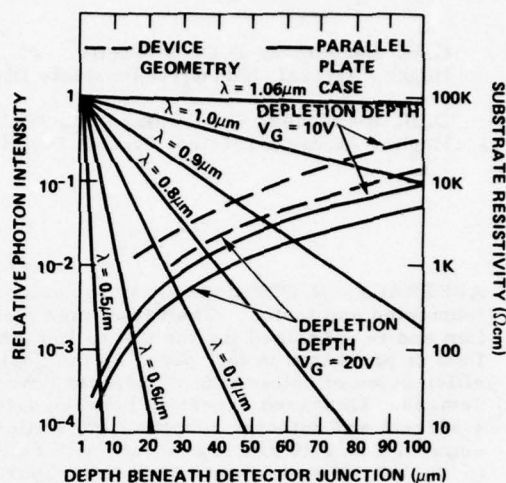
Figure 1. Decay at relative photon intensity for several wavelengths as a function of penetration depth into a silicon detector and depletion depth for voltages of 10 and 20 V as a function of substrate resistivity

deeper than the depletion volume create carriers in a field free region. Such carriers are free to migrate laterally which causes crosstalk. Furthermore, the recombination probability is much higher for carriers created in a nondepleted region which can result in a reduction in responsivity. Hence, meeting the crosstalk goal (10 percent) requires a depletion depth on the order of 30 to 50 μm. The depletion depths attainable for two MOS compatible voltages as a function of substrate resistivity are superimposed over the absorption curves in Figure 1. The solid lines in Figure 1 indicate the depletion depth versus bias of a one dimensional (parallel plate) detector geometry. For the actual geometries used in the device described in this paper, the depletion voltages are substantially higher as shown by the dashed lines in Figure 1, which represent the results of a two dimensional model of the device. Thus the geometry considerations further increase the demands on detector resistivity and for this device a goal of 8000 Ω-cm, which allows full depletion through a 50 μm material with a 10 volt bias, was chosen.

The design approach used to meet the goals of Table 1 utilizes a deep depletion, thinned, backside illuminated structure fabricated on a p-type high resistivity substrate. The backside illumination scheme allows 100 percent of the detector array's area to be optically active. The appearance of the completed array is shown in Figure 2.

The electrical equivalent circuit is shown in Figure 3. Each unit cell contains a PIN detector, a readout transfer gate and diffusion, and a bucket overload gate and drain. The Bucket Overload Protection (BOP) circuitry is required to prevent bloom at high illumination levels. Also the BOP can be used to vary the integration time of the detector pulsing the BOP gate. As illustrated in Figure 3, eight detectors are multiplexed onto a floating diffusion output buss which is connected to the input gate of a two stage N-MOS source follower amplifier.

Figure 3. Electrical equivalent circuit of *one line of 8 detector elements*

Figure 2. Photograph of a die containing the monolithic PIN/CCD array

III. DEVICE OPERATION

The device operates as follows. The floating n$^+$ anode of the PIN detector is set to a potential of approximately 15 volts which is sufficient to deplete the entire substrate thickness. Photon generated hole electron pairs are separated by the depletion field and the electrons are collected to the diffusion and are stored in an inversion layer under the bias gate. As the storage "bucket" fills with charge the potential on the floating diffusion decreases. Thus it is important that the initial voltage be high enough such that the substrate remains depleted under full well condition. If this is not the case, crosstalk will result. The stored charge packet is transferred from the storage gate to the

output node by addressing the proper transfer gate. The transfer of the negative charge packet to the floating output node causes the potential of the node to fall and the output amplifier responds. After the transfer gate is turned off and the output settles, the output node is reset to 20 volts by the MOS switch. Since 8 detectors are multiplexed onto one output bus, eight transfer gate clocks are required along with a reset clock and a sample and hold clock. The sample and hold transistor in the output amplifier is used to give a cleaner and longer response. The bucket overload gates perform a dual function. In addition to bloom protection, the gates can be clocked to vary the cell integration period which increases the dynamic range under strong signal conditions.

IV. EXPERIMENTAL SET UP

Characterization of array operation concentrated on the following parameters which were used to form a data base for analyzing the array operation:

1. Uniformity
2. Crosstalk
3. Responsivity
4. Frequency Response
5. Dynamic Range
6. Noise
7. Bucket Overload Protection
8. Detector Integration Time Variation
9. Array Transfer Properties

Testing of the detector array was performed on an optical bench. A modulated LED source was used that emitted in the wavelength range of 0.6 to 1 μm with a maximum at 0.9 μm. Modulation of the light was accomplished by means of a variable speed chopper which gave a modulation range of 50 Hz to 10 kHz. In front of the chopper a variable size aperture was used to vary the optical intensity and to decrease the spot size to less than 25 μm. To focus the source onto the detector array, a Nikor f/5, 63 mm lens was used. The chip was mounted on a motor controlled x-y translation table which permitted movement of the detector array relative to the optical spot. In front of the array, a Shott RG-5 spectral filter with 0.97 percent transmission between 0.7 and 1.2 μm, was used to screen out

possible room light interference. All measurements were performed at room temperature.

Each detector could be individually monitored by choosing an output line with a 20 position output selector switch followed by an 8 channel sample and hold demultiplexer.

To obtain spot scans of the detectors, the array is moved across the focused spot of light and the output response of a single detector is monitored by a wave analyzer which drives the y axis on the x-y recorder. The x axis is the spot position given by a position encoder controlled by the x-y translation table. This is shown schematically in Figure 4. The resultant curve is a plot of a single detector response as a function of spot position on the detector. This scan is repeated for adjacent detectors to display detector response uniformity and crosstalk.
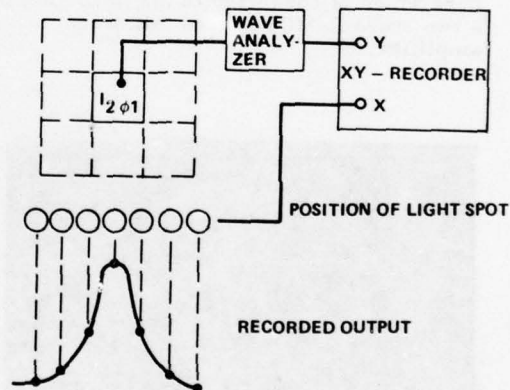
Figure 4. Schematic diagram of spot scan measurements of the PIN/CCD detector array

V. EXPERIMENTAL RESULTS

a. Output Devices

Each of the 20 video output lines had its own on chip output device as discussed previously. This output device was characterized using a separate test device of the exact same configuration. The results of this test are shown in Figure 5 for two values of gate bias on the MOS

source load resistors. Higher positive gate voltages increase the device conductance, reducing the source resistance which decreases gain and increases bandwidth. The gain bandwidth remained constant at about 300 kHz, more than sufficient for operation with 160 kHz video waveforms.
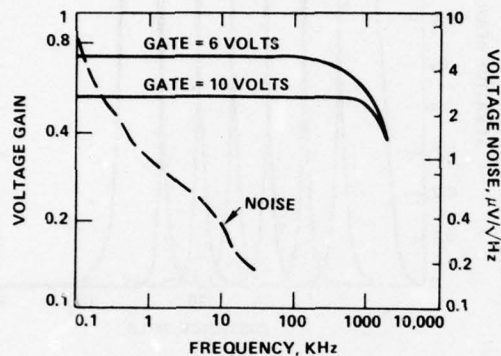
Figure 5. Gain and noise versus frequency of the dual source follower output

b. Detector Measurements

Measurements were made on response as a function of detector bias voltage using a 4 element linear test detector array of the same general configuration as the main array detectors. The test detector array consisted only of the n+ p detector, with no CCD readout. Measurements of these detectors was by means of a transimpedance amplifier. Figure 6 shows the measured detector response and cross talk (measured at the center of the adjacent detector) as a function of bias. Increasing the bias reduced the crosstalk from 8 percent to less than 2 percent for these test detectors, and increased responsivity as the detector base was further depleted. The response as a function of bias saturated above 10 volts at which bias the base was nearly fully depleted. This corresponds with the calculated value of 10V depletion for a 50 μm thick detector with a resistivity of 8000 Ω-cm as was shown in Figure 1.

c. Results of the Main Array

The output waveform of the array is shown in Figure 7. Figure 7a shows the output of one line with the focused spot (modulated at 1 kHz) centered on two adjacent detectors.
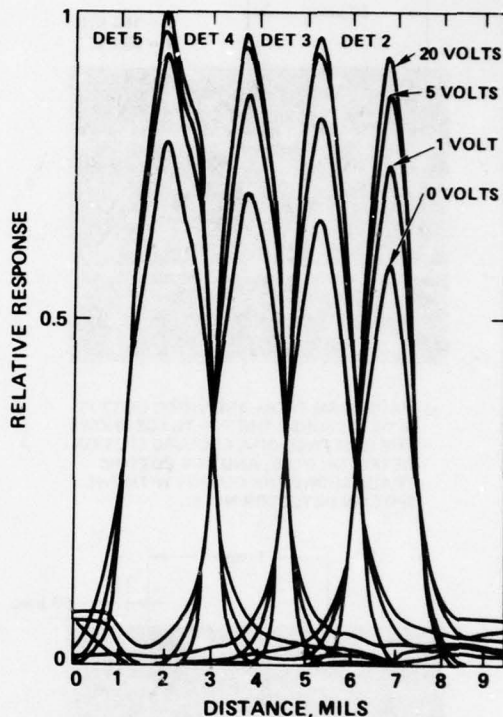
Figure 6. Relative response of test detectors as a function of bias

In each waveform the other 7 detectors are not illuminated. The output was kept valid for 85 percent of a full analog data bit period by a sample and hold circuit included in the on chip two stage source follower output device. Figure 7b shows the demultiplexed output waveform of one illuminated detector. The spread in amplitude of each sample interval is due to the aliasing of the 20 kHz sample rate with the unsynchronized 1 kHz signal.

A vertical spot scan of seven adjacent detectors in the center 8 x 8 portion of the chip is shown in Figure 8. As shown the uniformity is quite good with a standard deviation of 2.8 percent about the mean detector response. The spot scans shown have not been deconvolved to take out the optical blur of the focused signal, thus the spot scans show the total optical and electrical

50 μsec   fc = 160 KHz
T = 300°K

100mV   10μS
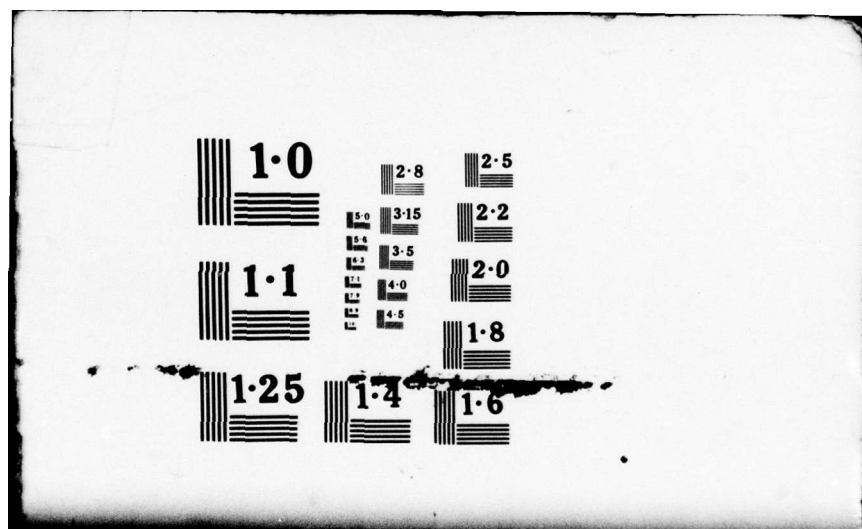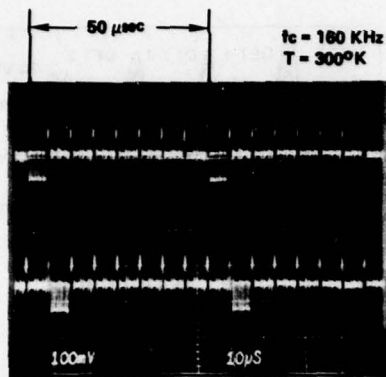
a) WAVEFORM FROM ONE VIDEO OUTPUT (8 DETECTORS). THE TOP TRACE SHOWS THE RESPONSE OF A FOCUSED SPOT ON DETECTOR NO. 5, AND THE BOTTOM TRACE SHOWS THE OUTPUT WITH THE SPOT ON DETECTOR NO. 6.

1 msec   50 μsec

200mV   200μS
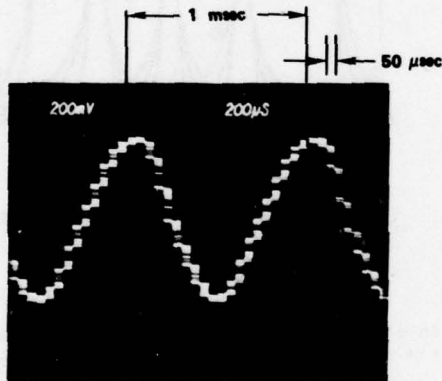
b) DEMULTIPLEXED OUTPUT OF ONE DETECTOR SHOWING A SINGLE DETECTOR RESPONSE TO A SIGNAL MODULATED AT 1 KHz.

Figure 7.   PIN/CCD array output waveforms

crosstalk to be less than 3 percent at the center of the adjacent detectors. Due to an open aluminum addressing line on this die, the eighth detector in the center array was not operational.

The scanned optical response of the ring detectors is shown in Figure 9. The
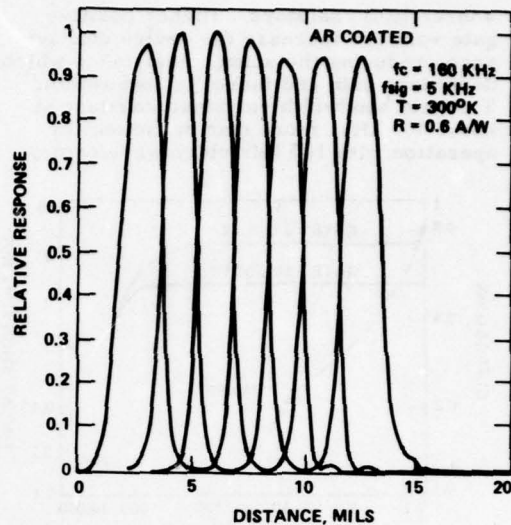
Figure 8.   Vertical spot scan of detectors in the center 8 x 8 detector area

response of each successive ring decreases because the larger input capacitance of the dual source follower on the larger detectors of the outer rings decreased the transimpedance of the output devices. The structure in the responsivity within one detector area is due to the cross section of the ring array detectors. The second ring was not operational.

Figure 10 compares the response of the arrays with two different dopings. The array fabricated on a $8K\Omega$-cm substrate shows an increase in response by a factor of 4 and a decrease of crosstalk (from 15 to 4 percent) over the same array constructed on a $100\ \Omega$-cm substrate. To fully deplete $50\ \mu m$ of a $100\ \Omega$-cm silicon a voltage of 200 volts is needed while only 10 volts is required to deplete the $8000\ \Omega$-cm material. Since 15 volts were applied to both arrays the $100\ \Omega$-cm was not fully depleted resulting in low quantum efficiency and higher crosstalk.

d. BOP Operation

As described in Figure 3, the BOP circuit can be used to vary the integration time of the detector element. The response as a function of integration time is shown in
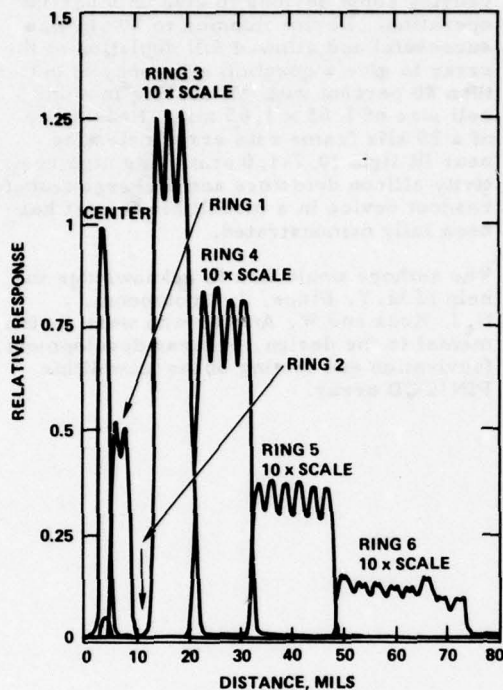
Figure 9. Spot scan response of the ring detectors
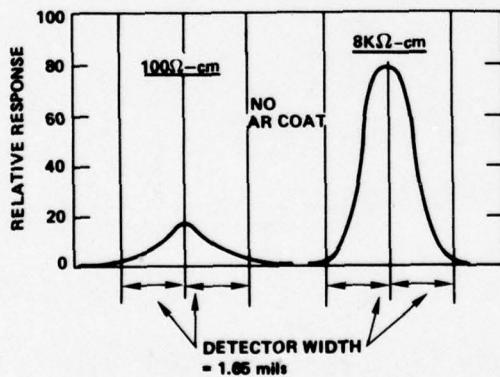
.Figure 10. Spot scan of detectors with two different base dopings

Figure 11, the response is linear over two orders of magnitude integration time variation from 0.5 to 50 μs. This allows a
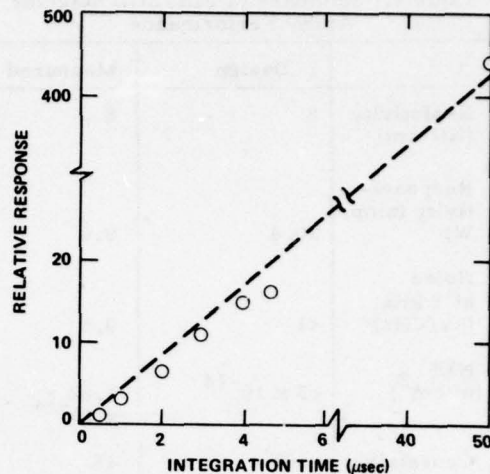
Figure 11. Relative response of detectors as a function of integration time (BOP)

dynamic range increase of a factor of 100 and provides the 10^5 overall dynamic range required in the design goals.

VI. CONCLUSIONS

A summary of the device operation is shown in Table 2 for a 8000 Ω-cm AR coated backside illuminated array and compared with design goals. Responsivity of 0.6 A/W was measured on the PIN/CCD detector elements with a variation of 10 percent. Crosstalk was 4 percent. The output voltage noise at 5 kHz was 600 nv/$\sqrt{Hz}$ which gave a noise equivalent intensity (NEI) of 1.62×10^{-14} w/cm^2 measured on the 8 x 8 center portion of the array. Ring detectors yielded higher values of NEI due to the lower transimpedance as was shown in Figure 9 which caused the noise of the ring detectors to be limited by the on chip output device noise.

In summary, all the design goals of this device were met or exceeded during characterization of the completed PIN/CCD detector arrays. Processing problems initially encountered were solved. Processing with an EPI-MOS process on high resistivity silicon substrates was shown to give good device operation with no degradation in substrate characteristics. Some problem was encountered with aluminum step coverage and soft diode breakdown,

Table 2. Summary of PIN/CCD detector Array Performance

	Design	Measured
Resistivity (KΩ-cm)	8	8
Responsitivity (amp/W)	>0.4	0.6
Noise at 5 kHz (μv/√Hz)	<1	0.6
NEI (w/cm²)	$<3 \times 10^{-14}$	1.62×10^{-14}
Crosstalk	<10%	4%
Uniformity	<15%	10%
Integration time (μsec)	0.5 to 50	0.5 to 50
Amplifier gain	0.7	0.7

causing some devices to give only partial operation. Device thinning to 50 μm was successful and allowed full depletion of the array to give a quantum efficiency of better than 80 percent with AR coating in a unit cell size of 1.65 x 1.65 mil. Feasibility of a 20 kHz frame rate array detecting near IR light (0.7-1.0 μm) using high resistivity silicon detectors and a charge transfer readout device in a monolithic format has been fully demonstrated.

PLATINUM-SILICIDE SCHOTTKY-BARRIER IR-CCD IMAGE SENSORS[*]

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ABSTRACT

We describe the construction, operation and characteristics of two types of monolithic silicon IR-CCD sensors with platinum-silicide (Pt_xSi) Schottky-barrier detectors. They are a 256-element line sensor and a 25x50-element area sensor. These IR-CCD's can be operated from 50 to 90 K, and are sensitive in the 1.2 to 4.6 μm spectral range. A typical value of the quantum-efficiency coefficient (C_1) of the platinum-silicide detectors is 5%/eV. A photoresponse uniformity of 0.55% rms was demonstrated with the 256-element line sensor. Thermal imaging data are reported for both calibrated infrared sources and human subjects. Noise-equivalent temperatures (NET) of 0.4°C and 1.0°C in 26°C ambient, noise-equivalent powers (NEP) of 8×10^{-12} W and 3.36×10^{-11} W, and linear dynamic ranges of 5,000 and 1,800 were demonstrated with the line and the area sensors, respectively, for operation with an integration (staring) time of 30 ms. The dynamic range of these infrared sensors, however, can be extended further by operation in a blooming control (saturation) mode.

I. INTRODUCTION

Schottky-barrier infrared detectors offer the possibility for production of highly uniform, monolithic silicon IR-CCD focal plane arrays. Platinum-silicide (Pt_xSi) Schottky barriers on p-type silicon have a barrier height of about 0.27 eV which corresponds to an infrared-response cutoff wavelength of 4.6 μm [1]. Thermal imaging with platinum-silicide IR-CCD arrays was described by Shepherd [1-3], Kohn, et.al. [4], Taylor et.al. [5], Skolnik, et.al. [6], and Capone et.al. [7]. In this paper we will describe the construction, operation, and infrared characteristics of a 256-element line sensor [5,6,8] and a 25x50-element area sensor [7, 9,10]. These devices were designed and fabricated at RCA Laboratories. The reported infrared measurements were made at RADC/ESE.

II. PLATINUM-SILICIDE SCHOTTKY-BARRIER DETECTORS

The use of Schottky-barrier detectors for infrared imaging has been described extensively in the literature [1-14]. The platinum-silicide (Pt_xSi) detector is formed by depositing a layer of platinum (typically about 600 Å) on a p-type silicon substrate (having resistivity of 10 to 50 Ω-cm) and then sintering it at a temperature in the range of 200 to 650°C. The composition of the Pt_xSi alloy varies with the sintering temperature and time as well as with the initial thickness of the platinum layer [14]. The reaction between the metal and the silicon places the Pt_xSi:Si junction beneath the original surface of silicon, and thus produces diodes free of surface effects and with highly uniform photoresponse. In fact, 1-cm diameter Pt_xSi diodes have been fabricated having rms photoresponse nonuniformities of less than 0.1% [3]. Therefore, the photoresponse uniformity of the platinum-silicide detectors fabricated thus far have

been basically limited by the uniformity of the geometric definition of the detectors. The photoyield, Y, for Schottky emission is given by [2]

$$Y = \frac{C_1 \ (h\nu - \psi_{ms})^2}{h\nu} \ \frac{electrons}{photon} \ , \quad (1)$$

where ψ_{ms} is the barrier height, h Planck's constant, ν the photon frequency and C_1 a factor determined by the geometrical, optical and transport properties of the silicide contact. With $h\nu$ and ψ_{ms} expressed in eV, C_1 is in reciprocal eV. An example of a photoyield curve for a 600 Å Pt/p-Si diode reacted at 320°C is shown in Fig. 1, where we plot $\sqrt{Yh\nu}$ vs $h\nu$. From the graph we find a barrier height of 0.268 eV and a C_1 of 3.6% eV. A
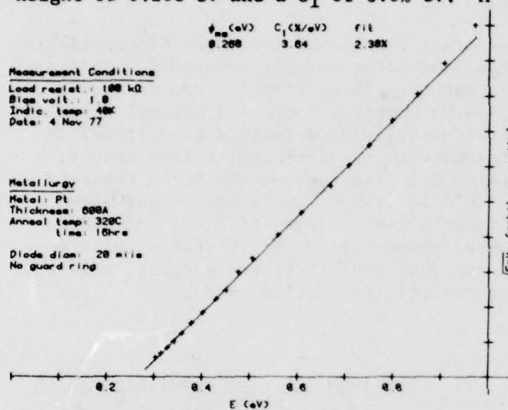
Fig. 1. Photoyield versus energy for 600 Å PtSi diode.

typical value of C_1 for Pt_xSi detectors is 5%/eV. It should be noted, however, that the form of the yield curve (Fig. 1) and the values of C_1 ($3 \leq C_1 \leq 11\%$/eV) are highly dependent on reaction conditions and initial Pt layer thickness. Effects such as electron-phonon mean-free-paths and enhanced thin-film reflections can influence the energy dependence of the photoresponse [12,13]. The effective quantum efficiency for thermal imaging of platinum-silicide Schottky-barrier detectors is rather small, i.e., on the order of 0.1%. However, the demonstrated high uniformity of photoresponse (0.5% rms and better) [3-7] combined with low-noise readout by buried-channel CCD's made the Schottky-barrier IR-CCDs attractive alternatives for many thermal imaging applications. The rather low quantum yield in Schottky detectors

can be made up by operating the arrays either in the staring or time-delay-integration mode. Calculations [3] based on present estimates indicate that these devices with 6.25×10^{-5} cm^2 (1 mil^2) detectors should be capable of resolving 0.1°C targets against a 300 K background at standard video frame rates.

III. DEVICE CONSTRUCTION AND OPERATION

A. Technology

The devices were processed using two-level polysilicon buried-channel CCD technology with p^+ channel stops and n^+ diffusions not self-aligned to the polysilicon gates. The substrates used were 20 to 50 Ω-cm, boron-doped, p-type [100] silicon wafers polished on both sides to a final thickness of 10 mils (250 μm). The platinum-silicide detectors were formed by depositing a 500 to 600 Å film of platinum on the Schottky contact holes opened in the oxide (SiO_2) and then sintering at temperatures in the range from 320 to 650°C. After the platinum silicide formation, the remaining platinum was etched off and a 14,000 Å aluminum metalization was deposited and defined to complete the device processing. The platinum-silicide detectors were formed surrounded by implanted n-type guard rings to reduce the excess dark (leakage) current. This was accomplished using the buried-channel implant, typically in the form of phosphorus with a dose of 1 to 2×10^{12} cm^{-2} at 180 KeV.

B. 256-Element IR-CCD Line Sensor

A block diagram of the 256-element IR-CCD line sensor is shown in Fig. 2. A more
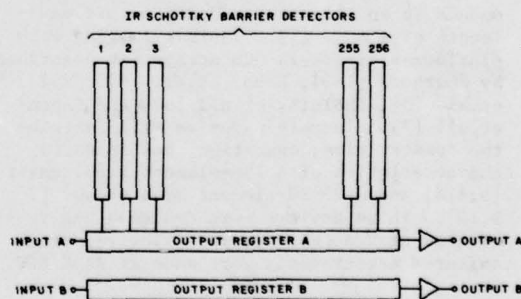
Fig. 2. Block diagram of 256-element IR-CCD line sensor.

Pt - Si SCHOTTKY BARRIER IR SENSORS
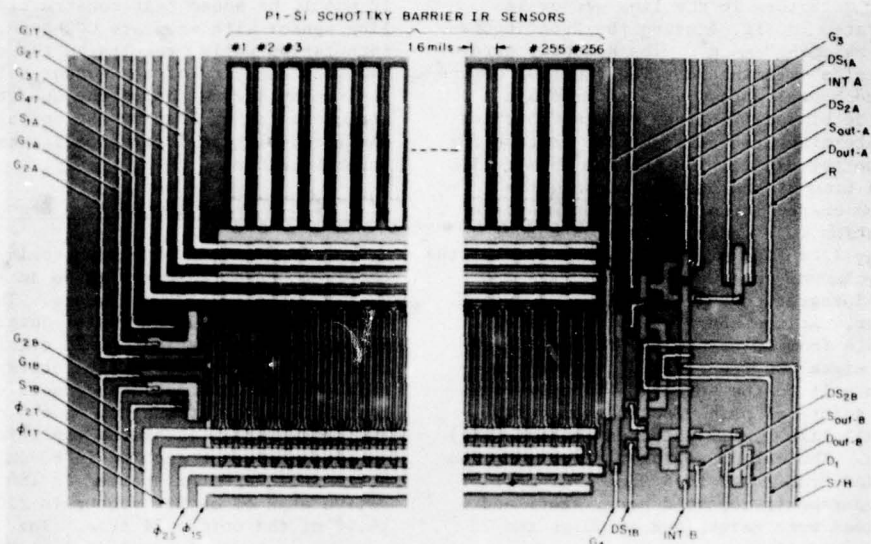
Fig. 3. Photomicrograph of the input and output sections of the 256-element IR-CCD line sensor.

detailed layout of this device is illustrated in Fig. 3, which shows the input and the output sections of the device. The cross-sectional view of the charge-coupling structrue between the platinum silicide detectors and the CCD Output Register A is shown in Fig. 4. The platinum-silicide detectors are surrounded by implanted n-type guard rings and are isolated from each other by 5 μm-wide, p+ channel stops. The effective size of the detectors is 10 μm x 200 μm, and the detectors are spaced on 40 μm centers. The line-sensor chip is 11.3 mm by 1.7 mm.

In addition to a buried-channel CCD, Output Register A, for scanning the infrared detectors, the chip also contains an identical register, Output Register B, driven by the same clock lines. In the tests reported here, the two registers were normally used together to cancel the common-mode clock pick-ups. However, it is also possible with this sensor to perform on-chip frame comparison schemes such as moving-target indication. The output registers are two-level polysilicon, two-phase BCCD's with 40 μm stages, and have been designed rather conservatively with 15 μm gates, 5 μm spaces, and 5 μm gate overlaps.
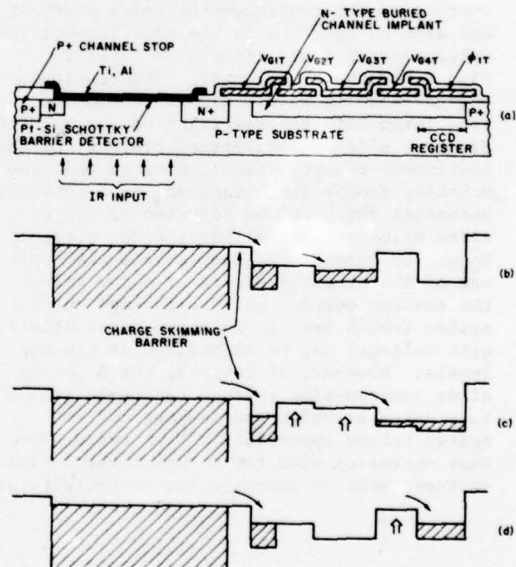
Fig. 4. Construction and operation of the Schottky-barrier detectors operating in the continuous-charge-skimming mode.

The readout of charge from the Schottky-barrier detectors in the line sensor is illustrated in Fig. 4 using the "continuous-charge-skimming" mode*. The detector array is backside illuminated. The function of the surface-channel gate G_{1T} is to maintain a fixed (dc biased) "charge-skimming" barrier that determines the reverse bias voltage for the Schottky diodes. During the integration (stare) time of the optical signal, the detected charge is collected in the charge-integration well under the buried-chanel gate G_{3T} (see Fig. 4(b)). The function of the buried-channel gate G_{4T} is to isolate the charge-integration well from the CCD output register. At the end of the stare time (variable from 10 to 100 ms) the collected charge signal is transferred from the inte-gration well to the serial CCD output regis-ter by a form of push clocking (one with slow fall time) as illustrated in Figs. 4(c) and (d). The output-register clock rate can be varied from 1 kHz to 5 MHz. For most of the measurements reported here, stare and line times were maintained at 30 ms and 23 ms, respectively.

Although the line sensor is designed to operate in the continuous-skimming mode, it can also be operated in the more conventional voltage-reset mode illustrated later in Fig. 9 for the area sensor. The continuous-charge-skimming mode minimizes the noise associated with the resetting of the Schottky diodes. Also an interesting property of the continuous-charge-skimming mode is that the Schottky diodes are maintained at a constant potential which can be adjusted to any de-sired value by controlling the dc voltage V_{G1T}. By maintaining the reverse-bias volt-age of the Schottky diodes at a low value, the leakage current and the leakage current spikes (which tend to increase exponentially with voltage) can be maintained at minimum levels. However, if desired, the Schottky diode reverse-bias voltage can be increased to a value at which the leakage current spikes become appreciable. Our tests show that operation with the larger reverse-bias voltage tends to increase the sensitivity of

these devices as infrared sensors. Finally it should be added that construction of the line sensor with separate CCD-type, charge-integration wells, results in the charge-handling capacity of the sensor being limited by the design of the CCD readout structure rather than by the normally-smaller depletion-layer capacitance of the Schottky diode.

C. 25x50-Element IR-CCD Area Sensor

A block diagram and a photomicrograph of the area-sensor chip are shown in Figs. 5 and 6. The chip is 5.84 mm square. The area sensor contains 25 columns of detectors with 50 detectors in each. The 25 column, charge-coupled shift registers are interspersed with the detector columns, and connect to a hori-zontal register at the top of the photo. The output stage is at the top left. The vertical detector spacing is 80 μm, while the horizontal detector spacing is 160 μm. The active area of each detector is 2100 $(\mu m)^2$ or 16.4% of the unit-cell area. The chip is mounted in a 28-pin dual-in-line ceramic package with a 4.75 mm square opening under the chip for near IR illumination. The chip also contains a 62-element line array, not discussed here, and many test devices.

INTERLINE TRANSFER SCHEME
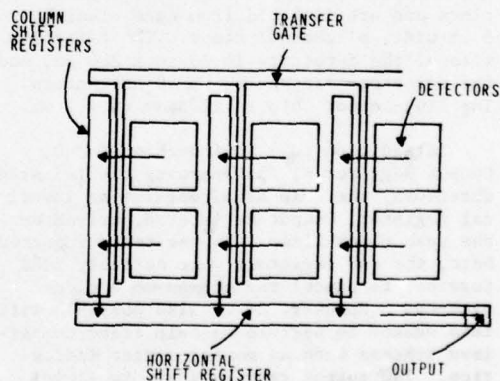
Fig. 5. Block diagram of the 25x50-element IR-CCD area sensor.

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*This mode of operation of the CCD imager, developed independently at RCA Laboratories, has been described by [15,16].
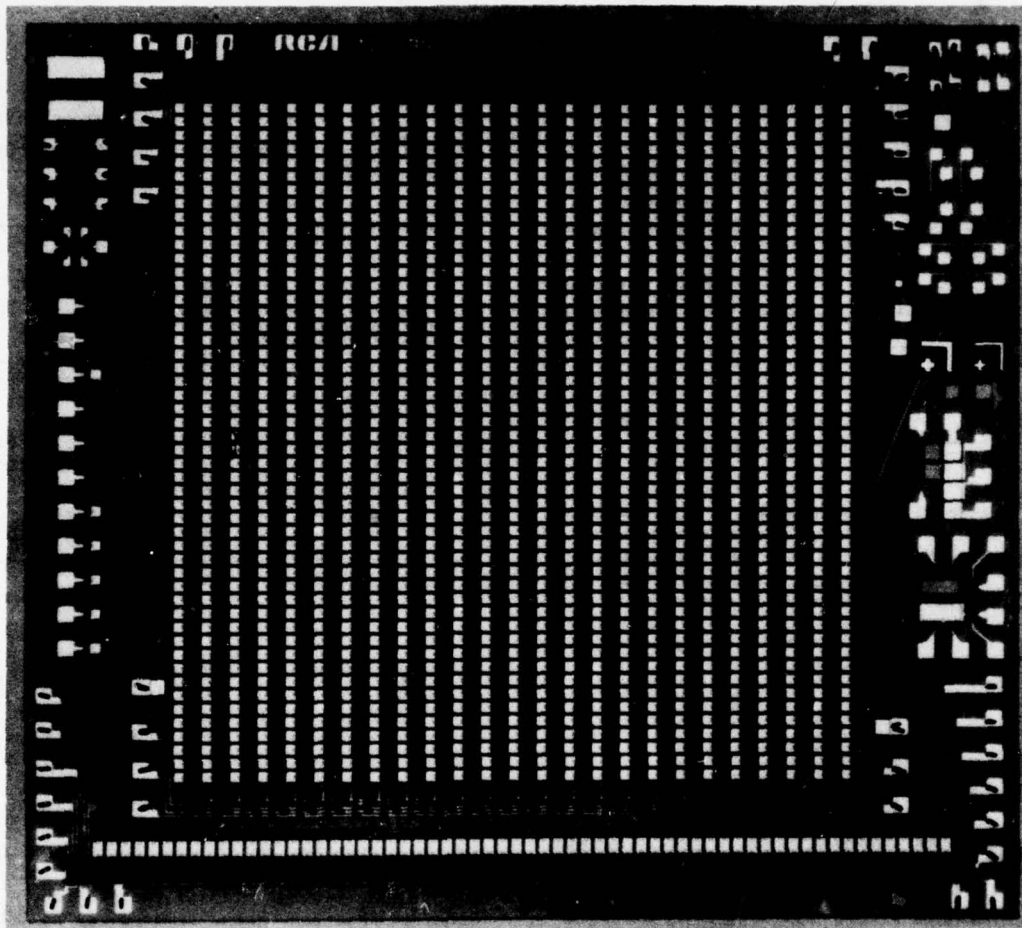
Fig. 6. Photomicrograph of the 25x50-element IR-CCD area sensor.

The construction of the area sensor is illustrated in more detail in the schematic diagram in Fig. 7. This diagram illustrates all of the elements and identifies the electrical terminals. This sensor has an interline-transfer organization. The infrared detectors are separated from the buried-channel CCD (BCCD) column shift register by vertical, surface-channel transfer gates. In the staring mode of operation, the detected image is transferred from the infrared detectors to the BCCD column registers once every frame time. Then, while the detectors integrate a new frame, the original frame is transferred, a line at a time, from the BCCD column registers to the BCCD horizontal output register, from which each horizontal line is read out in series by the floating-diffusion output amplifier. The floating-diffusion sensing-node capacitance of this device is about 0.7 pF, and the voltage gain of the source-follower output circuit is about 0.7. The column registers and output register are two-level-polysilicon, four-phase CCD's with 80 μm-long stages. The vertical column registers are coupled to every second stage of the output register.
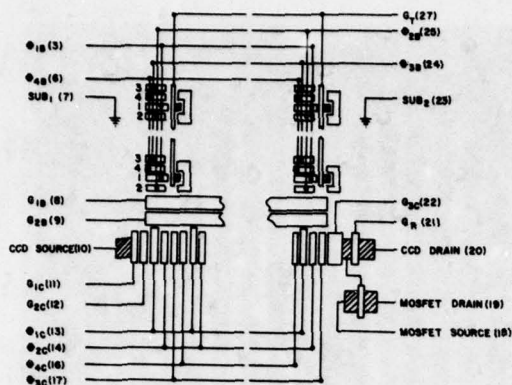
Fig. 7. Schematic diagram of the 25x50-
element IR-CCD area sensor.

A detailed description of the platinum-
silicide detectors of the area sensor is
shown in Fig. 8. This figure illustrates
how the effective area of the detector of
2100 $(\mu m)^2$ or 3.36 mil^2 is determined.
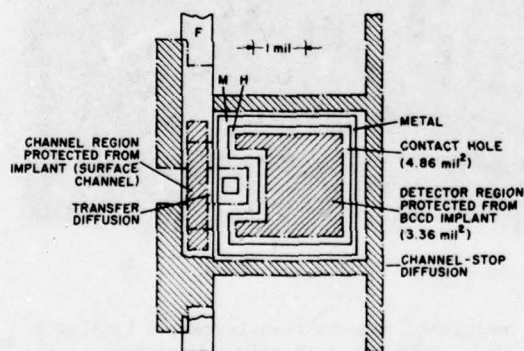
Fig. 8. Scale drawing of the effective
detector areas of the 25x50-element
IR-CCD area sensor as defined by the
Schottky-contact mask and the bur-
ied-channel or the guard ring mask.

The area sensor is operated in the volt-
age-reset mode illustrated in Fig. 9. This
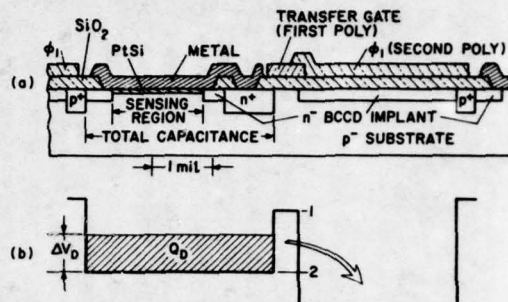
Fig. 9. Construction and operation of area-
array detectors: (a) cross section
of area sensor showing detector
region, transfer structure and
shift-register gate. (b) electron-
energy profile during voltage-reset
operation of detector.

mode was previously referred to as the
"vidicon" mode [4,9]. In this mode the
(surface-channel) transfer gate is pulsed
positively once each frame. The detectors
are set to a reverse bias determined by the
surface potential under the transfer gate
during the transfer pulse. Between transfer
pulses, the detectors are discharged by
infrared response and by dark current. At
each transfer pulse, each detector is set
to the same reverse bias as the previous
time, so that the charge removed to the CCD
well, as in Fig. 9(b), is the true signal
from the detector. As in the case of the
continuous-charge-skimming mode, small non-
uniformities in transfer threshold and detec-
tor capacitance do not cause non-uniformities
in the video signal, making possible direct
imaging without computer processing of the
video signal. By using a surface-channel
transfer gate between the Schottky diode and
the buried-channel CCD structure, we can cut
off (isolate) the Schottky diode from the
BCCD output register and thus allow testing
the CCD register at room temperature. The
surface-channel transfer gate is also needed
for the operation of the Schottky-diode
detectors in the blooming control (satura-
tion) mode (see Section IV-E).

IV. EXPERIMENTAL RESULTS

A. CCD Characteristics at 77 K

At room temperature the charge-transfer loss of the buried-channel CCD registers was typically 10^{-5} per transfer for operation with about 10% of bias charge and about 2×10^{-5} without the bias charge. At 77 K the transfer inefficiency was found to be larger, typically 5×10^{-5} with bias charge and 4×10^{-4} without bias charge.

For the infrared measurements reported here the line sensor and the output registers of the area sensor were always operated with a bias charge. However, the column registers of the area sensor have no provision for electrical input and thus exhibited some observable transfer inefficiency.

B. Dark (Leakage) Current of Platinum-Silicide Detectors

The theoretical dark current of an infrared-sensitive Schottky-barrier detector is due almost entirely to the internal thermionic emission of carriers from the metal over the barrier into the semiconductor. The current density for this process is given by [9]

$$J = A^* T^2 \exp - \frac{q\psi_{ms}}{kT} \qquad (2)$$

where A^* is ~ 32 A/cm^{2}K^2 for holes in Si, ψ_{ms} is the barrier height, q is the electronic charge, k is the Boltzmann's constant, and T is the detector temperature. For platinum-silicide Schottky-barrier detectors, the above dark-current density is 4×10^{-13} and 2×10^{-10} A/cm^2 for operation at temperatures of 77 and 90 K, respectively. In practice, the measured dark current of the platinum-silicide detectors tends to be increased by field concentration at the diode edges. This excess dark current can be controlled with n-type guard rings. Our experience shows that with the best devices operated at 80 K, no dark current is observed for thermal imaging with integration time in the range from 30 to 100 ms.

C. Infrared Test Set-Up

The experimental set-up used for infrared measurements consisted of an Electro-Optical Industries blackbody source and differential-temperature scene, Space Optics Research Lab IR optics, and an Air Products Displex refrigerator for cooling the arrays. The optics used included a four-element SORL f/1.2 Si/Ge lens which is AR coated for the 2-5 μm region.

For the infrared measurement, the sensors were cold-shielded and cold-filtered (3.4-4.2 μm) to minimize the background signal. The optical signals were imaged on the platinum-silicide sensor arrays through the back side of the optically-polished silicon substrate.

D. Uniformity

Because of low contrast in thermal scenes, spatial photoresponse non-uniformity can rapidly degrade the temperature sensitivity (NET) of staring arrays [17]. For example, a Schottky sensor with 4.5 μm cut-off has a signal-to-background contrast of 5%/K when responding to a 300 K scene. Therefore, a spatial uniformity of 0.5% is required to resolve 0.1 K [3]. As previously discussed, platinum-silicide Schottky-barrier IR-CCD's have inherently uniform response because photoyield is nearly independent of substrate doping concentration and lifetime. Thus it is possible to produce arrays which require no off-chip processing for individual pixel gain and no offset correction. The uniformity achieved with the 256-element IR-CCD line sensor is illustrated by the background response shown in Fig. 10. In Fig. 11 we show a typical portion of the line array illuminated by a 500 K blackbody source (through a 50% neutral density filter). The measured rms spatial non-uniformity across the line array is limited only by detector area variations due to the geometric definition of the diodes (i.e. reticulation).

E. Infrared Transfer Characteristics

The transfer characteristics of the 256-element IR-CCD sensor are shown in Fig. 12. The measured signal-to-noise ratio (S/N) is plotted versus the power density reaching the
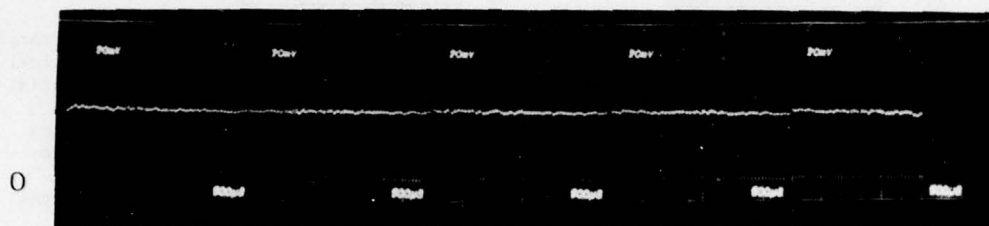
Fig. 10. Background response of 256-element IR-CCD line sensor with 3.4 to 4.2 μm band pass.
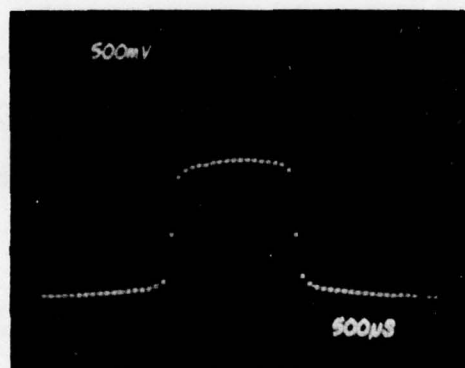
Fig. 11. Response of a typical portion of the 256-element IR-CCD line sensor as illuminated by a 500 K source (using 3.4 to 4.2 μm band pass filter and a 50% N.D. filter).

Fig. 12. Transfer characteristics of the 256-element IR-CCD line sensor.

back surface of the array. Since this array has no antireflective coatings, 30% of the incident power is reflected from the surface of the silicon substrate. The noise signal, determined by a superposition of the scope traces, corresponded to 2.0 mV peak-to-peak of which approximately 1.5 mV corresponds to a random noise and 1.5 mV to a coherent type of pick-up noise. From the curve in Fig. 12
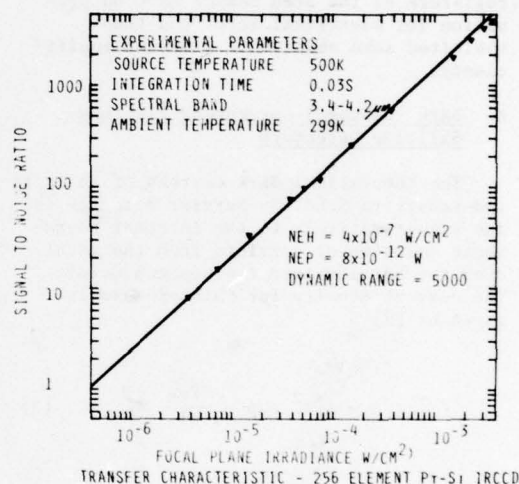
we determine the noise-equivalent irradiance (NEH) in the 3.4-4.2 μm band as 4.5×10^{-7} W/cm^2 which corresponds to the noise-equivalent power (NEP) per pixel of 8×10^{-12} W. The measured dynamic range (S/N max) of the line sensor is 5,000. A similar measured transfer curve for the area sensor is shown in Fig. 13. In this case NEH = 1.8×10^{-6} W/cm^2, NEP = 3.4×10^{-11} W, and the dynamic range is 1,800.
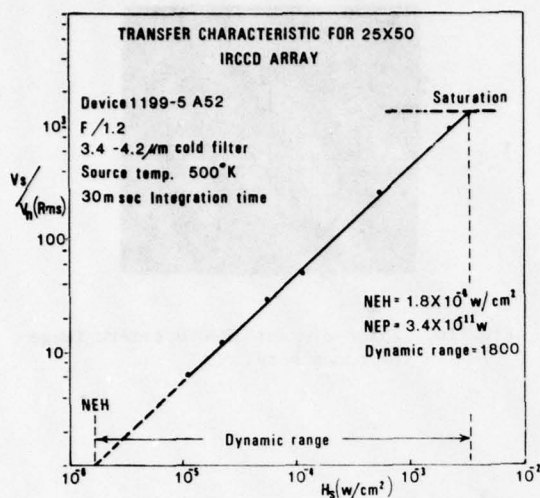
Fig. 13. Transfer characteristics of the 25x50-element IR-CCD area sensor.

Fig. 14. A 10°C test grid and a match flame imaged by the 25x50-element IR-CCD area sensor.

F. Thermal Response

The thermal transfer response of the 256-element IR-CCD line sensor is shown in Fig. 15 for 30 ms integration time. The experimental points in this figure are compared to the calculated response obtained by integrating the product of the Schottky photoyield function and the Planck blackbody spectrum [2]. By using a differential blackbody target, the noise-equivalent temperature (NET) of this array for 30 ms stare time was measured as 0.8°C against a 24.0°C ambient. A more recently measured line array with 20 μm x 200 μm detectors exhibited a reduced NET of 0.4°C.

Since the line sensor has been operated in the continuous-skimming mode, its dynamic range is limited by the capacity of the 50 μm-wide CCD output register. The area sensor is operated in the voltage-reset mode in which case the dynamic range of the sensor (the saturation level) is limited mainly by the effective capacitance of the detectors (estimated to be about 0.4 pF) and the amplitude of the transfer-gate voltage pulse, mentioned before in Section 3C. The Schottky-barrier detector design with a surface-channel transfer-gate and operated in the voltage-reset mode provides a built-in blooming-control mode of operation. In this mode the slope of the transfer curve past the saturation level (see Fig. 13) can be controlled by the duration of the transfer pulse.

The large dynamic range of the area sensor operating in the blooming control (saturation) mode is illustrated in Fig. 14. This figure shows a 10°C (above ambient) calibrated test grid detected by the area sensor with a match flame in the scene. While the match saturates the sensor where it is imaged, no blooming is observed. There is also no lag.

Fig. 15. Thermal response of the 256-element IR-CCD line sensor.

Fig. 16 shows the area-sensor image of radiation from a human hand ($\sim$ 32°C in 26°C ambient). The weakest target observed with the 25x50 IR-CCD area sensor had temperatures slightly less than 1°C above ambient (26°C). The present measurements are limited by excess noise and low diode-breakdown voltages. Correcting the above problems should improve sensitivity by at least a factor of 5. Further, recent processing advances have led to thin diodes that are a factor of 2 more sensitive at all wavelengths. Thus we believe that both present devices could be improved so as to have NET in the range of 0.1 to 0.2°C.

Table I summarizes and compares parameters measured for both line and area sensors.

Fig. 16. 25x50-element IR-CCD camera image of human hand.

Table I

Parameters for 256-Element Linear and 25x50-Element Area PtSi IRCCD: 3.4-4.2 μm, 30 ms stare time

Parameter	Value Line	Value Area	Comment
NET (°C)	0.8°C	1.0°C	0.4°C with larger area diodes ultimately 0.1°C.
NEH (W/cm^2)	4.5x10^{-7}	1.8x10^{-6}	
NEP (W)	8x10^{-12}	3.36x10^{-11}	
Linear Dynamic Range	5,000	1,800	Presently CCD limited for line array. Detector limited for area array.
Noise Level (mV p-p)	$\sim$2 mV p-p	2 mV p-p	1.5 mV random; 1.5 mV coherent pick-up.
Photoresponse Uniformity (%)	0.55%	2%	Reticulation limited for line array.
Quantum Efficiency Coefficient (%/eV)	$\sim$5%/eV	$\sim$5%/eV	
Operating Temperature (K)	80 K	80 K	40 K-103 K
Transfer Inefficiency (per transfer)	5x10^{-5}	5x10^{-5}	77 K, 10% bias charge.

V. CONCLUSIONS

The advantages of the Schottky IR-CCD's are:

. high uniformity limited only by the geometric definition of the detectors

. high detector densities possible

. modest cooling requirements (in the range of 80 to 90 K)

. no optical cross-talk

. monolithic silicon construction with standard IC processing

. staring mode of operating

. no lag

. very large dynamic range

. antiblooming capability.

We have developed two types of IR-CCD's with Schottky-barrier platinum-silicide detectors, a 256-element line sensor and a 25x50-element area sensor.

We have demonstrated thermal imaging with a temperature discrimination of 1°C above ambient for the 25x50-element area sensor and 0.4°C for the 256-element line sensor.

With new designs and processing improvements, Schottky IR-CCD's with higher density and capable of temperature discrimination in the range of 0.1 to 0.2°C above ambient are anticipated. Such IR-CCD sensors, with resolution approaching that of commercial television, are expected to have applications in IR surveillance, reliability studies, and medical diagnostics.

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THE PbS-Si HETEROJUNCTION: A NEW APPROACH TO INFRARED FOCAL
PLANE ARRAY INTEGRATION

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Abstract

A novel approach to IR focal plane array integration, the PbS-Si Heterojunction, is presented. The PbS-Si HJ structure and basic electrical properties are discussed. The IR detection properties of isotype and anisotype HJ's are covered mainly in the current mode operation. Detectivity levels higher than 10^{11} cm $\sqrt{Hz}$/W are reported at 85°K and 2 Hz. The integration of the HJ with either a CCD or MOS switch array is discussed. An experimental CMOS chip designed to evaluate the PbS-Si HJ focal plane array is presented.

I. Introduction

The current work in the area of the monolithic integration of large scale infrared focal plane arrays with a solid state self-scanned read-out mechanism is centered on the use of charge coupled devices [1]. The two basic approaches receiving most attention are direct extensions of the original charge transfer concept: a) the use of an MOS structure built around a narrow bandgap semiconductor substrate; b) the use of an MOS structure built around a Si substrate doped with shallow, IR-sensitive impurities.

In this paper, we discuss a novel approach: the thin film narrow gap semiconductor - Si heterojunction. In the heterojunction approach, IR photons are absorbed in the narrow gap thin film. The resulting photocarriers are injected into the Si substrate where they are first accumulated at individual storage sites and then transferred out by a CCD shift register. Alternatively, the read-out can be performed by an array of MOS switches in which case random as well as serial read-out can be achieved. The principal advantages to be derived from this approach are due to the fact that in the heterostructure the photogeneration and read-out processes are separated and performed in materials appropriate for each function. First, the detection takes place in the narrow bandgap semiconductor requiring only a thin film of no more than a few microns. Second, the charge transfer process takes place in a CCD structure fabricated on standard Si material, thus fully utilizing the advantages of IC technology.

The advantages of the heterojunction approach can be realized, however, only if the detection properties of the basic heterojunction are competitive with state-of-art IR detectors. In this paper we will discuss the operation and characteristics of the PbS-Si heterojunction (HJ) detector and its application to focal plane integration.

II. PbS-Si HJ: Structure and Basic Properties

The PbS-Si HJ is formed by growing, at room temperature, a PbS film from chemical solution onto a silicon substrate. Constituents of the chemical solution growth technique [2], [3], [4] are the following: Lead Nitrate($Pb(NO_3)_2$), Sodium Hydroxide (NaOH), Thiourea ($(NH_2)_2 CS$) and Deionized Water. The growth reaction results in a PbS film in intimate and continuous contact with the silicon substrate, as can be seen in the SEM photograph of Fig. 1. The
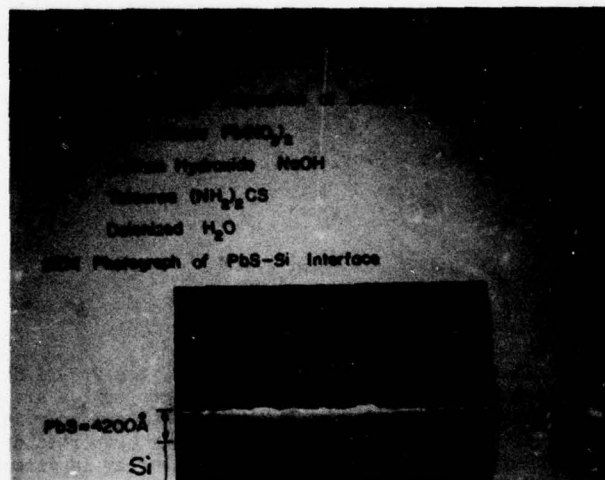
Fig. 1 PbS-Si HJ Fabrication
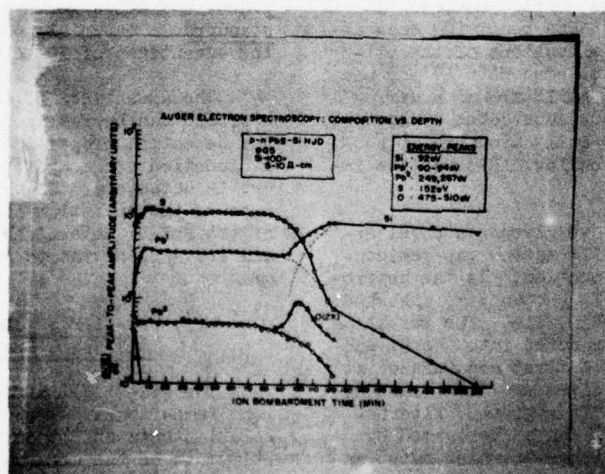
Fig. 2 Auger Electron Spectroscopy

PbS films grown by this method have been shown by X-ray diffraction to be polycrystalline. We have successfully delineated the PbS crystallite pattern using a heat treatment technique [5]. The average grain size in the plane of the substrate has been determined to be around 2500Å. The basic chemical composition and uniformity of the PbS film was investigated by Auger Electron Spectroscopy. An example is shown in Fig. 2 for a PbS film grown on (100) Si. A uniform film composition and a fairly abrupt junction are observed. The O_2 peak of the interface can be attributed to either traces of SiO_2, PbO or surface absorbed oxygen.

The PbS films grown by chemical solution growth have been found to be p-type. Therefore, either isotype [6] (p-p) HJ's or anisotype [7] (p-n) HJ's can be obtained by choosing either p or n-type Si as a substrate. The basic electrical properties of the PbS-Si HJ can be studied from the current voltage (I-V) and capacitance-voltage (C-V) characteristics. In Fig. 3 is shown a typical I-V characteristic of a p-p PbS-Si HJ at 77°K. This device has an area of $6 \times 10^{-4} cm^2$. The extremely small leakage current and sharp turn-on characteristics are indicative of the high quality of our devices. In Fig. 4 is shown the C-V characteristic of a PbS-Si HJD at both 77°K and 300°K. The data is plotted in the usual $1/C^2$ vs. V format. The linear relationship under reverse bias follows the theoretical characteristic and is therefore also indicative of the quality of the HJD.

III. IR Detector Characteristics

We have found that the PbS-Si HJ exhibits substantial IR sensitivity in both isotype [6] and anisotype [7] form when operated in either the voltage (open circuit) mode or the current mode [8]. In this paper, we will highlight the properties of one p-n PbS-Si HJ operated in the current mode at a temperature of 80 to 85°K. It is worthwhile to note that we have achieved a detectivity of over $10^{11} cm \sqrt{Hz}/W$ in the 2.5-3.0μm region.

The photocurrent signal measurements were performed on the blackbody test station illustrated in Fig. 5. In Fig. 6, the photocurrent is plotted versus power density for different values of bias at a signal frequency of 10 Hz. The photocurrent is seen to increase a factor of 3-5 when the bias is raised from zero volts to -50 mV. To obtain the same factor of signal improvement again one has to increase the bias to between -1 V to -2 V. It is important to note that the linear region of the photocurrent vs. power curve is extended as one increases the bias. The frequency response of the photocurrent as a function of bias level is shown in Fig. 7.

Current noise measurements have been performed as a function of frequency and bias. These measurements require considerable care due to the very low level of noise generated by the HJD. In Fig. 8, the current noise at zero bias and at -50 mV bias is shown as a function of frequency. It is important to note that the noise for both bias levels is essentially the same over the entire range measured, 2 Hz to 1 kHz. As shown above, the signal at -50 mV is between three to five times higher than at zero bias. It can also be seen from the data that no 1/f noise component was observed in either case down to a frequency of 2 Hz. The preamp current noise is also plotted separately in Fig. 8. Due to the very low noise of the HJD, the total noise measured in the 2-10 Hz range is very close to being preamp noise limited. For example, at 2 Hz and -50 mV the total current noise measured is 5 fA Hz. The preamp noise was measured to be 3.5 fA/$\sqrt{Hz}$ resulting in a calculated detector-only current noise of also 3.5 fA/$\sqrt{Hz}$.

The blackbody detectivity has been calculated from the signal and noise data presented above. In Fig. 9, the blackbody detectivity is plotted versus frequency at zero bias and -50 mV. At a frequency of 2 Hz and -50 mV bias we obtain a detectivity of $1.8 \times 10^{11} cm \sqrt{Hz}/W$ while for zero bias and 2 Hz a $D_{BB}^* = 6 \times 10^{10} cm \sqrt{Hz}/W$ is obtained. The relatively high reproducibility of the PbS-Si HJ detectivity is exemplified in Fig. 10, where D_{BB}^* is plotted versus frequency for two detectors held at the same bias level of -50 mV. The spectral response of the HJD was measured on the test station illustrated in Fig. 11. The spectral response of the p-n PbS-Si HJD operated in the current mode and with zero bias is shown in Fig. 12. In Fig. 13, the spectral detectivity is plotted at a frequency of 2 Hz and a reverse bias of 50 mV. In the spectral region of interest, 2.5-3.0 μm, D_λ^* is around $10^{11} cm \sqrt{Hz}/W$. At λ = 2.75μm the conversion factor from blackbody to spectral detectivity is approximate-
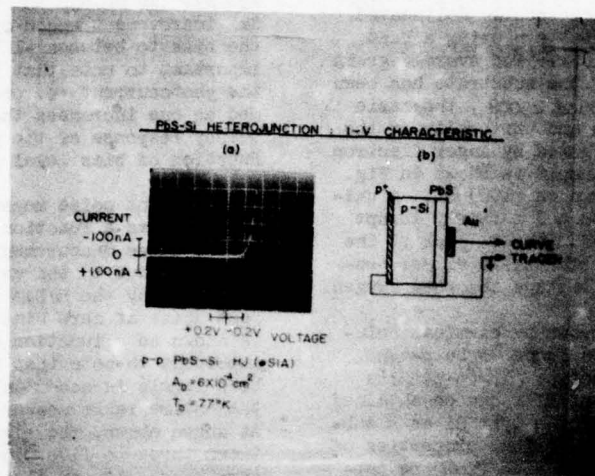
Fig. 3. p-p PbS-Si HJ: I-V Characteristic

Fig. 4 p-p PbS-Si HJ: C-V Characteristic
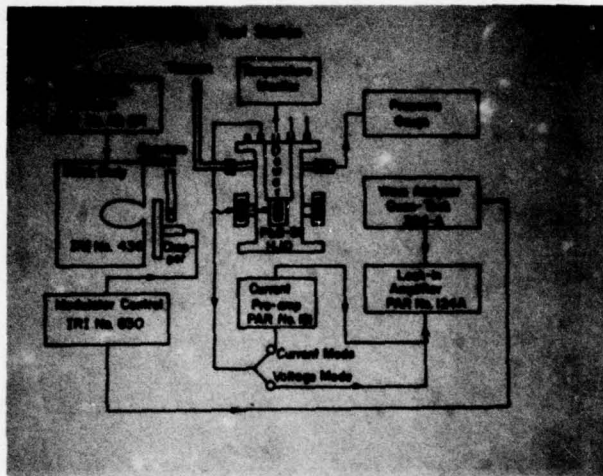
Fig. 5 Blackbody Test Station
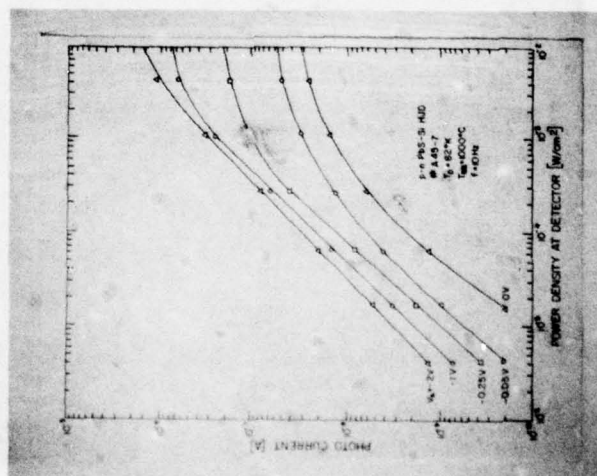
Fig. 6 Photocurrent vs. Power Density at f = 10 Hz
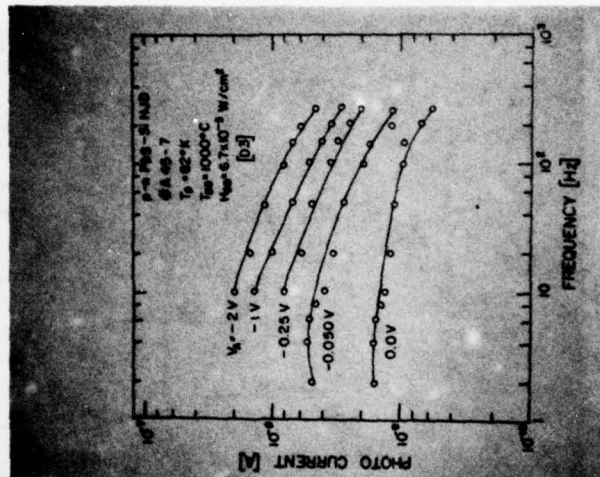
Fig. 7 Photocurrent Frequency Response at $6.7 \times 10^{-5} W/cm^2$
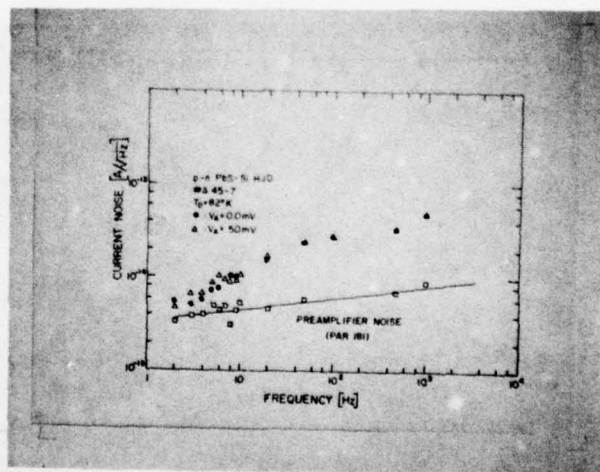
Fig. 8 Detector Current Noise
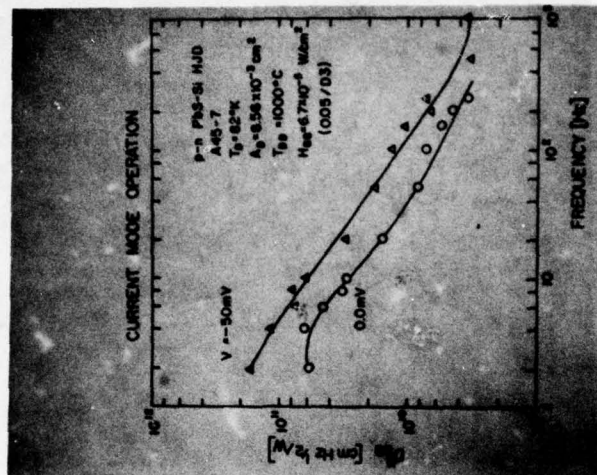
Fig. 9 Blackbody Detectivity for $V_A = 0$, -50 mV
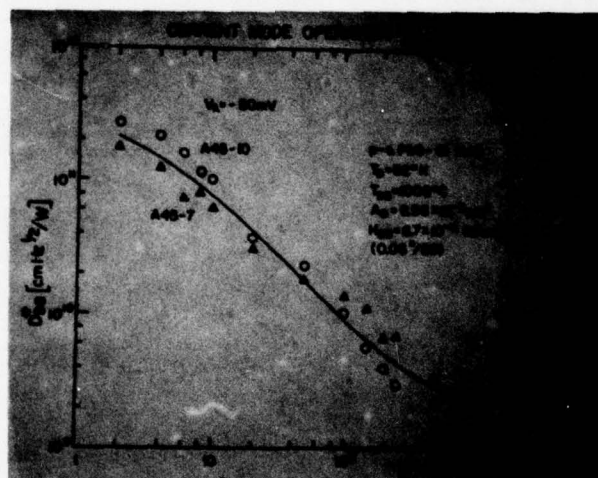
Fig. 10 Blackbody Detectivity for Two Detectors
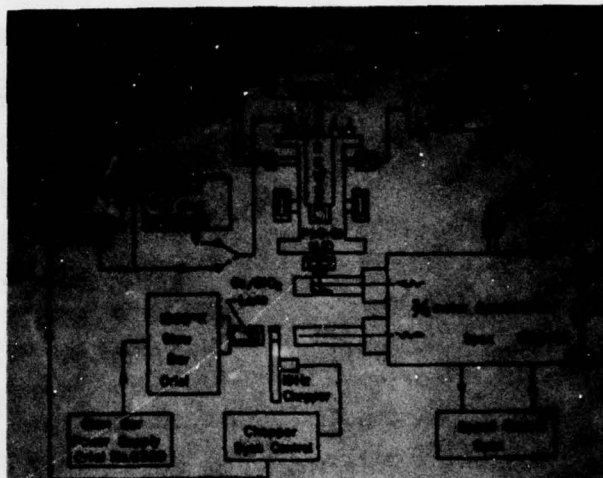
Fig. 11 Sprctral Response Test Station
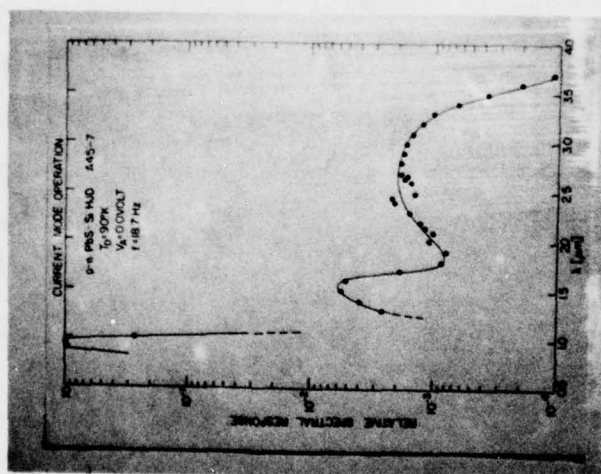
Fig. 12 Current Mode Spectral Response
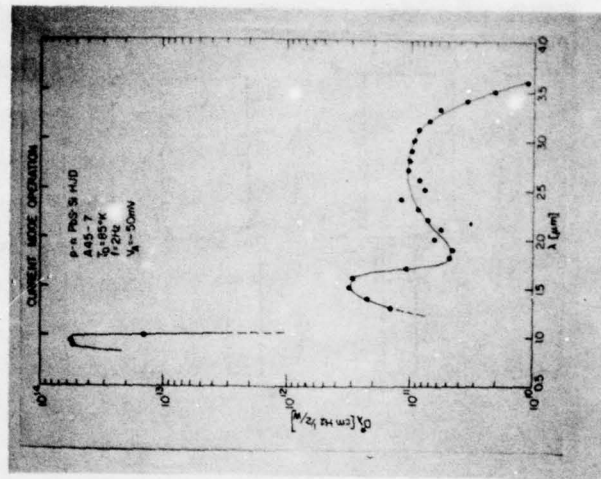
Fig. 13 Current Mode Spectral Detectivity
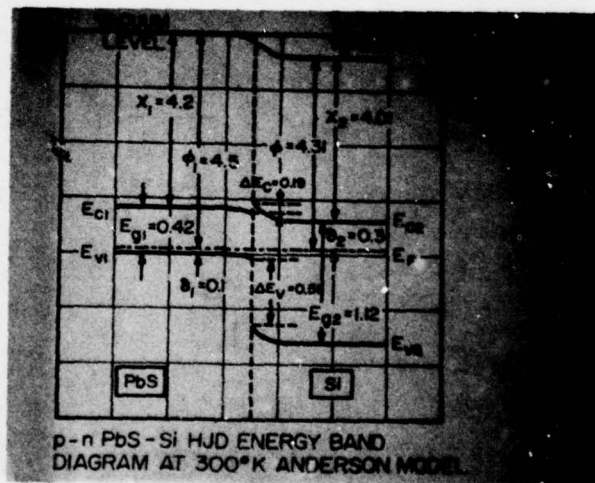
Fig. 14 PbS-Si HJ Energy Band Diagram
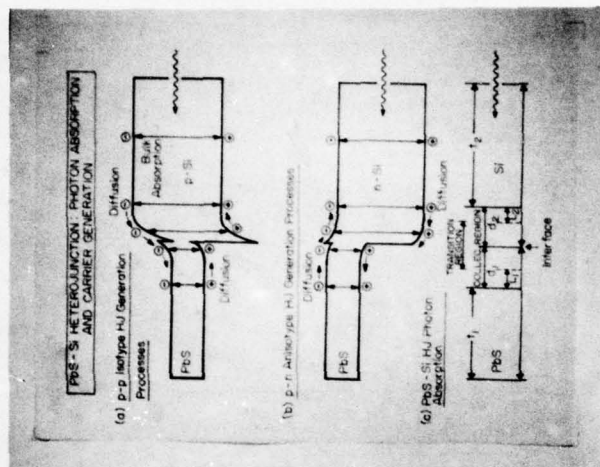
Fig. 15 Anisotype HJ Generation Processes
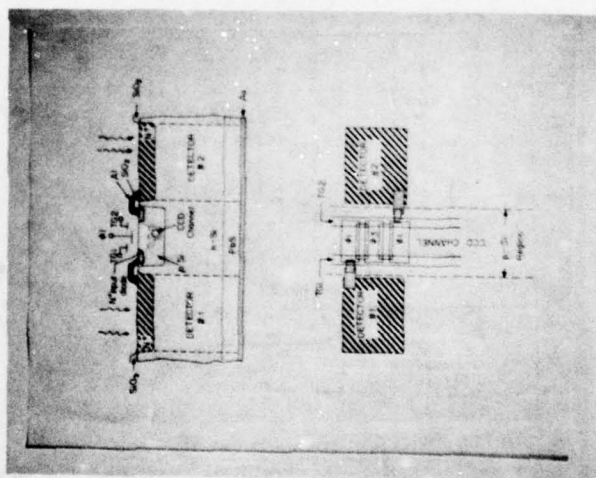
Fig. 16 PbS-Si CCD Integration
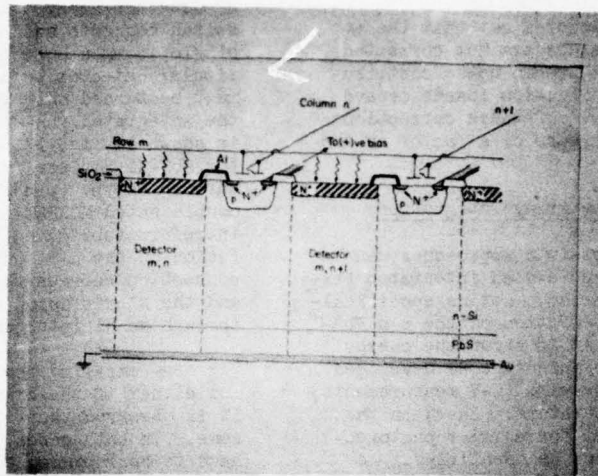
Fig. 17   PbS-Si MOS X-Y Integration
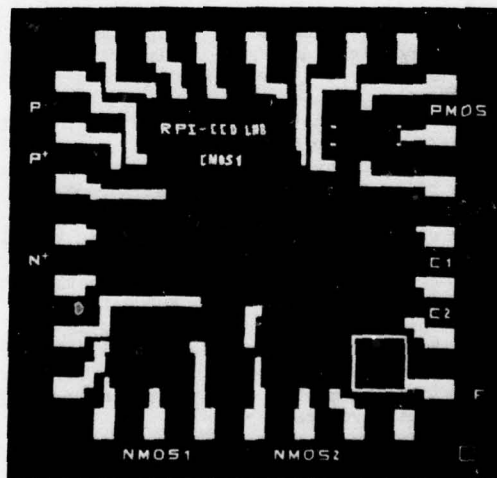
Fig. 18   CMOS Integration Chip

ly 2/3. Therefore by multiplying the curves of figures 9 and 10 by 2/3, the frequency response of D_λ^* (2.75 μm) can be observed.

It should be pointed out that the above detectivity values are not corrected for the substantial preamp noise contribution nor for the reflection losses caused by the dewar window. If these corrections are included an increase of a factor of two in D_λ^* is obtained.

IV. HJ Focal Plane Array Integration

A number of possible approaches can be taken in order to achieve an integrated PbS-Si HJ focal plane array. Let us specifically consider the integration of the p-n PbS-Si HJ. In Fig. 14 it is shown the energy band diagram of the anisotype HJ developed from experimental results (C-V measurements) and data in the literature. Based on the energy band diagram, the carrier photogeneration processes can be identified. As can be seen from Fig. 15, photoelectrons generated at or close to the interface result in the current which represents the infrared sensitive process. In reverse bias operation the Si substrate is held at a positive potential with respect of the PbS film, resulting in a dramatic photocurrent increase.

On this basis we have devised the integrated PbS-Si HJ CCD shown in Fig. 16. In Fig. 16a, the cross-section of the device is shown. Each HJ detector is connected through an Al interconnect to an input diode of the CCD register. The CCD is a n-channel device fabricated on a deep p-diffusion in the substrate. The HJ detector is effectively connected to the CCD channel through gate TG which also sets the bias on the detector. Since the CCD is n-channel, the polarity of the gate voltages will be positive, which is also the polarity required for reverse bias operation of the p-n PbS-Si HJ. In this fashion we will be injecting IR photogenerated electrons into the CCD and collecting them in the potential well under $\emptyset 1$. While only a very simple CCD input was used in this illustration, more versatile and more complex input circuits could be designed in order to implement such functions as background subtraction. A top view of the PbS-Si IRCCD is shown in Fig. 16b. In the particular design shown, two detector columns are accessed alternately by one CCD register in order to minimize dead space.

A second integration technique uses an array of MOSFET switches addressed by X and Y scan generators to read out the PbS-Si HJ detector array. A double-gated MOSFET switch connects each detector element to a single, common output. To read out a particular detector both gates of the switch must be turned on. The cross-section of the integrated PbS-Si HJ/MOS X-Y read-out is shown in Fig. 17. The cross-section of the PbS-Si HJ itself is that of the standard anisotype (p-n) PbS-Si structure. The double gated MOSFET switch is n-channel and therefore fabricated in a deep p-type diffusion on the n-Si substrate. The interconnection between the detector N^+ contact and the N^+ diffusion of the MOSFET is made through an Al interconnect.

By comparing the structure required for either of these integration approaches, it is observed that it is essentially the same. In both cases, n-channel circuits have to be implemented on an n-type substrate, thus requiring a p-well. We have therefore designed and fabricated a CMOS chip which contains the common basic structure and circuit required for the read-out of the integrated PbS-Si focal plane array. A photograph of the chip is shown in Fig. 18. The chip contains two devices designed to test the integration by either hard-wiring the detector output to the MOSFET input (NMOS1) or by a completely integrated structure (NMOS2). Also present on the chip are a p-channel device and test capacitors and resistors.

V. Conclusions

In this paper we have discussed the basic properties and the detector characteristics of the PbS-Si HJ. Detectivities of greater than 10^{11} cm $\sqrt{Hz}$/W have been reproducibly achieved. PbS-Si MOS integration structures have been discussed and a CMOS integration chip described. In conclusion, we feel that the PbS-Si heterojunction detector represents an attractive approach for the achievement of focal plane array integration in the 3μm region.

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THEORETICAL LIMITATIONS OF NARROW BANDGAP SEMICONDUCTOR MIS DEVICES USED AS IR IMAGING DETECTORS.

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Abstract : The silicon example has been a useful approach to IRCCD and CID processing, but specific limitations due to the nature of narrow bandgap semiconductors have emerged progressively. This paper will consider, via the elementary MIS cell, the effect on key parameters of the system of the following physical phenomena : the tunnel current on the magnitude of stored charge, dark current on storage time, insulator traps on stability and reproducibility, interface states on transfer and noise. The results show that the performance is strongly dependent on process improvement.

INTRODUCTION

Among the different approaches available for the development of infrared-optical imaging and detection systems, monolithic IRCCD and CID processing techniques have received the most particular attention in the past few years. As a result, a tremendous effort of investigation on materials like doped wide bandgap and narrow bandgap semiconductors has been necessary.

Even if the doped silicon could appear as the most attractive choice due to the advantage of the well skilled silicon technology, III-V and II-VI compound devices, in spite of their novelty, became rapidly brought to a high state of development. In that case, the silicon example has been certainly useful to set up the first step of a new procedure ; but specific limitations due to the nature of these narrow bandgap semiconductors have emerged progressively. Some of them have been already studied extensively ; others need additionnal work to be explained. The aim of this paper is to analyse their impact on MIS devices used as IR imaging detectors. In table I are shown the physical limitations facing the performances of narrow bandgap CCD or CID systems :

OPERATION PARAMETERS	PHYSICAL LIMITATIONS
magnitude of stored charge	tunnel current
storage time	thermal generation current (dark current)
stability and reproducibility	insulator traps
transfer	interface states
noise	

TABLE I

TUNNEL CURRENT INFLUENCE

One of the system performances arises from the maximum photonic charge quantity to be stored in the MIS detector. This quantity depends on the incident photon absorption in the semiconductor

and is also limited by the thermal carrier generation which is directly related to the depth of the transient depleted zone and to the minority carrier surface life-time. In narrow bandgap semiconductors, J.FARRE et al [1] were the first to focuse the attention on a third limitating phenomenon, a band to band tunnel current which restricts the dynamic of the structure, while W.W. Anderson [2] proposed a theoretical treatment of interband tunneling based on the WKB approximation to evaluate the corresponding current.

The effect of this current is easily observed in the transient capacitance versus voltage measurement when deeper and deeper depleting voltage steps are applied to the structure. As shown in figure 1, the transient depletion zone width keeps constant beyond the apparition point of the tunnel current.

One of the main conclusions was to predict the upper performance of the device as a function of the cut off wavelength of the material considered. As shown in figure 2, [1] the shortest the bandgap width is, the lowest is the maximum surface potential which can be reached in a deep depletion mode of operation of the MIS, the best conditions being obtained at low doping densities.

Figure 1 - Pulsed C-V plot of an elementary N-type InSb MIS cell.
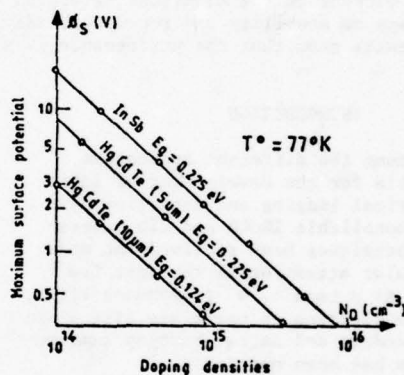
Figure 2

Notice that crystals presenting a carrier concentration below $10^{14} cm^{-3}$ are not up to now available on the market. Another direct consequence of the tunnel current will be to select high permittivity dielectrics in order to increase the maximum storage charge [3] . Finally, the effect of the working temperature on the bandgap width should be kept in mind.

THERMAL GENERATION

The thermal generation current or, even better, the minority carrier lifetime determines the technological requirements, the behaviour of the detector and the characteristics of the control electronic circuits. This can be seen especially through its influence on two parameters in CCD or CID operation : the storage time T_S, which determines the lowest frequency rate of the electronic circuits, and the transfer inefficiency η, which fixes the quality of the image.

A direct consequence is that the highest possible value of τ will increase T_S and minimize η as it can be shown, in the latter case, from the expression of η which can be deduced from the H-S. Lee and L.G. Heller paper [4] and put under the form.

$$\eta = \frac{4}{\pi^2} \left(\frac{L}{L_D}\right)^2 \frac{1}{U_S} Ln\left[1 + \frac{U_S}{1 + \frac{4}{\pi^2}\left(\frac{L}{L_D}\right)^2}\right]$$

where L is the electrode length, $L_d = \sqrt{D\tau}$ the diffusion length, $U_s = \frac{\phi_s}{U_T}$ the reduced surface potential, $U_T = kT/q$ the thermodynamic potential. A value of 10^{-8}s being readily obtained for τ, taking D=10 and assuming =1V, that means a 3 μm electrode length should be necessary to reach in these conditions an inefficiency factor $\eta = 10^{-2}$; whereas if τ can be dropped down to 10^{-7}S, L will rise up to 30 μm which is a length easily processed in wide applications.

According to this conclusion, a correct interpretation of the measurement of the lifetime τ and a good determination of the region of the semiconductor concerned with the measure are capital.

The method of the parallel conductance of the MIS structure can be used to provide the minority carrier lifetime at the surface of the semiconductor ; considering the equivalent model of the MIS of figure 3, where C_o, C_d and C_{st} are respectively the dielectric,
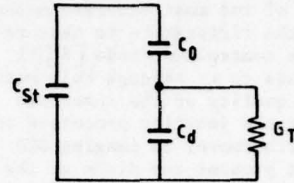
Figure 3 - Equivalent model of MIS Structure (inversion)

depletion and stray capacitance, G_t being the admittance accounting for the thermal generation, τ has been deduced from G_T which can be expressed under the form [5] [6]

$$G_T = \frac{q n_i L_D}{U_T \tau \sqrt{U_F} - exp \frac{U_F}{2}}$$

where q is the magnitude of the electronic charge, n_i the semiconductor intrinsic density, L_D the intrinsic Debye length and $U_F = \frac{\phi_F}{U_T}$ the reduced Fermi potential. A current value of 5×10^{-8}s has been obtained for InSb.

The transient capacitance method, also called the "Zerbst method" [7] provides τ within the depletion region and consists in applying a step voltage on the gate of the MIS, which deeply depletes the surface of the semiconductor. τ is determined from the slope of the linear portion presented by the relaxation curve : $-\frac{d}{dt}\left(\frac{C_o}{C}\right)^2$ versus $\frac{C_F}{C} - 1$ [7], where C_o is the dielectric capacitance, C and C_F being respectively the transient and steady-state (inversion) MIS capacitance. This method is especially suitable to "bulk dominated" samples" . MIS processed on semiconductor compounds can exhibit often a "surface dominated" characteristic, and make evaluation of τ more problematic, as the relaxation curve does not present any linear shape. Measurements on InSb samples have

yielded a mean value of 10^{-8}s.

A fully characterization of thermal generation in the detector implies the determination of another parameter : the surface generation velocity s_o. In silicon devices, one of the most accurate method proposed in the litterature to measure s_o used the gate controlled diode [8][9] However, access to s_o through this method needs a high quality of the interface SiO_2/Si under the junction processed under the gate. Furthermore, as imaging CCD arrays do not present any diode at the imput like in shift register or signal processing systems, a special device must be therefore processed to perform the measure. Consequently, this technique cannot be straightforward applied to III-V or II-VI coumpound semiconductors as long as the interface state density is not severely controlled.

The "Zerbst method" [7] is sometimes proposed to get the same evaluation. Actually, this parameter has been artificially introduced to account for a positive intercept of the relaxation curve on the ordonates (Y-axis) of the model which uses an approximated form for the bulk thermal generation current I_G taking place in the MIS pulsed into deep depletion, namely $I_G = \frac{qn_i}{\tau} (W-W_F)$ [10], where W and W_F are the transient and steady-state depletion width. In fact, the use of an expression accounting for the carrier generation in the whole space charge region rather than in the part included between W and W_F needs not any kind of such hypothesis and naturally leeds to a model presenting a positive intercept on the Y-axis of the extrapolation of the linear part of the relaxation curve. [11].

The transient capacitance method being inadequate to evaluate s_o, D.K. Schröder and H.C. Nathanson [12] have proposed the assumption of a variation with time of the surface recombination velocity to overcome the discrepancies between theory and experiment : but it seems difficult to physically justify this hypothesis, especially if we consider the "screen" effect of the inversion layer during the transient.

At this state of the technology, a direct measure of s_o on IRCCD or CID processed on narrow bandgap material does not seem available. The method developed for silicon by D.G. Ong and R.F. Pierret [13] using a CCD connected in a gate controlled diode configuration could be later a way to reach the surface recombination velocity.

INSULATOR TRAPS EFFECT

Very few papers in the litterature report a time instability which could affect the MIS elements of a IRCCD. However, we have often noticed, especially on structures processed on Indium Antimonide, the presence of a hysteresis on C – V characteristics whose magnitude is a function of the extremes of voltage stress : V_A (accumulation), V_I (inversion) and on the voltage sweep rate $\frac{dV}{dT}$. Such a problem had previously arised with the first silicon structures, the origin of the phenomenon being essentially a migration of mobile ions in the silicon dioxide. In the present case, ionic drift within the insulator or polarisation of the dielectric layer can generally be ruled out, and a study of the flat band voltage shift ΔV_G (t) with parameters V_A, V_I, $\frac{dV}{dt}$ and temperature, indicates that this shift should be due to the tunneling of free carriers from the semiconductor into the insulator traps [14][15]. The analysis of such a mechanism emphasizes the influence of the semiconductor bandgap, narrow bandgap semiconductors tending to magnify the hysteresis effect with respect to that of a structure of equal quality processed on silicon [16].

This difference can be seen through the analysis of the time dependent occupancy factor f_T of the trap located at a distance δ from the interface, which is given by [17][18].

$$\frac{df_T}{dt} = \frac{f_T - f_S}{10^{-13} \cdot exp\,(\chi^{1/2}\, \delta)}$$

where δ is expressed in angström, f_S is the occupancy factor at the semiconductor surface for the corresponding trap energy level, χ the electronic affinity of the semiconductor.

The equilibrium value $\overline{f_T}$ being reached for $f_T = f_S$, $\overline{f_T}$ will be $\ll 1$ for wide bandgap semiconductors like silicon

(case 1), whereas $\overline{f_T}$ will be close to 1 for narrow bandgap semiconductors (case 2), as they present a conduction band strongly degenerated near the surface under the accumulation condition.

Accordingly, assuming that all the traps within the insulator up to a distance $\overline{X}$ (t) from the interface are in equilibrium, the flat band shift will be

in case 1

$$\Delta V_{G_1} = \frac{N_T}{C_0} \cdot \overline{X}(t) \cdot \int_{E_C^s}^{\infty} Exp\left[-\frac{E_C - E_F}{RT}\right] dE_C$$

and in case 2

$$\Delta V_{G_2} = \frac{N_T}{C_0} \cdot \overline{X}(t) \cdot \int_{E_C^s}^{\infty} \frac{1}{1 + exp\frac{E_C - E_F}{RT}} dE_C$$

where E_C is the energy of the bottom of the conduction band and E_F the Fermi level energy.
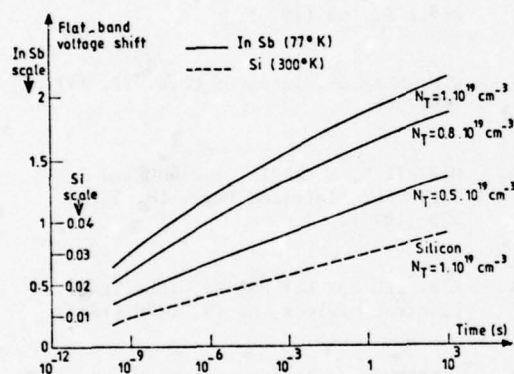
Figure 4

Values of ΔV_G for silicon at 300°K appear in figure 4 to be a hundred times smaller than those computed for a narrow bandgap semiconductor like InSb at 77°K. (A spatially uniform energy distribution density of traps N_T is assumed in the computation).

To overcome this disadvantage in the system behaviour, a "refreshment" operation can be used, consisting in a periodic cycling between V_A and V_I, in order to allow the MIS detector to work always along the same C-V characteristic. Such a method has been used in a 32 elements linear array processed on InSb with SiON CVD layer as dielectric and packaged in a dewar presenting a 15° field of view and a cold filter limiting the spectral bandwidth in the 3,7 to 4,8 μm range. The sensitive area of the elementary cell is 200 μm x 200 μm and an image at a 25 frames/second rate has been produced (figure 5).

Figure 5

Such a technique has been also applied successfully to a 8 x 8 elements matrix array, each cell presenting a sensitive area limited to 35 μm x 70 μm to get a good transfer efficiency.

INTERFACES STATES

Interface states are a well known severe limitation, through noise, transfer and stability, of the highest performances of IRCCD and CID.As a matter of fact, noise sources in CCD have been extensively analysed, especially by J.E. CARNES and W.F. KOSONOCKY [19][20] who have emphasized the major role of fast interface state

trapping over the other components of noise. In CID arrays, H.K.BURKE and G.J. MICHON [21] have underlined the minus importance of charge transfer noise in CCD devices, and discussed the possibility of rejection of KTC noise which could be one of the predominant source in such application, especially when the system behaviour is based on the parallel injection technique [21]. As measurement methods have been proposed by J.C. KIM to evaluate noise sources separately [22], we shall only add to, according to the works of S.CHRISTIENSSON et al on MOS Silicon transistors [23], the possible contribution of a 1/f spectrum noise in narrow bandgap systems caused by the tunneling mechanism between interface states and traps in the dielectric layer, described in the precedent chapter.

Interface states are therefore to be measured with a technique which must not be affected by the presence of the hysteresis, i.e. by the instability of the structure. A high density of states, as shown in fig.6 being generally present in narrow bandgap MIS structure, a pulsed HF-C-V curve has been plotted to avoid the drift due to the tunneling of carriers between semiconductor and insulator. This transient curve is identical to the HF C-V curve [24] as long as the surface potential will not reach $2\phi_F$. The lowest value that we have observed on SiON - InSb interface is $5 \times 10^{11} cm^{-2}-eV^{-1}$.
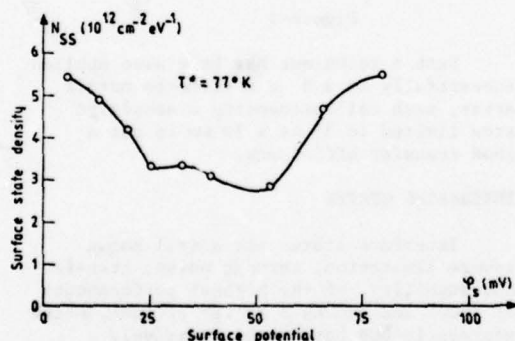
Figure 6 - Interface of an elementary SiON-InSb MIS cell

CONCLUSION

The analysis of performance limitations due to narrow bandgap semiconductors used as a substrate in IR imaging charge coupled devices and charge injection devices has been presented.

Improvement of the characteristics of these detectors is strongly dependent on the process and on the resulting insulator - semiconductor interface quality. Besides the type of dielectric to be selected, the question is to know which technology among thermal evaporation, chemical vapor deposition, molecular electron beam or even other methods, will allow to get over a new step in the high grade device fabrication.

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A SILICON CCD/NMOS PROCESSOR FOR InSb CID ARRAYS

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ABSTRACT: Current infrared systems are limited in performance by the relatively small number of detectors which can economically be included on the focal plane. Several technology development programs have been initiated to improve the performance of IR systems by making feasible the fabrication of IR focal plane arrays (FPAs) including orders of magnitude more detectors than is practical with present technologies. In the case of imagers (FLIR) for tactical applications, FPA's with several thousands of detectors can be combined with time-delay-and-integration (TDI) signal processing in serial-parallel scanned systems to give dramatic improvements in sensitivity.

One technical approach to the realization of FPAs is the use of an intrinsic detector array of charge injection devices (CIDs) coupled to a silicon signal processor chip. This approach requires many fewer interconnects than the one per detector of most hybrid approaches and additionally can be implemented with a less mature detector MIS technology than is required for monolithic intrinsic approaches.

This paper describes the development of a silicon signal processor for an on-focal plane application with a 16 x 24 element InSb CID detector array. The processor chip includes preamplifier, correlated double sampling (CDS), 16-element TDI and AC couple/DC restore circuitry for each of 24 detector channels. The parallel signals are combined in a 24 channel CCD multiplexer.

I. INTRODUCTION

Current generation infrared systems are limited in performance by the relatively small numbers of detectors, typically less than 200, which can economically be included on the focal plane. Several technology development programs have been pursued to make feasible the fabrication of infrared focal plane arrays (FPAs) having many more detectors than are presently practical. In the case of infrared imagers, or FLIR, for tactical applications, FPAs with several thousand detectors would provide dramatic improvements in performance.

As a result of the low contrast available for tactical infrared imagers, the staring mode of imaging commonly used at visible wavelengths

has difficulty in distinguishing between variations in detector responsivity and variations in scene irradiance. For example, since it is necessary to resolve apparent target temperature differences of less than 0.1°C, detector responsivity uniformity would have to be better than a few tenths of a per cent in the 3-5 μm wavelength band. Device uniformities of this order are simply not practical with available technologies. As a result, the mechanically scanned mode of operation - resulting in an effective AC coupling of the imager to the scene - is generally used for infrared imagers to avoid severe uniformity requirements for the detector responsivities. Two dimensional arrays operated in a serial-parallel scan mode can take advantage of time-delay-and-integration

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(TDI) signal processing to achieve enhanced signal-to-noise ratios and built-in redundancy protection against failure of a few detectors.

One approach to the realization of FPAs for serial-parallel scanned imagers is the combined use of an intrinsic IR detector array with an on-focal plane silicon IC designed to provide the desired signal processing functions for conditioning the raw detector information.[1] The development of charge injection device (CID) arrays fabricated on InSb has resulted in the potential for achieving background limited IR imager performance at detector sampling rates commensurate with tactical requirements.[2] The CID is an MIS structure in which IR-photon generated minority carriers are stored in potential wells which are created by means of external voltages applied to the gate electrodes. Read-out of the signal charge is typically accomplished by injecting the stored charge into the substrate and sensing the resulting current with external circuitry. The function of the silicon signal processor IC is to sense the detector signal and perform the necessary preamplification and the desired TDI processing for signal-to-noise enhancement.

The InSb CID/Si processor approach offers several advantages. It requires many fewer interconnects than the one per detector needed for most hybrid photo-diode approaches, and it is expected to have fewer frequency response problems than the hybrid arrays. In addition, the CID approach can be implemented with a much less advanced MIS interface technology than would be required for infrared CCDs. The disadvantages of the CID approach result from the relatively high capacitance of the detector output node and from the need to read the entire array into the silicon processor within every sample time (at least once per dwell time, in other words). The high output capacitance results in a small output noise voltage for a given noise on the charge packet. This means that the preamplifier on the processor must have a very low

input noise if the system is to be limited by the background shot noise on the charge packet. Read out of the entire array, which may contain many detectors, during each sample time means a relatively high output data rate for imager applications. This requires a wide bandwidth for the processor circuits (particularly the preamplifier), which makes low noise, low power performance even more difficult to achieve.

II. PROCESSOR REQUIREMENTS

This paper describes the development of a silicon signal processor designed to interface with a 16x24 element InSb CID detector array.[2] For the purpose of the signal processor technology development, a prototype system was assumed to be a horizontally scanned, 525-line TV-compatible FLIR. The focal plane was assumed to consist of ten 16x24 element CID arrays, with the 16 elements in the direction of scan for TDI, with an associated signal processor chip for each CID array. A complete list of the prototype system specifications appears in Table 1. This type of system was selected, in part, because it placed relatively stringent requirements on the signal processor circuits in terms of sampling rate and noise performance.

A processor implementation with silicon CCD/NMOS technology was based on the following considerations: 1) the operation of NMOS circuitry is enhanced at low temperatures[3], whereas that of bipolar circuitry is typically degraded[4], 2) the TDI function is easily implemented with CCD structures,[5] 3) CID control and signal sensing are facilitated using NMOS amplifier circuits which exhibit extremely high input impedances. Based on the prototype system specification the signal processor chip was configured to provide the necessary preamplification, TDI processing and multiplexing for 24 detector channels from each CID array. The block diagram in Figure 1 illustrates the components included in each channel and will be discussed in detail in the next section.

Scan	Horizontal Unidirectional (70% Efficiency)
Display Compatibility	525-Line TV (2:1 Interlace with 4/3 Aspect Ratio)
Detectors	10- 16x24 CID Arrays
Dwell Time	24 μs
Samples/Dwell	2 1/4
Background Rate (N_b)	3×10^9 Carriers/sec per Detector
Focal Plane Temperature	77°K
Power Dissipation on Focal Plane	1W

Table 1. Prototype FLIR System Specifications

The preamp is followed by a correlated double sampling (CDS) circuit[6] which suppresses kTC noise on the detector sense line and 1/f noise in the preamp. The signal from the CDS circuit is applied to the input of a CCD TDI consisting of a 16 stage charge transfer shift register which is connected to a 48 stage CCD TDI register through parallel transfer gates. Charge in the TDI register is advanced one stage each time the shift register is filled, thereby matching the oversampling rate of the detectors. The AC couple/DC restore operation is accomplished at the TDI output and the 24 channels are combined in a charge transfer output multiplexer. This configuration is a fully parallel implementation (necessitated by sampling rate considerations) of the focal plane processor concept discussed by Milton and Hess[1].
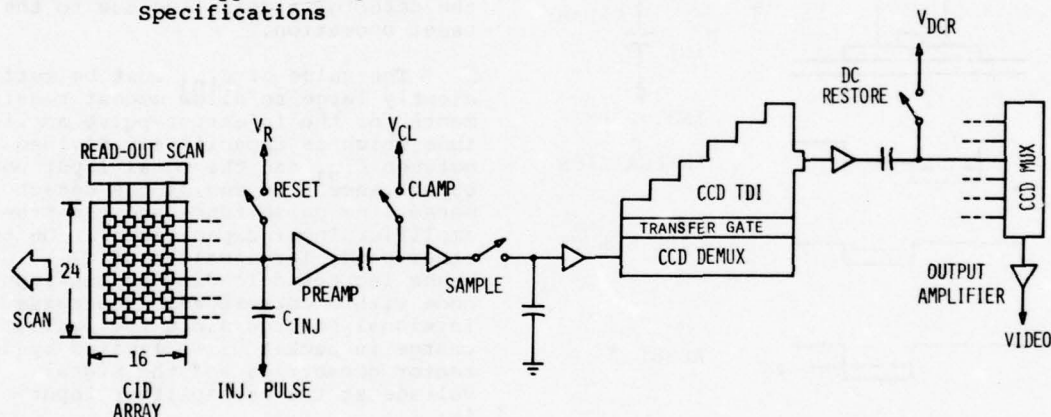
Figure 1. Block Diagram Showing the Components of the Silicon Processor Chip

The low noise preamplifier is an NMOS design with negative feedback employed for small signal gain and DC operating point stabilization. Significant aspects of the preamplifier design include: 1) low noise operation with the limited power budget required for on-focal-plane applications; 2) sufficient bandwidth and slew rate to allow settling of transients due to detector control pulses; 3) sufficient linear range to accommodate typical NMOS threshold voltage variations.

III. PROCESSOR DESIGN

The processor circuit is composed of six functional units, as can be seen in the block diagram of Figure 1: 1) detector signal line control, 2) preamplifier, 3) CDS, 4) TDI, 5) AC couple/DC restore, and 6) output multiplexer. In this section we discuss the details of the design considerations and resulting circuit configurations for each functional unit.

Detector Signal Line Control

Operation of the CID detector illustrating the detector control circuitry is shown in Figure 2. When a particular address line A_n is enabled by the read-out scan register, the integrated signal charge Q_S is transferred into the potential well beneath the CID electrode connected to the detector signal line. This causes a change in the signal line voltage proportional to Q_S, however the signal is not sensed at this time. Rather, the Reset Switch is closed briefly which sets the signal line voltage to the reference level V_R, and therefore the surface potential beneath the CID electrode to $\emptyset_R$. Shortly thereafter, an injection pulse is applied through C_{inj} which collapses the potential well and causes Q_S to be injected into the substrate.
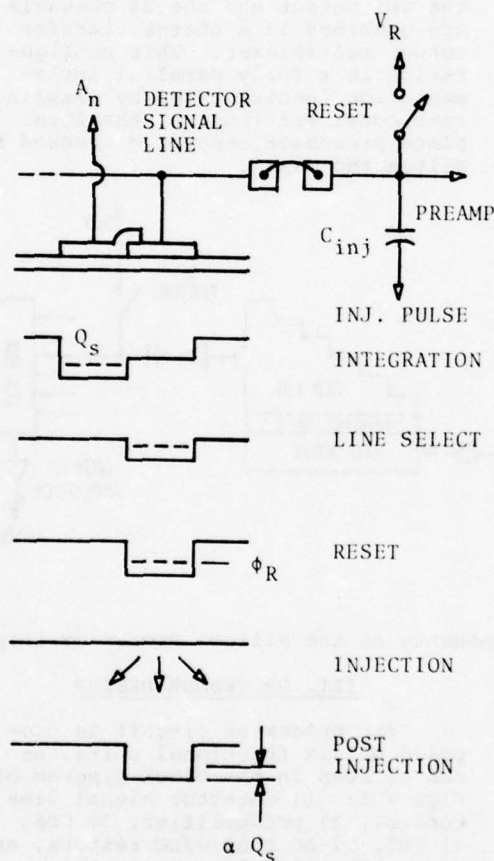
When the switching transients due to the injection pulse have settled out, the surface potential beneath the CID electrode, and hence the signal line voltage, will have changed by an amount proportional to Q_S. At this point the preamplified signal is sampled. The operation described above occurs synchronously with the operation of the CDS circuit (to be described later) in order to suppress the well known kTC noise on the detector signal line due to the reset operation.

The value of C_{inj} must be sufficiently large to allow modest requirements for the injection pulse amplitude which is capacitively divided between C_{inj} and the total input node capacitance (the sum of the detector sense line capacitance and the preamplifier input capacitance). On the other hand, large values of C_{inj} cause increased loading of the input node with a corresponding decrease in signal voltage since the maximum charge in packet Q_S is limited by detector geometries and the signal voltage at the preamplifier input is:

$$V_{sig} = \frac{Q_S\, C_O}{C_D(C_O + C_T) + C_O\, C_T}$$

where C_O is the detector electrode oxide capacitance, C_D is the depletion capacitance and C_T is the total signal line capacitance which includes the preamplifier input capacitance and C_{inj}. This signal attenuation results in a lower input referred noise requirement for the preamplifier in order to obtain background limited performance.

Figure 2. CID Operation by the Processor Chip Control Circuit.

Choice of design parameters for the Reset Switch transistor involves similar considerations. The W/L ratio must be sufficiently large to allow completion of the reset operation in the time allotted (50 ns) with reasonable control pulse amplitudes. However, the gate-drain capacitance adds directly to the total signal line capacitance C_T and a minimum gate width is desirable.

Low Noise Preamplifier

The low noise NMOS preamplifier is the most critical component of the silicon processor and consequently presents the most challenging design problem. Of the several configurations considered, the one shown schematically in Figure 3 appeared the most immediately promising in terms of meeting the design goals.
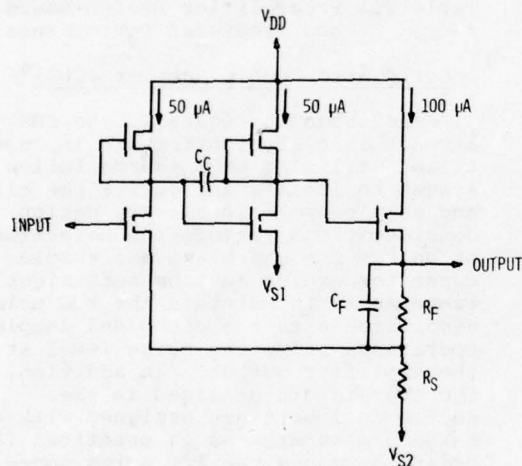
Figure 3. Schematic of the Preamplifier.

The circuit consists of a pair of cascaded inverters with a subsequent source follower stage which provides the low output impedance required for proper operation with the CDS circuit and negative feedback to the first stage for AC gain and DC operating point stabilization.

Although gain and bandwidth were important considerations in this design, the key trade-off is between noise performance and power dissipation,

the latter being extremely limited due to the constraints imposed by on-focal plane operation. The dominant sources of Johnson noise are the input transistor and the feedback resistor, R_s. The input referred Johnson noise generated in the input transistor is given by:

$$e_n = (8kT/3g_m)^{1/2} \quad V/Hz^{1/2}$$

The improvement in MOS transistor parameters at low temperatures is primarily due to the increase in surface mobility which results in an increase in g_m. Thus, on-focal plane operation of the processor chip at 77°K results in a decrease in input referred noise by a factor of 4-6 relative to 300°K operation.

The Johnson noise generated in the input transistor when operated in the saturation region is approximately given by:

$$e_n = (\frac{8kT}{3})^{1/2} (K' I_D \frac{W}{L})^{-1/4}$$

where $K' = 2 \mu s \, \epsilon_{ox}/t_{ox}$.

The drain current I_D is constrained by the limited power dissipation, and the W/L ratio by device area, photolithographic limitations, and short channel effects accompanying very small gate lengths. The value of R_s is limited by power dissipation and linear operating range considerations. The linear operating range must be sufficient to accommodate expected NMOS threshold variations, thus the amplifier output node must be capable of ± 4 volt swings about a nominal value. This results in a nominal 4 volt drop across $R_f + R_s$, thereby dictating the minimum drain current in the source follower stage. Since the ratio R_f/R_s determines the amplifier gain, a decrease in R_s requires the same percentage decrease in $R_f + R_s$ and results in an increase in the source follower drain current.

Assuming equal noise contributions from the input transistor and R_s, the design trade-offs can be accommodated (to first order) by the following:

1) Determine value of R_s based on

$$8kTBR_s = e_n^2$$

where e_n is the desired input-referred noise in volts/$Hz^{1/2}$ and B is an estimate of the preamplifier bandwidth.

2) Determine source follower drain current from a nominal 4 volt drop across $R_f + R_s$, with R_f determined by R_s and the desired gain.

3) Apportion the remaining supply current equally between the inverter stages and determine the W/L of the input transistor such that the Johnson noise component is equal to that due to R_s.

4) Determine whether the resulting design meets gain, bandwidth and area requirements. If not, increase e_n and repeat the procedure from 1).

The amplifier circuit obtained from the cycle described above may differ from design goals in noise performance, but furnishes an initial set of device parameters which can be further massaged to provide optimum performance.

Table 2 summarizes the design goals and the predicted performance of the final preamplifier design based on computer simulation with device models appropriate for 77°K operation. The design goal for input referred noise performance is based on the background rate given in Table 1, an estimate of the total input capacitance (8 pF) and a 4 MHz preamplifier bandwidth. The predicted preamplifier noise performance is the best effort based on circuit area restrictions imposed by a conservative estimate of ultimate chip dimensions. The preamplifier bandwidth is primarily determined by its transient response to the injection pulse which

occurs at a 1.48 MHz rate with an estimated duration of 85 ns. Proper operation of the CDS circuit requires that the preamp transients settle out within approximately 300 ns.[7] The preamplifier voltage gain is based on an estimate of the minimum value required to match the noise characteristics of the following stages (CDS, TDI, and multiplexer).

Parameter	Goal	Predicted
Input Referred Johnson Noise	$1.8nV/Hz^{1/2}$	$2.9nV/Hz^{1/2}$
Power Dissipation	4 mW	4.1 mW
Bandwidth	Optimum	4.3 MHz
Gain	Optimum	40

Table 2. Preamplifier Design Goals and Predicted Performance.

Correlated Double Sampler (CDS)[6]

As shown in Figure 1, the CDS circuit is a straightforward implementation utilizing NMOS source follower stages to isolate and buffer the clamp and sample operations. Key design considerations include the selection of values for the clamp and sample capacitors which must be sufficiently large so as to maintain the kTC noise associated with the clamp and sample operations below the noise level at the amplifier output. In addition, the transistors utilized in the source followers are designed with as large a gate area as is practical in order to reduce the $1/f$ noise generated in these devices.[8] Power dissipation in the CDS circuit is predicted to be 0.2 mW.

Time Delay and Integration (TDI)

The function of TDI is to increase the signal-to-noise ratio of the detector output by integrating the response of each detector element over a number of samples. In the case of a scanned array, consecutive samples from each detector element must be delayed before integrating to account for movement of the scene relative to the detector array. CCD

structures have been designed to delay and add the parallel signals from a number of serially scanned detectors to produce a serial video output with enhanced signal-to-noise.[5,9] For these applications the detector signals are continually loaded in parallel into a CCD register as the CCD is clocked with the result that the signal from each detector is added in the CCD to delayed signals from each other detector. The CCD clocks must be synchronized with the mechanical scan of the array.

The CID array effectively multi-plexes the detector signals. So the TDI structure must incorporate a de-multiplexer in order to permit parallel entry of the detector signals into the summing register. Over-sampling the detectors further com-plicates the design.

The TDI circuit for the processor chip is a CCD structure consisting of a 16 stage analog shift register coupled to a 48 stage TDI (summing) register through a set of parallel transfer gates. Although the detec-tors are sampled 2 1/4 times per dwell in the TDI (scan) direction, the de-tector spacing is adjusted to provide a 3:1 interleave for TDI. In other words, although the sampling rate is noninteger, the detector spacing and scan rate are such that every third sample occurs at the same "position" within each consecutive detector with respect to the image of a stationary point source.

Thus the analog shift register is filled with 16 samples at a 1.48 MHz rate (2 1/4 samples per 24 μs dwell time x 16 detectors in the TDI direction). These samples are trans-ferred in parallel into the TDI register as the 17th sample enters the shift register. The charge in the TDI register is advanced one stage before the next 16 samples are loaded via the parallel transfer, etc. The operation is identical with that obtained from three individual 16 stage TDIs having inputs com-mutated every 16 samples and outputs 3:1 multiplexed. The resulting data rate at the TDI output is 92.5 kHz.

Primary considerations in the design of the TDI structure include kTC noise of the input and output circuits and 1/f noise of the source follower output buffer. The CCDs in the shift register and TDI register were designed as two phase devices with ion implanted wells. In addition, floating diffusions were used in the shift register in order to match the pitch of the TDI register. In order to maintain acceptable CTE in the shift register, transfer gate lengths must be care-fully determined so as to minimize subthreshold leakage effects.[10] Figure 4 shows the channel stop and gate levels for the input circuit and first three stages of the CCD TDI structure.
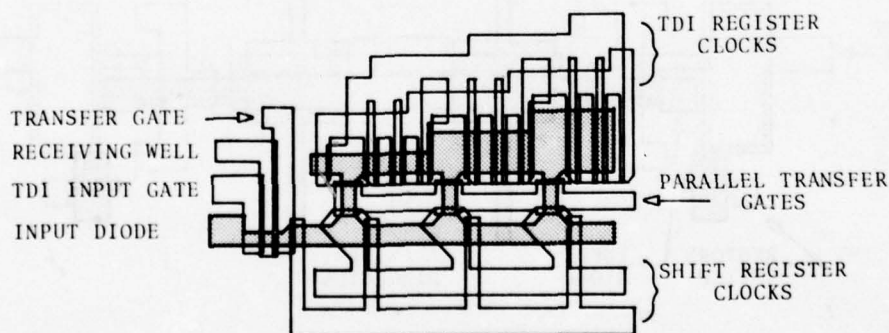
Figure 4. Channel Stop and Gate Levels For the Input Circuit and First Three Transfer Stages of the TDI Structure.

AC Couple/DC Restore and Output Multiplexer

DC restoration is accomplished by clamping the capacitively coupled multiplexer input via the DC restore switch shown in Figure 1. This operation removes all electronic offsets in the detector and processor circuits and, in addition, removes detector background response non-uniformities if a thermal reference is scanned by the detector array during the clamp.

The primary design consideration for the 24-channel output multiplexer is minimization of fixed pattern noise components commonly associated with CCD multiplexers due to MOS threshold voltage variations among the input circuits. A threshold-independent CCD input scheme has been described in the literature[11], however close examination revealed that it was not compatible with the AC couple/DC restore requirements. As a result, fixed pattern offsets introduced by the multiplexer will have to be "processed out" further down the signal processing chain.

A secondary design consideration involved matching the pitch of the multiplexer to the spacing of the processor channels. As in the TDI,

this was accomplished with floating diffusions. The dominant noise sources include kTC noise in the multiplexer input and output circuits and 1/f noise in the output buffer amplifier.

Channel stop and gate levels for the AC couple/DC restore circuit and the multiplexer input circuit/transfer cell are illustrated in Figure 5. The multiplexer is a dual channel, two phase, phase multiplexed structure which reduces the clock rate in each channel. The AC coupling capacitors are the rectangular structures just above the restore switch transistors.

IV. PROCESSOR FABRICATON AND TESTS

The silicon processor chip has been fabricated using a double level, self-aligned polysilicon gate CCD/NMOS process. A photomicrograph of the completed chip appears in Figure 6. The output multiplexer is the vertical structure in the center of the chip. The interconnecting diffusions can be seen extending between the input circuit/transfer cells.
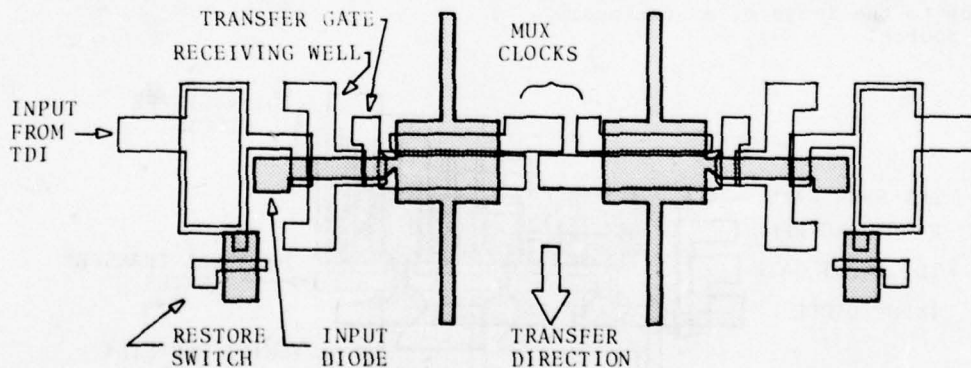
Figure 5. Channel Stop and Gate Levels for the AC Couple/DC Restore Circuit and Multiplexer Input Circuit/Transfer Cell.
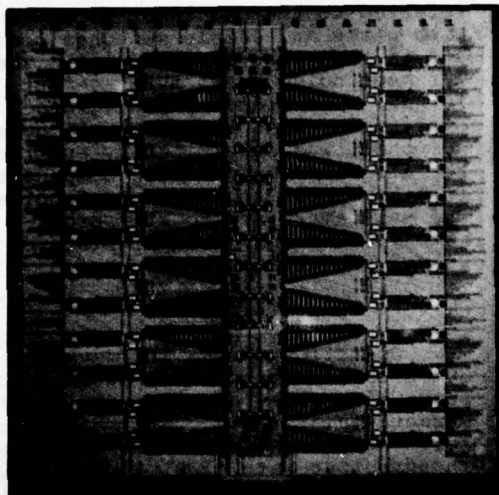
Figure 6. Photomicrograph of the
Processor Chip.

As in any IC design incorporating
moderately high circuit densities, a
key design problem is interconnection
of the various circuit components and
routing of control and signal lines.
Although this problem is somewhat
alleviated by the highly parallel or-
ganization of the processor circuits,
a considerable amount of effort was
expended in laying out the intercon-
nects, with special attention paid to
avoiding control line - signal line
crossovers.

An enlarged view of the chip
showing more component detail appears
in Figure 7. In addition to the pro-
cessor chip, a test chip was designed
and fabricated which includes each of
the major components as separately
bondable test structures. This allows
full characterization of each of the
individual components at 77°K with
small laboratory liquid nitrogen dewars
and considerably less equipment than is
required to support operation of the
full processor.

Preamplifier Test

The low noise preamplifier test
structure includes an additional source
follower stage as an output buffer
in order to drive the large parasitic
output capacitance associated with
packaging and testing. The measured
gain and noise performance of the test
structure at 300°K and 77°K are pre-
sented in Figure 8. Preamplifier
performance at 300°K agrees to within
expected limits with predicted per-
formance obtained from computer
simulations. Performance at 77°K,
however, is severely degraded. The
3 dB bandwidth is approximately
2 MHz and the input referred noise
level is 5 nV/Hz $^{1/2}$ as compared
with predicted values of 4.2 MHz and
2.9 nV/Hz $^{1/2}$ respectively.
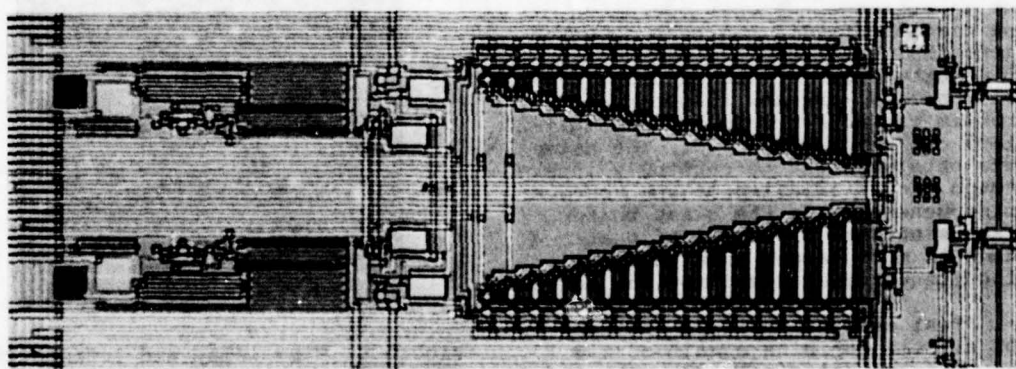
Figure 7. Enlarged View of the Processor Chip Showing Component Detail.

2-69
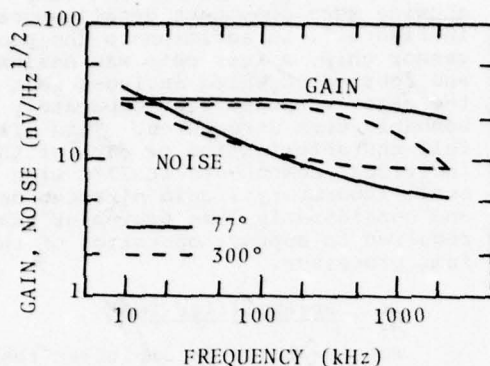
Figure 8. Voltage Gain and Input Referred Noise in the Preamplifier at 300°K and 77°K.

Further analysis indicates the source of the problem to be improper modeling of the temperature dependence of depletion load device parameters. This has resulted in a considerable decrease in DC drain currents in the first two stages, thereby causing an increase in noise and a decrease in small signal bandwidth and slew rate.

CDS Tests

The CDS test structure does not include an additional output buffer stage, and was tested at lower operating rates than required in the processor due to the large parasitic output capacitance. Proper operation of the circuit at 77°K has been observed. Since the depletion load devices in the source follower stages are externally biased, the low temperature problem (as observed in the preamplifier) can be circumvented. The noise data obtained must be carefully interpreted due to aliasing of the Johnson noise generated in the clamp buffer stage since the bandwidth of that stage is much larger than the operating frequency utilized for the tests.

Test results indicate that the CDS circuit exhibits a gain of 0.8 and operates satisfactorily with the required 50 ns clamp and sample pulse widths. The Johnson noise level

referred to the CDS input is measured with clamp and sample switches closed and is less than 30 nV/Hz$^{1/2}$. The 1/f spot noise is 65 nV/Hz$^{1/2}$ at 10 kHz. The wideband (integrated over the Nyquist interval) kTC noise component was determined by subtracting the aliased Johnson noise component from the total input referred noise and was determined to be approximately 60 μV rms, well within processor requirements.

TDI Tests

Operation of the TDI device at 300°K is illustrated in Figure 9 which shows time delay and integration of a rectangular pulse. The shift register clock rate is 1.48 MHz resulting in an output rate of 92.5 kHz. Figures 9a and b correspond to pulse durations of less than 48 TDI register clock cycles while the input pulse in Figure 9c is greater than 48 cycles long. Voltage gain through the TDI is nearly unity, and measured wideband noise is approximately 260 μV rms at room temperature.
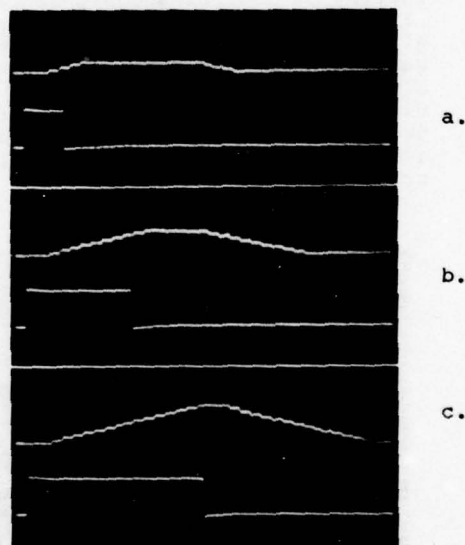
Figure 9. Time Delay and Integration of a Rectangular Pulse. (Top: TDI Output, .5V/div; Bottom: Input Waveform, .5V/div; Horiz: 0.1 ms/div).

Calculation of the predicted noise performance of the TDI indicates that it should be dominated by kTC noise resulting in a wideband output noise level of less than 100 μV rms. However, these calculations neglected the floating diffusion "bucket-brigade" type transfer as a potential noise source. An analysis of the bucket brigade transfer mechanism shows that the variance in the number of charges transferred at each transfer is [12]

$$\langle \zeta^2 \rangle = kTC_{FD}/q^2$$

where C_{FD} is the capacitance of the floating diffusion. The value of C_{FD} is calculated to be .069 pF from geometrical considerations, resulting in 106 noise electrons per transfer at room temperature. Since each consecutive charge packet contributing to a single TDI output charge packet experiences an additional transfer through a floating diffusion, the resulting variance on the output charge packet is

$$\langle \zeta_{out}^2 \rangle = \langle \zeta^2 \rangle [1+2+3+\cdots 16] = 136 \langle \zeta^2 \rangle$$

Since adjacent charge packets in the shift register are separated by two interleaved packets in the TDI register, a strong correlation will exist between charge packets Q_n and Q_{n+3} resulting in peaks in the noise spectral density at odd multiples of $f_{clock}/6$.

The expression for the single sided noise spectral density as measured at the TDI output is [12]

$$S(f) = \frac{2}{f_c} \left(\frac{q}{C_{out}}\right)^2 \langle \zeta_{out}^2 \rangle (1-\cos 6\pi f/f_c)$$

where f_c is the TDI register clock rate and C_{out} is the value of the output node capacitance. The sinx/x aperture function of the sample and hold output has been neglected. Inserting the appropriate numerical values (C_{out} = 0.7 pF, f_c = 92.5 kHz) yields

$$S(f) = 1.73 \times 10^{-12} (1-\cos 6\pi f/f_c).$$

Figure 10 compares the noise spectrum measured at the TDI output for normal operation with the expression above, and also shows the output circuit kTC noise level which was measured by disabling the TDI input circuit.
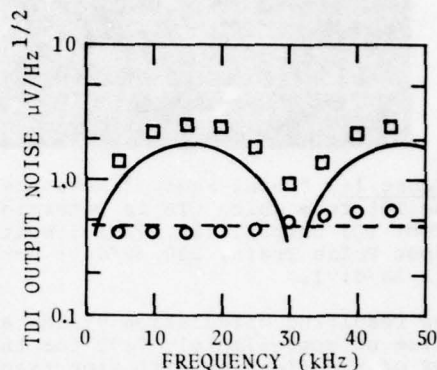
Figure 10. TDI Output Noise Spectrum. (Solid Line: Theoretical Transfer Noise, Dashed Line: Predicted kTC Noise, Measured values are indicated by squares and circles, respectively).

Figure 11 illustrates the "point source" response of the TDI. This is obtained by application of a properly synchronized 16-unit pulse train in order to integrate all 16 samples into a single charge packet. (Note that in actual operation, a point source would result in a TDI output signal which is 3 cycles in duration, due to oversampling of the detectors.) The second pulse seen trailing the main output in the oscillograph is due to CTE effects in the shift register caused by the floating diffusions which interconnect CCD transfer cells. Using only first order terms, the ratio of the charge in the signal packet to that in the trailing packet is

$$\frac{signal}{error} = \frac{\sum_{n=1}^{16} (CTE)^n}{\sum_{n=1}^{16} (1-CTE)^n}$$
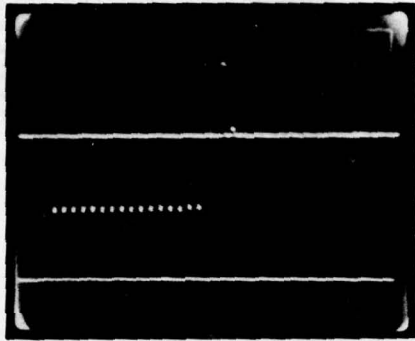
Figure 11. "Point Source" Response of the TDI from which CTE is Determined. (Top: TDI Output, 200 mV/div; Bottom: Input Pulse Train, 200 mV/div; Horiz: 0.1 ms/div).

The resulting calculation yields a value of approximately 0.99 for the CTE of the floating diffusion transfers.

Proper operation of the TDI device has been observed at 77°K, although a detailed analysis has not yet been performed due to excessive crosstalk among signal and control lines in the cables interconnecting the device and the test equipment.

Multiplexer Tests

Operation of the 24 channel output multiplexer at 300°K is demonstrated in the oscillograph in Figure 12 where a test signal has been applied to input number 13. Voltage gain through the device is approximately 0.14 due to a 5:1 mismatch between input and output capacitances (necessitated by the phase multiplexed design) and a voltage gain of 0.7 in the multiplexer output buffer amplifier. Figure 13 is an expanded view of the output waveform illustrating the fixed pattern noise component due to threshold voltage variations among the input circuits. Except for a large transient induced by the parallel transfer pulse (believed to be spurious coupling in the experimental set up), the fixed pattern variations are within an input

referred range of $\pm$ 100 mV. This is at least a factor of two larger than the worst case expected, and further investigation is required to resolve the discrepancy.
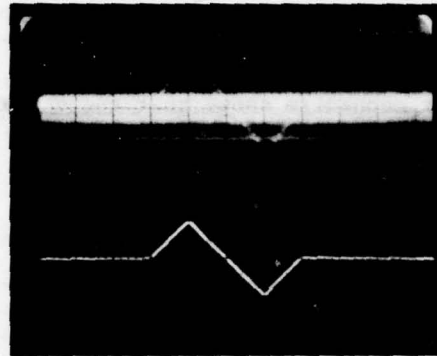
Figure 12. Multiplexer Response (Top: Multiplexer Output, 0.1V/div; Bottom: Signal Applied to Input Number 13, 1V/div; Horiz: 0.2 ms/div).
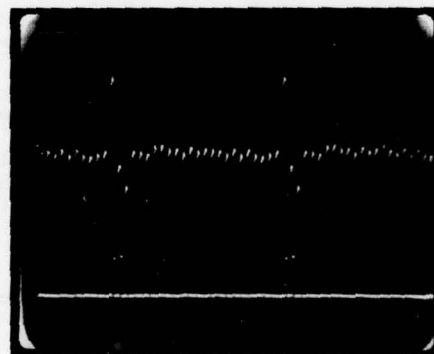
Figure 13. Detail of Multiplexer Response Showing Fixed Pattern Noise Component. (Top: Multiplexer Output, 0.1V/div; Bottom: Parallel Transfer Pulse, 10V/div; Horiz: 5 μs/div).

As in the TDI, the primary thermal noise source in the multiplexer is due to the bucket brigade transfers in the floating diffusions. CTE in the multiplexer is slightly better than in the TDI due to larger gate lengths which reduces the drain dependence of the subthreshold leakage.

The multiplexer has not been tested at 77°K, although operation of the output buffer amplifier is expected to be degraded due to the use of fixed bias depletion loads.

Processor Tests

Preliminary tests of the processor chip have been performed and have confirmed proper interconnection of the components. Although detailed tests to evaluate the performance of the processor have yet to be accomplished, preliminary evaluation of a single processor channel at 300°K has been accomplished by interconnecting the individual preamplifier, CDS and TDI test structures on the test chip.

The input waveform for these tests was generated with an external clamp/sample circuit in order to provide a reference level for the CDS clamp operation. Although the test structures utilized were on the same chip, they were interconnected externally, and the input sample rate was reduced to 148 kHz to accommodate parasitic capacitance. Figure 14 shows the input signal, CDS output and TDI output waveforms corresponding to the maximum signal amplitude for linear operation of the TDI. The voltage gain through the preamplifier and CDS circuits is approximately 10
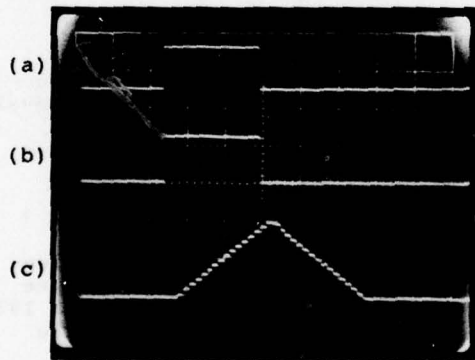
Figure 14. Response of the Processor Channel Test Circuit. (a) Input Signal, 50 mV/div. (b) CDS Output, 500 mV/div. (c) TDI Output, 500 mV/div. Horiz: 2 ms/div.

due to the additional source follower in the preamplifier test structure and high bias levels in the CDS source followers required to obtain sufficient bandwidth.

Figure 15 shows the CDS and TDI output waveforms when the test signal is reduced in amplitude by 40 dB. The smeared appearance of the TDI output waveform is due to droop in the sample and hold circuit connected to the TDI output in order to reduce clock feedthrough. This effect is shown in the expanded portion of the TDI output waveform. The wideband noise measured at the TDI output is approximately 520 µV rms and is generated within the TDI structure (confirmed by shortng the TDI input to ground). The primary noise component is due to the bucket brigade transfer discussed earlier, as was evidenced by observation of the characteristic noise spectral density function for that noise source. The resulting dynamic range observed in the TDI is 65 dB (peak signal to rms noise).
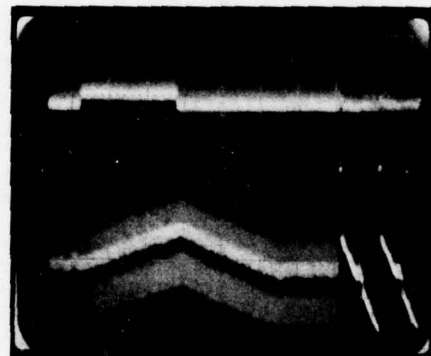
Figure 15. Response of the Processor Channel Test Circuit with Input Waveform Attenuated by 40 dB. (Top: CDS Output, 20 mV/div; Bottom: TDI Output 10 mV/div; Horiz: 2 ms/div, 100 µs/div)

The wideband noise measured at the CDS output is approximately 430 µV and is primarily due to aliasing of Johnson noise components in the preamplifier and CDS circuits.

V. DISCUSSION

The noise performance of the processor channel test circuit is dominated by transfer noise generated in the TDI input shift register. This will remain the dominant thermal noise source in operation of the processor chip. Although the gain of the preamplifier and CDS circuits is expected to increase by approximately a factor of 3, the noise in those circuits is expected to decrease by about the same amount due to a decrease in the noise aliased into the Nyquist interval. Input sample rates of from 500 kHz to 700 kHz should be possible at 77°K, with an input referred wideband noise level of approximately 14 μV - a factor of three higher than that required for background limited performance.

The transfer noise in the TDI can be improved by decreasing the capacitance (i.e, the area) of the floating diffusions. Although the geometry of the present design could be modified to reduce the area of the floating diffusions by a factor of 2 or 3, reduction by a factor of 20 to 30 is required to suppress the transfer noise level below the kTC noise generated in the TDI input and output circuit. The motivation for employing the floating diffusion interconnect was the reduced clock rate in the input shift register. This structure can be realized with a CCD shift register having the same cell pitch as in the TDI register and operating at a clock rate 48 times that in the TDI register, with the input circuit entering a charge packet every 3 clock cycles. The resulting clock rate in the input register is 4.5 MHz. Although this approach results in the potential for increased clock to signal crosstalk, it appears, in retrospect, to represent a lower overall risk in terms of processor noise performance.

Two key problem areas recognized in the early stages of this development program were related to preamplifier noise performance and multiplexer fixed pattern noise. Their status, in this regard, has not changed. The problem encountered with the depletion load devices in the preamplifier are quite disappointing, but hardly insurmountable. In addition, new amplifier configurations are currently under study which show much higher potential for low noise, low power operation than the circuit described here. Fixed pattern offsets in multi-channel CCDs have been problematic to designers for years. The realities of tactical FLIR applications dictate an eventual analog-digital interface, and thus the possibility for "processing out" fixed pattern variations in the digital processor. The main requirement is that the fixed pattern offsets be sufficiently small - say, a few percent of the peak signal - so as not to degrade processor accuracy when the scene contrast is low.

In summary, although unexpected problem areas have been encountered, it is felt that low risk solutions are available. The result of this silicon processor development is a confirmation of the applicability of analog NMOS/CCD circuits to on-focal plane signal processors for intrinsic CID detector arrays. Further work in this area is unquestionably required, in order to more carefully analyze the performance of the present processor configurations and to define the optimum architecture for future processors.

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Planar GaInSb CCDs

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In recent years there has been a major effort in developing CCD imagers in narrow-bandgap semiconductors. The purpose is to develop high performance, self-multiplexed area imagers in the IR which are the analog of Si CCD imagers in the visible region. CCD operations have been reported in many non-silicon materials, including Ge, InSb, GaAs, and HgCdTe. In this paper we report for the first time the successful fabrication and testing of CCDs in a III-V ternary epitaxial layer, GaInSb. The cut-off wavelength of GaInSb layers can be compositionally tuned from $1.7\mu m$ at 77K. The development of CCDs on alloy semiconductor epitaxial layers offers the potential of more versatile device structures to tailor to different application requirements. For example, the GaInSb/GaSb CCD imager can be operated in the backside-illuminated mode without thinning the GaSb substrate. This is because the energy bandgap of the GaSb substrate is greater than that of the GaInSb epitaxial layer. The backside-illuminated feature is essential for high density, high resolution, mechanically rigid IR area imagers.

The CCDs were fabricated using a planar technology on single crystal, n-type GaInSb layers which were grown by liquid phase epitaxy (LPE) technique on GaSb substrates. The carrier concentration in the layer was typically $\sim 10^{14}$ cm^{-3}, sometimes as low as $\sim 5 \times 10^{13}$ cm^{-3}. The CCD test structure is a four-phase, overlapping-gate, surface channel, 4-bit (19 transfer gates) shift register. The input/output diffusion were formed by ion-implantation. The gate insulator is formed by low temperature ($\sim 300°C$) chemical vapor deposition of SiO$_2$ doped with NH$_3$. The electrodes were formed by thermal evaporation of Al. The CCD was tested under low background at 195K. Initial results show that the charge transfer efficiency of 0.97 has been obtained.

In this paper we also report the results of MISFETs fabricated on the GaInSb epitaxial layers. The MISFETs are essential for incorporating on-chip signal processing functions. It has been measured that the GaInSb MISFET characteristics follow the ideal square law relation of FETs over the temperature range of 20-300K. The hole mobility in the inversion layer was 180cm^2/v-sec at 195K. The threshold voltage was found to vary inversely as the operating temperature. Detailed discussions on these results will be presented.

(The full paper was not available in time for publication in the proceedings.)

GaAs CCD WITH HIGH TRANSFER EFFICIENCY

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ABSTRACT. A Schottky barrier gate GaAs CCD has been successfully operated with high transfer efficiency. This CCD structure in GaAs offers the potential of ultra high speed signal processing devices as well as near-infrared and visible imaging CCD's.

1. INTRODUCTION

Over the past few years, vigorous development effort has brought silicon charge coupled device (CCD) technology to the point where widespread applications in signal processing and imaging have become practical. The technological maturation of Si CCD's has also brought the realization that there are certain limitations, particularly in speed and charge storage time, that could not be overcome. GaAs and related III-V compound semiconductors show promise for overcoming the fundamental limitations on CCD performance imposed by silicon material properties. Research on GaAs CCDs has, however, been hampered by the persistently high surface state densities and instability in GaAs MIS (metal-insulator-semiconductor) structures. Non-MIS gate CCDs have been previously proposed[1]. A new GaAs CCD structure employing Schottky barrier gates has recently been demonstrated.[2,3] Charge transfer efficiency in excess of 0.999 per transfer has been measured on this device,[4] making it the first CCD in a material other than silicon in shich high transfer efficiency has been demonstrated. Improved performance in GaAs based CCD is expected because of better material properties and greater flexibility in device design.

The 4 to 5 times larger low-field mobility of electrons in n-type GaAs over silicon is the principle contributor to higher speed GaAs devices. In a buried channel CCD (such as the Schottky gate GaAs CCD) which is designed for the "peristaltic" mode of operation, the higher GaAs electron mobility results in higher speed transfer from one gate to the next. High transfer efficiency at speeds well in excess of 1 GHz is possible. A second consequence of the high mobility for high speed CCDs is the bandwidth of the on-chip read-out amplifier. In order to operate a CCD at sample rates approaching 1 GHz, the bandwidth of the on-chip amplifier must be several GHz. This is the principle reason that silicon CCDs have not been operated at much more than about 200 MHz. The bandwidth (or f_τ) of on-chip silicon FETs (N-MOS) is about 500 MHz. Reduced geometry N-MOS or D-MOS devices exhibit $f_\tau \simeq 1$ GHz. Compare this with a typical Schottky gate GaAs FET for which $f_\tau = 15$ GHz.

An additional subtle, but highly important, advantage in favor of GaAs for high speed devices is the availability of semi-insulating GaAs which can be used as the substrate in a GaAs CCD. Incorporation of this material into the CCD design reduces power dissipation at high frequency, thus making the device more practical and reducing the design problem of on-chip clock drivers. It reduces the output-node capacitance, thus increasing charge detection sensitivity. Furthermore, since there is no p-n junction between the active charge transport layer and substrate, a "natural" channel-stop is formed by extending the CCD gates beyond the active layer onto the substrate. This feature can be seen in the photograph of the device (Fig. 1).
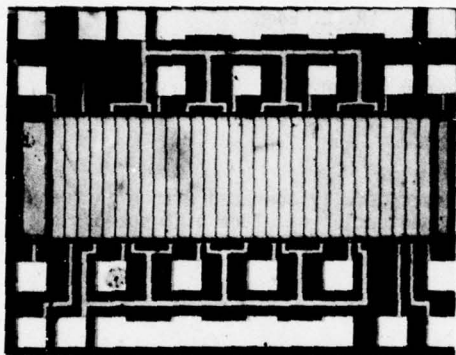
Fig. 1 Ten-cell, 3-phase Schottky gate
GaAs CCD

The availability of heterojunction
technology in III-V compounds makes pos-
sible another related class of devices
with significant performance advantages.
The ability to choose the material energy
gap (by the alloy composition) permits
selection of the desired optical response
in imaging devices. Forming a hetero-
junction of this optical absorber and a
wide bandgap alloy in which charge trans-
port takes place results in a CCD with
exceptionally low dark current. Low dark
current results from low intrinsic car-
rier concentration (n_i) in wide bandgap
alloys. Since intrinsic carrier concen-
tration and energy gap are related expo-
nentially, a few tenths of an electron
volt difference in energy gap results in
orders of magnitude difference in intrin-
sic carrier concentration. For example,
GaAlAs with Eg = 1.7 to 1.9 eV will have
10^6 to 10^7 times smaller intrinsic
carrier concentration than silicon
(Eg = 1.1 eV). This results in imaging
devices or memory devices with room tem-
perature charge integration/storage times
of hours rather than fractions of a sec-
ond.

Still further advantages accrue from
the insuator-free (non-MIS) device struc-
ture. These devices are a naturally
antiblooming structure since charge in
excess of a full well is removed as a
gate current and does not overflow into

adjacent wells. In addition, GaAs
Schottky gate CCDs are much more radia-
tion resistant than Si-CCDs, both in
terms of photocurrent (because the deple-
tion region and diffusion lengths are
small) and permanent degradation, since
there is no oxide to charge up.

Finally, a highly desirable feature
in a high speed CCD technology is availa-
bility of a compatible high speed inte-
grated circuit (IC) technology, so that
not only the read-out amplifier, but
clock drivers and ancillary electronics
can be integrated on chip. Such compati-
bility does not exist in silicon technol-
ogy. For example, Si-high speed technol-
ogy (bipolar-ECL) and CCD technology
(N-MOS) are not compatible processes,
while GaAs Schottky barrier gate CCD and
IC technologies are completely compati-
ble.

2. OPERATING PRINCIPLES

The basic structure of the device is
shown in Fig. 1. The spacing between the
gates is of the order of one micron. Three
gates are required to handle one packet
of charge. The energy band diagram for a
cross-section of the device under a gate
is shown in Fig. 2. The operation of the
device can be understood by a study of
this figure. Initially (at thermal equi-
librium), with no bias applied, the n-
layer is partially depleted from both
sides due to the built-in junction poten-
tials. When the maximum (negative)
"push-clock" voltage is applied to the
gate, the minimum potential in the chan-
nel is raised so that all the mobile
electrons are removed to the adjacent
gate. Biasing the output ohmic contact
to the layer positively, results in the
mobile charges being quickly "pumped" out
of the device. As the push-clock bias is
reduced to zero, the potential maximum
returns to a large positive value which
corresponds to an empty well. This well
is then ready to store charge created by
photogeneration, injection or thermally
generated dark current. The potential
distribution for a well partially filled
by any of these means is also shown. The
completely filled well is indistinguish-
able from the thermal equilibrium condi-
tion. The device will remain in a state
of non-equilibrium until the thermal gen-

eration of carriers has restored equilibrium. During the period of non-equilibrium, CCD operation is possible. The period of charge storage is determined by the thermal generation rate for carriers which is proportional to the intrinsic carrier concentration, n_i:

$$\left(\frac{dn}{dt}\right)_{Thermal} = n_i/\tau_e$$

where τ_e is the effective generation lifetime. The fill time for a bucket is the time required to restore the electron concentration to the equilibrium (donor) density, N_D, or:

$$T_{Fill} = \frac{N_D \tau_e}{n_i}$$

for GaAs, $\tau_e \simeq 10^{-8}$ sec.

The potential minima in the channel are, thus, representative of the status of a well. This is analogous to the silicon CCD case, and the charge transfer scheme is identical to that required for a buried channel Si-CCD. Figure 3 shows the result of injecting three equal amplitude pulses into the device through the input diode and shows the high transfer efficiency in the GaAs CCD. This result is obtained without the use of background change as is common even in buried channel silicon CCDs. The measured transfer efficiency is 0.9994.

Fig. 3 Output of GaAs CCD with 3 equal amplitude input pulses. No background charge. CTE > 0.999/transfer

In the Schottky gate CCD, there is no insulator interface, so that all the applied potential drop occurs in the semiconductor giving a somewhat increased top-end in the dynamic range over conventional CCDs. More significantly, without a "fat-zero" or bias charge, the low end of the dynamic range should be at least as good as a buried channel Si-CCD (or even better, since the thermal generation rate is lower). The minimum detectable signal can be calculated using a simple model which assumes that the signal charge is detected as a voltage change, ΔV, on the total output capacitance, C_O

$$\Delta V = \frac{Q_S}{C_O}$$

where Q_S is the signal charge, C_O is the CCD output capacitance, and C_g is the amplifier input capacitance. The minimum detectable signal is defined as $\Delta V = e_n$, where e_n is the equivalent input noise voltage of the CCD output amplifier (FET). The minimum detectable number of electrons, N_O, is, then;

$$N_O = \frac{(Q_S)_{min}}{q} = \frac{e_n(C_O + C_g)}{q}$$

Thus, the limit to the detection of charge is set by the total equivalent input capacitance and the amplifier equivalent input noise voltage. The device noise is limited by the detection noise

Fig. 2 Potential profile for Schottky barrier gate CCD with semi-insulating substrate.

when reset amplifier noise can be eliminated (for example, with floating gate detection) and when input noise can be ignored (for example, with optical input).

For GaAs FETs with $1 \mu m$ long, $25 \mu m$ wide gates, $e_n \simeq 1 nV/\sqrt{Hz}$ and $C_g = .033 pF$. If the CCD output capacitance is $.02 pF$, then a train of pulses with 1ns spacing (bandwidth = 500 MHz) can be detected with $N_0 \simeq 7$ electrons. It is the extremely small total capacitance and the low FET noise which provides this capability. This level of performance has been demonstrated in a similar situation which arises in the design of an optical communication receiver using GaAs FET devices[6]. In this case, a low-capacitance avalanche photodiode is connected to a GaAs FET amplifier connected in the trans-impedance mode. N_0 was measured to be 347 electrons and was limited by Johnson-noise in the feedback resistor.

3. APPLICATION TO HIGH-SPEED SIGNAL PROCESSING

At high frequencies, such as radar IF frequencies, signal processing functions such as correlation are performed on Surface Acoustic Wave (SAW) devices using transversal filter implementations. This class of functions as well as others, could in mnay instances be advantageously performed monolithically on a semiconductor material. The obvious reason for this is that the element of tunability is achieved (SAW) devices are fixed function devices since the signal delay is proportional to the ultra sound propagation velocity). Also the capability to perform complete signal processing functions on chips is attractive from a systems/cost point of view. Utilization of CCDs to perform these functions at high frequencies (>10 MHz) has not been practical due to the limitations in Si CCDs discussed. GaAs CCDs offer the prospect for devices with SAW type bandwidths, while maintaining the flexibility of clock controlled propogation delay. CCD implementation of transversal filters requires the use of floating gates. In a non-MIS CCD, since overlapping gates can not be used. The simplest implementation of floating gates is dc coupling through a high impedance. Using this technique the form "sense" gates of the ϕ_3 electrodes in the GaAs CCD of Fig. 1, while ϕ_1 and ϕ_2 are clocked in the normal manner, a binary tap-weighted transversal

filter was constructed as shown in Fig. 4. To obtain a good main-peak to side-lobe ratio, a 7 bit Barker code[5] was used. Seven of the available nine ϕ_3 electrodes were connected with this code. Thus, (+) and (-) buses were created and connected to the current-mode amplifiers to sense the displacement currents. The difference of these two signals (obtained in a third differential amplifier) is then the correlated output. In Fig. 4 the expected position of the correlation peak relative to the input pattern is indicated. Fig. 5 is an oscilloscope photograph of the input and output and shows the resulting correlation. Most of the clutter is due to the clock feedthrough and could be easily eliminated with a sample/hold circuit. The expected peak-side lobe ratio in a 7 bit Barker code is 16.9 dB.

Of course, the floating gate concept can also be used with split electrodes for analog functions as well as to make floating gate detection amplifiers. A further extension of the transversal filter concept is a pseudo-noise (p-n) sequence correlator. A block diagram of this device is shown in Fig. 6. This device is a binary weighted transversal filter in which the tap weight assignments are altered at will and rapidly by FET switches. The useful realization of such a device requires high speed on-chip logic. The compatibility of the rapidly developing GaAs IC technology[6] with the CCD described here makes devices such as the p-n sequence correlator feasible.

4. CONCLUSION

The recently demonstrated GaAs CCD and GaAs IC technology are compatible for integration of CCD, digital, and analog functions on a single chip which together make possible a powerful new class of high-speed signal processing devices.
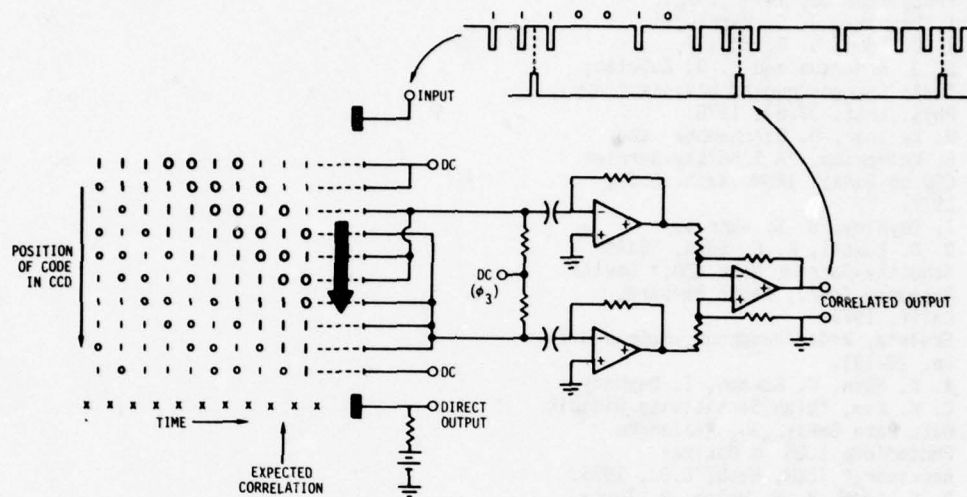
Fig. 4   GaAs CCD Transversal filter (floating gate)
demonstration scheme using 7-bit Barker code
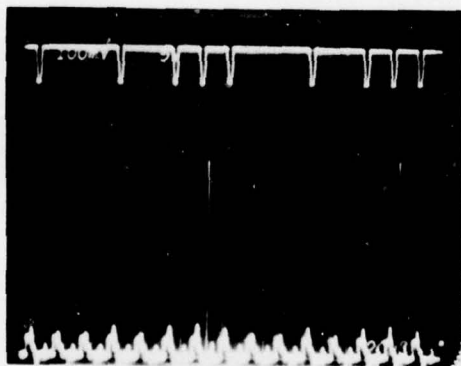
Fig. 5   Correlation output from GaAs
CCD Transversal filter
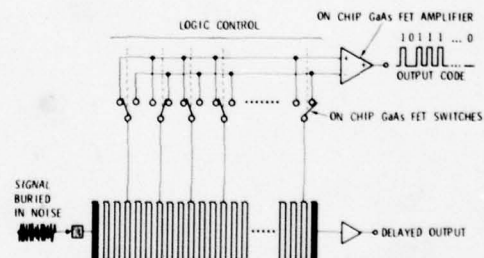
Fig. 6   High speed adaptive p-n sequence
correlator

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CCD ANALOG ADAPTIVE SIGNAL PROCESSING*

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ABSTRACT

A CCD Adaptive Signal Processor is described which uses the "clipped-data" least-mean-square (LMS) error algorithm to optimize the selection of tap weights in a CCD filter. The filter is comprised of a basic linear combiner formed with a nondestructively tapped CCD analog delay line and electrically reprogrammable MOS analog conductances as the tap weights. Two methods of varying the analog conductance are discussed: (1) variable V_{GS} with fixed threshold voltage V_T and (2) variable V_T with fixed V_{GS}. The former is performed with a CCD bidirectional charge control weight adjustment, whereas the latter is accomplished with MNOS memory transistors. To demonstrate the feasibility of adaptive analog signal processing a 2-tap weight CCD adaptive filter is described and experimental results presented. Also presented is some discussion of the effort to construct a 16-tap all-monolithic CCD adaptive filter chip. Applications include optimum filtering, prediction, noise cancellation, and system modeling.

1.0 Introduction

The history of adaptive signal processing might well begin with the introduction of the least squares estimation theory by Gauss[1] and Legendre.[2] Gauss introduced this technique to solve a large number of redundant equations to extract the "most probable values" of certain astronomical parameters. Modern adaptive filter theory begins with the work of Wiener[3] and Kolmogorov[4] on the prediction and filtering of stationary time series. The Wiener/Kolmogorov work provided the basic design criteria for optimal linear filters to suppress noise, perform signal prediction, and smooth statistically stationary signals. Kalman and Bucy[5] extended the work of Wiener and Kolmogorov to consider the design of time-varying filters for nonstationary signals with a priori information regarding the signal statistics. The so-called Kalman filter represents a recursive solution of Gauss's least-square estimation problem in which the computational benefits of modern digital computers are used to advantage.[6]

Adaptive filters are a class of "learning machines" in which the filter design (weight or parameter adjustments) is self-learning and based upon estimated (measured) statistical characteristics of the input and output signals. Adaptive filtering based on a recursive

algorithm (correlation-cancellation loop) was employed in the RF antenna field in the 1950's.[7] Two groups, working independently, developed techniques for adaptive interference or clutter cancelling. One group worked on radar IF sidelobe clutter cancellers[8] with optimization achieved by an algorithm that maximized a generalized signal-to-noise ratio.[9] The other group worked on a self-optimizing array for control systems based on sampled signals and a least-mean-square (LMS) error algorithm.[10] These two adaptive algorithms, although arrived at with different approaches and different objectives, are nevertheless very similar since both derive their adaptive parameter adjustments by sensing the correlation between input signals. Thus, both algorithms use the covariance matrix describing the system inputs and both algorithms converge toward the optimum Wiener/Kolmogorov solution. In this paper, the LMS adaptive algorithm developed by Widrow and Hoff[11] in 1959 with modifications by Moschner[12] in 1970 is used.

The general form of an adaptive filter is limited by practical considerations since the inversion and storage of large matrices of data requires a sizeable volume of computer space and real-time signal processing is difficult to achieve. The iterative LMS algorithm requires very little computer time or

memory and the algorithm is suitable for real-time processing of large amounts of data. With this algorithm the statistics of the signals are not measured explicitly to design the filter but, instead, through a recursive algorithm, the weight adjustments are made automatically with the arrival of each new data sample. Thus, the LMS algorithm allows the realization of an adaptive filter which can be used in real-time signal processing applications and may be implemented with analog circuit techniques. The CCD analog adaptive filter to be discussed here uses the "clipped data" LMS algorithm to allow ease of monolithic chip implementation with little sacrifice in system performance.

2.0 Analog Adaptive Filter Using the "Clipped Data" LMS Algorithm

Figure 1 illustrates a block diagram of an adaptive
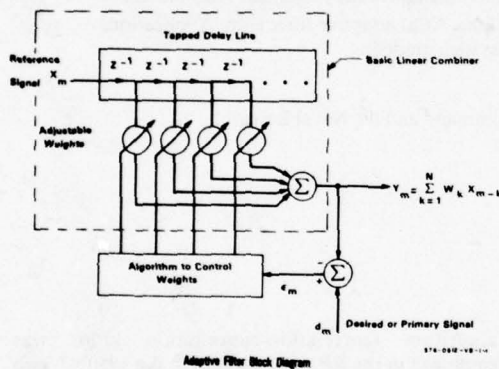
Figure 1. Adaptive Transversal Filter

filter. For sampled-data input signals, an error is formed at each clock according to the expression

$$\epsilon(m) = d(m) - y(m) \tag{1}$$

where d is the desired input, m is the clock index, and y is the weighted sum of the past N inputs, with N the length of the delay line. The error is used as the input to the algorithm which in turn adjusts the weight at each tap location to minimize the mean-square error.

The "clipped data" algorithm changes the weight of each tap location according to the equation

$$W_i(m+1) = W_i(m) + 2\mu\epsilon(m) \, \text{sgn} \, X(m) \tag{2}$$

$$= W_i(o) + 2\mu \sum_{k=1}^{m} \epsilon(k) \, \text{sgn} \, X_i(k)$$

where i is the tap location, μ is a constant which determines stability and convergence rate, ϵ is the instantaneous error defined by equation 1, X is the tap output, and sgn is the sign function. Equation 2 indicates that the algorithm retains full linearity of the error but requires a multiplier and integrator at each tap location. The multiplier is actually a branch operation which checks the sign of X and on this basis adds or subtracts the quantity $2\mu \, \epsilon(m)$ from the current tap weight to form the new weight value.

2.1 Analyses of Clipped Data LMS Algorithm for a 2-Tap Weight Adaptive Filter

In this section an analysis of a 2-tap weight adaptive filter using the clipped-data LMS adaptive algorithm is presented. Figure 2 illustrates a block diagram of the
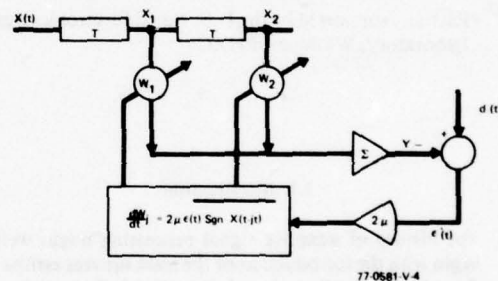
Figure 2. A 2-Tap Weight Adaptive Filter with Clipped Data LMS Algorithm Control

element to be analyzed with an input composed of a sinusoidal signal in the presence of white noise. The primary signal may be written as

$$d(t) = d_o \cos(\omega t + \phi) \tag{3}$$

where ϕ is the relative phase shift with respect to the signal at tap 1. The tapped signals are,

$$X_1(t) = X_o \cos(\omega t) + n_1(t) \tag{4}$$

$$X_2(t) = X_o \cos[\omega(t - T)] + n_2(t)$$

where T is the time delay between tap positions, and $n_1(t)$ and $n_2(t)$ are uncorrelated noise sources at the

tap positions. We will use a continuous time analysis in this section to illustrate the performance of the 2-tap weight adaptive filter. For continuous time the following expression for the weight factor, W, can be written

$$\frac{dW}{dt} = 2\mu P - 2\mu RW \tag{5}$$

where $P = E\ [d(t)\text{sgn}X(t)]$ and $R = E\ [X(t)\text{sgn}X(t)]$ define the matrix elements, and μ is the convergence factor. The matrix elements of the covariance matrix R become

$$E\ [X_1\ \text{sgn}\ X_1] = 2X_0/\pi + \sqrt{2/\pi}\ \sigma_n$$

$$\tag{6}$$

$$E\ [n_1^2] = E\ [n_2^2] = \sigma_n^2$$

$$E\ [n_1 n_2] = E\ [X_1 n_1] = E\ [X_2 n_1] = E\ [X_1 n_2] = E\ [X_2 n_2] = 0$$

$$E\ [X_2\ \text{sgn}\ X_2] = E\ [X_1\ \text{sgn}\ X_1]\ ;\ E\ [X_1\ \text{sgn}\ X_2]$$

$$= E\ [X_2\ \text{sgn}\ X_1] = \frac{2}{\pi}\ X_0\ \cos\ [\omega T]$$

Calculation of the remaining steering vector matrix elements yield

$$E[d\ \text{sgn}\ X_1] = \frac{2}{\pi}\ d_0\ \cos\ [\phi]\ ; E\ [d\ \text{sgn}\ X_2] = \tag{7}$$

$$\frac{2}{\pi}\ d_0\ \cos\ [\omega T + \phi]$$

Combining equations 6 and 7 results in the weight equation

$$\frac{d}{dt}\begin{pmatrix} W_1 \\ W_2 \end{pmatrix} = \frac{4\mu d_0}{\pi}\begin{pmatrix} \cos\phi \\ \cos(\omega T + \phi) \end{pmatrix}\ -2\mu$$

$$\begin{pmatrix} \frac{2X_0}{\pi} + \sqrt{\frac{2}{\pi}}\sigma_n & \frac{2X_0}{\pi}\cos\omega T \\ \frac{2X_0}{\pi}\cos\omega T & \frac{2X_0}{\pi} + \sqrt{\frac{2}{\pi}}\ \sigma_n \end{pmatrix}\begin{pmatrix} W_1 \\ W_2 \end{pmatrix} \tag{8}$$

Equation 8 illustrates the cross-coupling between the taps due to the delay T. When $\omega = (2n + 1)\pi/2$, M = 0,1,2..., the system is decoupled and in so-called normal form. The weights may be transformed into a normal coordinate system and a transient and steady-state

solution extracted. An interesting case arises when the system is coupled by a 90° phase shift between the taps to obtain a notch filter. Glover has analyzed this particular case and he showed that when a sum of sinusoids is applied to an adaptive filter, the filter converges to a dynamic solution in which the weights are time varying.[13] This time-varying solution gives rise to a tunable notch filter with a notch located at each of the reference frequencies. In this example, the desired, or primary, and reference frequencies were identical (i.e., $f_d = f_r$); however, when $f_d \neq f_r$, the weights have a dynamic steady-state response with an oscillation at the difference frequency ($f_d - f_r$) and the instantaneous response f_r. This time-varying solution should not be considered as noise in the adaptation process, since the time-varying weights modulate the reference frequency f_r and heterodyne it into the desired frequency f_d, thereby creating a notch effect.

When the system is decoupled and $f_d = f_r$, the steady-state weights approached their optical values

$$W_1\ (op) = \frac{d_0\ \cos\ [\phi]}{X_0 + \sqrt{\pi/2}\ \sigma_n} \tag{9}$$

$$W_2\ (op) = \frac{-d_0\ \sin\ [\phi]}{X_0 + \sqrt{\pi/2}\ \sigma_n}$$

with an exponential decay described by a characteristic time constant

$$\tau = \frac{1}{2\mu\ [\frac{2X_0}{\pi} + \sqrt{2/\pi}\ \sigma_n]} \tag{10}$$

Several important consequences of the "clipped" data LMS algorithm may be seen from the above analysis:

(1) the final steady-state values of the weights are determined by the amplitude of the input signals rather than the power levels as in the linear LMS case.

(2) the influence of the noise on the final values is through σ_n rather than the variance σ_n^2 as in the LMS case.

(3) the characteristic time constant is also dependent upon amplitude rather than power levels.

Thus, the clipped data LMS algorithm, besides being easier to implement in integrated circuit form, is less dependent upon the fluctuation in input power levels. This is a direct consequence of the "limiter" function introduced by the sgn function in the comparators.

The adaptive filter may be operated as a simple single-frequency noise canceller in the case of 2-tap weights. A transfer function may be obtained for this mode of operation by considering the synchronously sampled system shown in figure 3. The primary, or desired, input may be any type of signal (i.e., stochastic, deterministic, periodic, transient, or combination thereof) while the input reference signal is a pure cosine signal $X_o \cos[\omega t - \phi]$. The desired and reference signals are sampled synchronously at $f_c = 1/T$ with a 90° phase shift between taps X_1 and X_2. The algorithm for updating the weights is

$$W_1(m+1) = W_1(m) + 2\mu\epsilon(m) \, sgn[X_1(m)] \quad (11)$$

$$W_2(m+1) = W_2(m) + 2\mu\epsilon(m) \, sgn[X_2(m)]$$

The first step in the analysis is to consider the adaptive noise canceller as a feedback network with the filter output $Y(m)$ disconnected, in the manner of Widrow, et. al.[16] Under these conditions, a unit impulse is applied at the desired input to create an error

$$\epsilon(m) = \delta(m-k) \quad \begin{cases} 1 \; m = k \\ 0 \; m \neq k \end{cases} \quad (12)$$

The resulting pulse transfer function G(Z) is averaged over T/4 to obtain

$$G(Z) = \frac{8\mu X_o}{\pi} \frac{(Z \cos[\omega_o T] - 1)}{Z^2 - 2Z \cos[\omega_o T] + 1} \quad (13)$$

and since the closed-loop transfer function is $H(Z) = [1 + G(Z)]^{-1}$, the closed-loop zeroes are given as

$$Z = e^{\pm j\omega_o T} \quad (14)$$

and poles from the solution of $1 + G(Z) = 0$. If the narrow-band approximation is used with $\mu X_o < 1$, then the poles are inside the unit circle with a radial distance
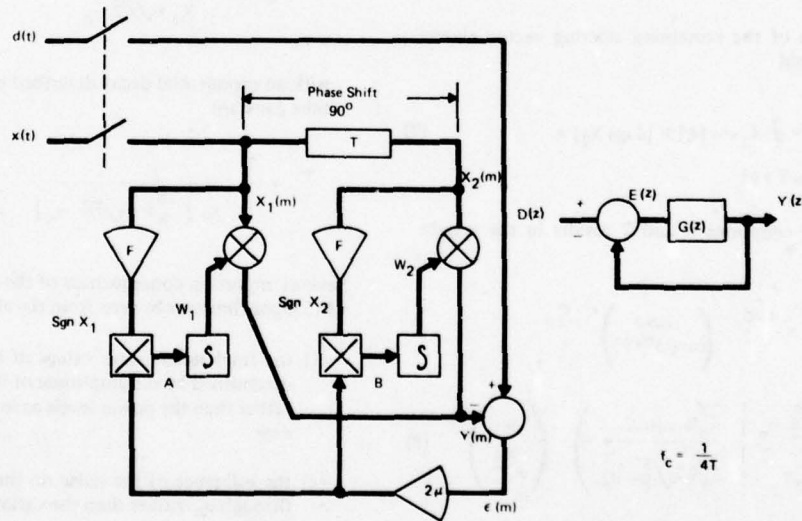
$$\left(1 - 8\mu\frac{X_o}{\pi}\right)^{1/2} \cong 1 - 4\mu\frac{X_o}{\pi} \quad (15)$$

Figure 3. Single Frequency Adaptive Noise Canceller with Clipped Data LMS Algorithm

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from the origin as indicated in figure 4. The angles of

source current is given by

$$i_{ds} = K (V_{GS} - V_T) V_{ds} (V_{ds} \cong 0) \qquad (17)$$

$$= g_{ds} V_{ds}$$
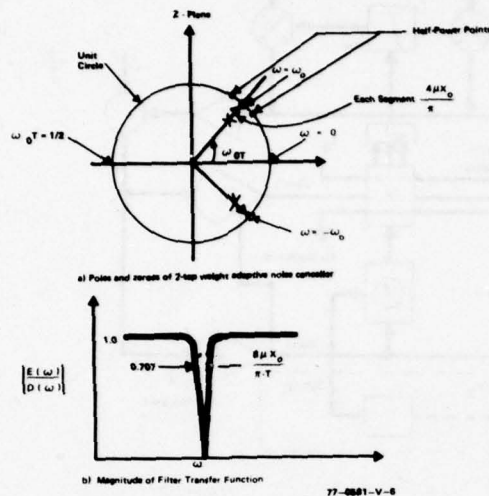
Figure 4. Characteristics of a 2-Tap Weight Adaptive
Noise Canceller with Clipped Data LMS Algorithm

the poles are almost identical to those of the zeroes
with a notch filter bandwidth of

$$\Delta \omega = \frac{8\mu X_o}{\pi T} \qquad (16)$$

and $Q = \omega_o / \Delta\omega$.

2.2 Monolithic CCD Adaptive Filter Design Considerations

A block diagram of the monolithic 16-tap analog
adaptive filter is shown in figure 5. The analog delay
line is a 2-1/2-phase CCD tapped delay line with a
floating clock electrode sensor circuit[15] at each tap
location to nondestructively sense the CCD signal
charge and provide charge-to-voltage conversion. The
CCD structure and timing is designed to maximize
isolation between the clock signals and the signal sens-
ing mode of the CCD.

The output of each tap location is a voltage which is
converted to a weighted current, representing the re-
quired multiplication, via the drain-source con-
ductance of a NMOS transistor biased in the triode
region. In the triode region, the incremental drain-

where K is a constant dependent on device geometry
and processing parameters, V_{GS} is the gate-source
voltage (integrated value of $2\mu|\epsilon|$), V_T is the
threshold voltage, v_{ds} is the drain-source voltage
(delay line output), and g_{ds} is the drain-source con-
ductance. Positive and negative weight values are
achieved by using two transistors at each tap location,
setting the conductance of one transistor to a fixed
value, and allowing the conductance of the second
device to vary via the adaptive algorithm. The required
integrator is realized via the gate capacitance of the
NMOS transistor weight. The incremental change in
tap weights is achieved using the bidirectional charge
controlled circuit described below.

The two currents from each tap are summed
simultaneously with the weighted currents from the
respective transistors at the other tap locations. The
input nodes of two CMOS operational amplifiers serve
as the two summing nodes. The two currents are con-
verted to a voltage and further processed by a subtrac-
tor, comparator, absolute value circuit, and gain
amplifier, as required by the "clipped data" LMS
algorithm.

Referring to equation 2, the weight update algorithm
requires a comparator at each tap location to form sgn
X(m). The circuit complexity is reduced considerably
by using a single comparator at the delay-line input
and applying the comparator output (sgn X) to a
digital shift register which is clocked in synchronism
with the analog sample in the CCD. An Exclusive OR
circuit provides the digital multiplication which pro-
vides the branch operation to increment or decrement
the voltage of the NMOS weight.

On-chip timing is generated using three D-type flip-
flops configured as a ripple counter to provide
decoding waveforms for the NAND/NOR gates used
in the combinatorial logic. The ability to update all the
weights simultaneously relaxes the requirements of the
clock drivers.

2.2.1 Methods for Achieving Programmable Weights

In order to achieve a variable V_{GS}, the error $\epsilon(mT)$
can be converted to digital form with an A/D con-
verter, storage and accuracy can be achieved with ac-
cumulators, and finally, the multiplication can be ac-
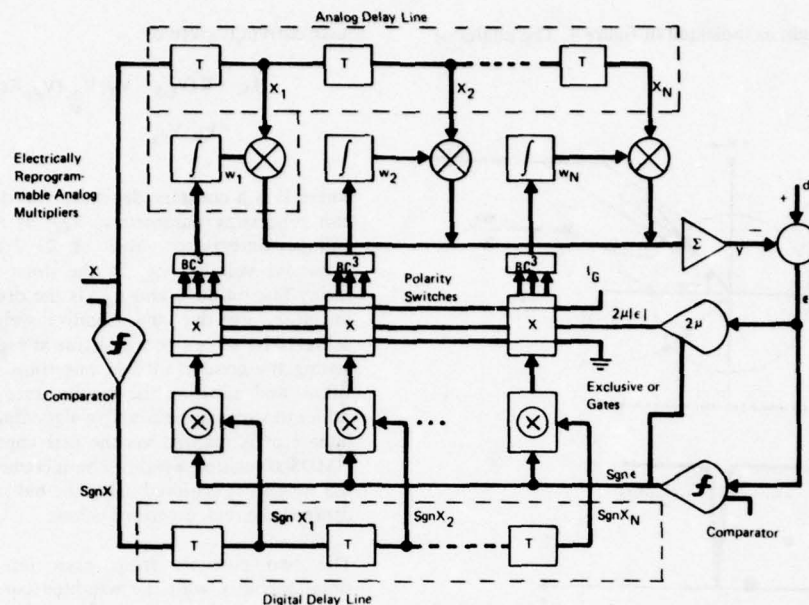
Figure 5. Monolithic CCD Analog Adaptive Filter

complished with multiplying digital-to-analog converters (MDAC's). This is an attractive approach because of the recent advancements in capacitor-weighted MDAC's.[16] However, unless the MDAC is shared over many taps, the complexity of the adaptive signal processor is increased.[17] In general, an MDAC for each tap weight is not too appealing an approach because of the chip area involved in the layout. In addition, the off-chip peripheral hardware is quite involved because of storage and accuracy requirements in the A/D conversion process. An 8-tap weight system has been built with this approach and it performed adaptive linear prediction with the clipped LMS algorithm.[17] However, the approach used lumped L-C delay lines with different dispersive characteristics, and a large amount of peripheral hardware was required for implementation.

Another method for achieving programmable weights is to replace the NMOS transistors described above with metal-nitride-oxide-silicon (MNOS) nonvolatile memory transistors. Memory is achieved in the MNOS transistor by electrically reversible tunneling of charge from the silicon semiconductor to deep traps near the SiO_2/Si_3N_4 interface. By the application of suitable voltages to the gate of the transistor, the threshold voltage can be changed in discrete increments. These

changes can then be sensed as a change in the conductance of the transistor. This type of device has been used as the programmable tap weight and integrator, with a tapped CCD, to demonstrate in a hybrid form a 2-tap integrated circuit LMS adaptive filter.

A final approach to achieving programmable tap weights is the bidirectional charge-controlled circuit (BC³). The technique uses stabilized charge injection to increment or decrement analog signal charge onto the node of a MOS-FET analog conductance. The concept is illustrated in figure 6. The analog, scaled error signal, $2\mu\epsilon$, is applied to a CCD storage or holding well and the control of the signal is accomplished by selecting the proper function of the G_1 and G_2 electrodes. The selection process involves the binary multiplication of

$$\text{sgn} [\epsilon(mT)] \otimes \text{sgn} [x(m-k)] \qquad (18)$$

with an Exclusive OR gate as indicated in figure 5. The incremental voltage applied to the gate of the MOS-FET voltage-controlled analog conductance weight is

$$\Delta V = 2\mu |\epsilon| \frac{C_H}{C} \qquad (19)$$
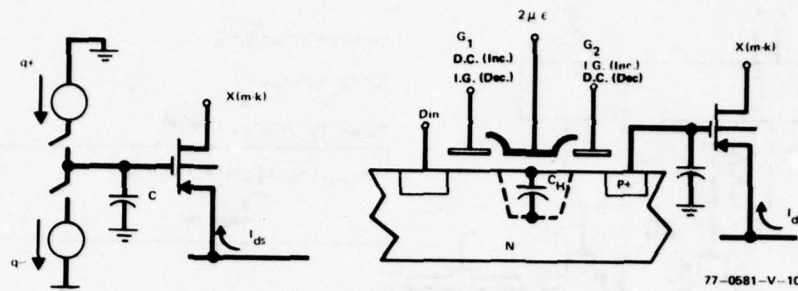
Figure 6. Bidirectional Charge Control for Incremental Adjustment of MOS-FET Analog Conductance Weight

where $|\epsilon|$ is formed with an absolute-value amplifier, and C_H is the holding well capacitance. The storage or integration of the weight values is performed with the on-chip capacitance C associated with the gate node of the MOS-FET weight. In order to achieve long-term weight retention, as might be necessary for some voice processing applications, either the C must be increased, which decreases the sensitivity of the weight to adjustment and increases the chip area for on-chip weighting, or some method of weight updating must be employed. One such method is to use an off-chip weight capacitance. Another method is to employ an A/D converter, memory, and a MDAC to sequentially update the weights in synchronization with the CCD clock.

3.0 Experimental Results

The feasibility of implementing the "clipped" LMS algorithm has been confirmed by fabricating and testing a 2-tap weight hybrid processor. The processor has been constructed using a basic linear combiner composed of a CCD serial in/serial out structure (see ref. 15), MNOS analog conductances, operational amplifiers, comparators, CMOS switches, and CMOS logic. A block diagram of the hybrid processor is shown in figure 7. The processor was configured, as shown in figure 8, to allow characteristic measurements to be made. Measurements were performed to determine the convergence factor, μ, as a function of processor transient response. The ability of the processor to track as a function of phase and amplitude variation in the desired channel (d of figure 8) was also confirmed.

The processor was then configured as a noise canceller. The block diagram of the arrangement and experimental results are presented in figure 9. The desired signal was corrupted by a narrow band tone 16

dB greater. After processing by the adaptive filter, the output interfering tone was 18 dB below the desired tone, representing a rejection of 34 dB.

4.0 Applications

There are a number of applications for adaptive filters with special need for real-time signal processing. Several applications are:
- Estimation/Prediction
- Filtering
- Spectral Analysis
- Data Compression
- Interpolation
- Multiple Linear Regression
- Echo Cancellation
- Speech Analysis
- Noise Cancellation
- Coherent Signal Processing
- Frequency Measurement
- System Modeling.

4.1 Adaptive Noise Cancellation

A very important application area is adaptive noise cancelling, such as the removal of interference in electrocardiographs, noise in speech signals, clutter cancellation in antenna sidelobe interference (or similar type systems with hydrophones, seismic/acoustic tranducers, electro-optical sensors, etc) and coherent signal processing when periodic signals must be separated from broadband interference, such as in spread spectrum systems. Cancellation of 60-Hz interference in conventional ECG, the donor ECG in heart transplants, and the maternal ECG in fetal electrocardiography is a straightforward use of the 2-tap adaptive noise canceller to reject the interference of a single frequency. The advantage of this technique is
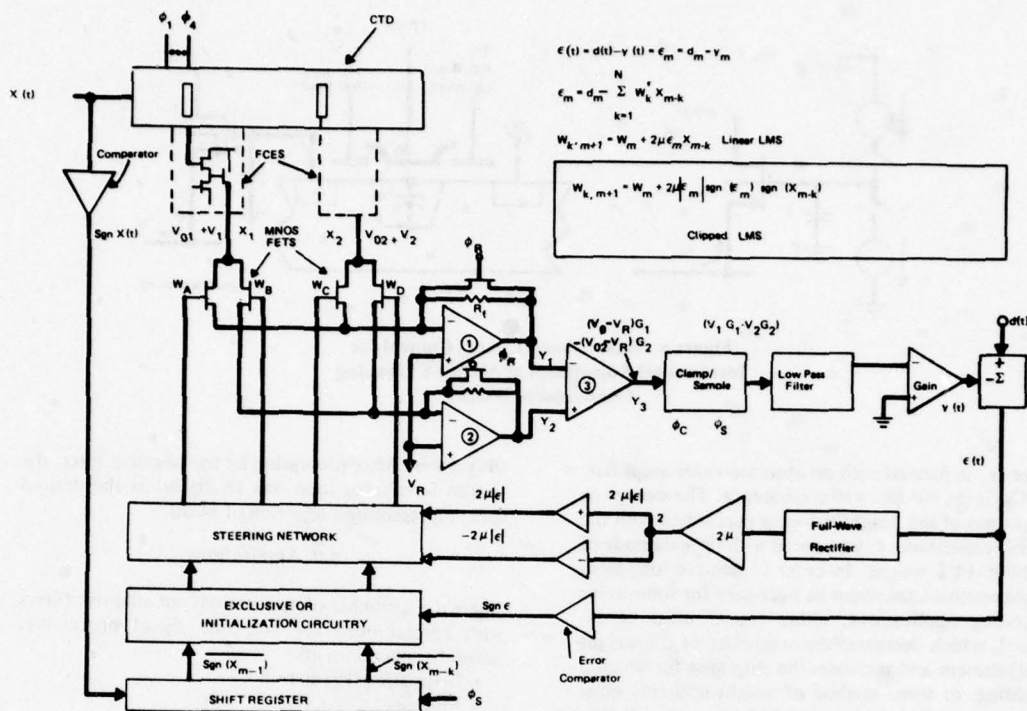
Figure 7. Adaptive Signal Processor Block Diagram (Clipped Data LMS Algorithm)
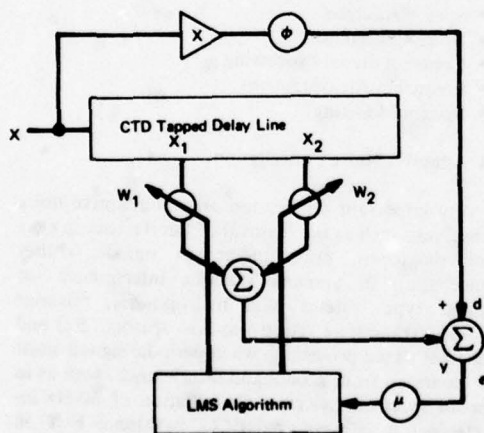
Figure 8. Configuration of Hybrid Adaptive Processor for Making Fundamental Performance Measurements

the cancellation of the interference even when the latter interfering signal frequency changes with time, since the reference input to the filter also changes.

A second area is the cancellation of noise in speech applications, such as the situation which arises in pilot communications with a high level of background engine noise. This interference contains strong periodic components in the speech frequency band and the intelligibility of the radio transmission is affected. A conventional filter would not suffice since the frequency and intensity of these interference signals vary with engine speed and load, in addition to the location of the pilots head.

A third area of noise cancelling is in adaptive cancellation of sidelobe interference in receiving arrays. For example, a sensor beamformer may be constructed with the adaptive noise canceller as shown in figure 10. The multiple reference inputs to the noise canceller are obtained from the beamformer element outputs prior to summation. The operation of the beamformer is

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Figure 9. CCD Adaptive Noise Canceller with 2-Tap Adaptive Element

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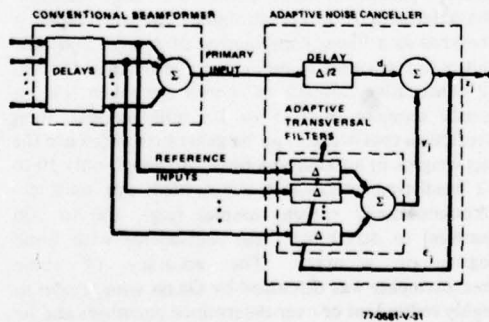
Figure 10. A Null-Constrained Adaptive Beamformer Array

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constrained by the selection of the weighting coefficients of the adaptive filter taps. The gains of the control taps in the adaptive filter are constrained to zero in some manner so as to provide compensation for variations in element gain and phase, and to permit the reception of broadband signals over a desired angular sector.

A fourth area of interest is the separation of broadband and periodic signals as illustrated in figure 11. The insertion of a fixed delay in the reference path, as shown in figure 11a, decorrelates the broadband components while the narrow-band components remain correlated. This is an excellent method in the case when no external reference input is available, such as speech or music playback in the presence of tape hum

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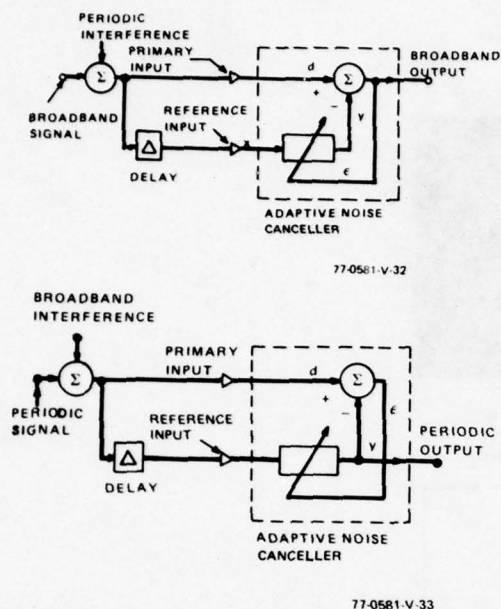
Figure 11. Separation of Broadband and Periodic Signals

or turntable rumble. Another area of application is in spread-spectrum communication. In this application, the narrow-band jamming signals can be separated from the broadband spread spectrum signal, and thus avoid compression of system dynamic range. Figure 11b illustrates the recovery of the periodic components and application, such as automatic signal seeking and the enhancement of low level sinusoidal signals buried in broadband noise. Thus, the adaptive filter can function as a coherent signal processor.

4.2 Adaptive Linear Prediction and Noise Cancellation for Narrow-Band Robust Voice Processing

A promising area for CCD adaptive filtering is in speech processing where redundancy in the spoken word has long been recognized by researchers. Electrical processing of speech which takes this redundancy into account can be used to substantially reduce the bandwidth required for speech transmission. For example, if speech is sampled and quantized at 56 k bits/sec (7 bits or 128 possible amplitude levels per sample at 8 kHz) for acceptable fidelity but the channel bandwidth restricts transmission to below 4 k bits/sec, then a speech compression ratio of approx-

imately 15:1 is required. This low data rate would permit speech to be transmitted over high frequency radio or telephone links which have bandwidths barely wide enough for the original analog speech sounds. Such a narrow-band voice digitizer may be used in frequency division multiplexing for simultaneous transmission over wide-band channels. Narrow-band digitized speech lends itself to encryption for secure communication and provides a better S/N than a wide-band digitizer, particularly in RF transmission communication satellite links with limited or fixed available power.

"Speech compression, which maintains intelligibility, has always been difficult because speech consists of more than words and messages. Speech has the vocal timbre and conversational idiosyncrosies of the speaker and the emotion behind his words. It is normally constructed in an impromptu manner and delivered in a free and informal fashion. Speech flows in time as a continuation that a voice digitizer must process in real time, leaving no chance for later evaluation or correction. Although the information content of the message itself may be low (possibly below 100 bits/sec), transmission of the subtle vocal inflections requires a data rate of several thousand bits/sec."[18] Historically, speech compression and reconstruction began with the Dudley channel vocoder in 1936 in which the Fourier spectrum characteristics of speech determined the parameters of a filter bank. This filter bank approximated the vocal tract resonance characteristics of speech. It was excited by a pulse generator (variable period) to approximate the vowels or larynx vibration and a random noise generator to represent the consonants or fricative nasal sounds.

Another technique has proven quite successful in speech compression: linear prediction coding (LPC).[19] Linear prediction algorithms use time domain characteristics of the speech signal. The voice signal is analyzed as a linear combination of present and past values to form a set of prediction coefficients. If 10 to 12 consecutive samples of speech are taken (i.e., a speech segment of 1.25 to 1.5 milliseconds), then prediction coefficients can be generated which are the tap weights in an adaptive filter. Although only 10 to 12 prediction coefficients are needed, one must accumulate many speech samples (e.g., 100 to 200 samples) to determine these coefficients with some degree of accuracy. The accuracy of these measurements was discussed by Gauss with regard to highly redundant or over-determined equations and he formulated the method of least-squares. This method is used in the CCD adaptive filter.

Figure 12 illustrates a functional diagram of a conventional digital linear productive narrow-band voice processor. The major functional elements of this system are:

- Vocal tract analyzer
- Pitch extractor
- Voice/unvoice analyzer
- Synthesizer
- Encoder/decoder.

Many digital narrow-band voice systems using linear prediction algorithms have been analyzed and built over the last 5 years. The present major limitations to an all-digital approach are size, power dissipation, and cost. It is possible, however, that VLSI technology may impact some of these limitations in the future.

Figures 13 and 14 illustrate the use of the CCD adaptive filter as an analysis filter to generate the prediction coefficients $W_1 \ldots W_N$. The voice input is band-pass filtered and applied to the adaptive filter. The filter input is also used as the primary or desired signal to generate an error called the prediction residual. This error signal may then be used to extract the pitch period, amplitude, and voice/unvoice decision. The speech sample frame may be nominally 20 milliseconds in length and the error must converge to its minimum value within this time. Near the end of the time period, a unit pulse is inserted into the filter. The filter output is the impulse response of the filter. The converged weights are the predictive coefficients representing the state of the vocal tract. These coefficients can then be transformed to partial correlation

coefficients for later transmission. The clipped data LMS algorithm has been computer simulated with the following constraints:[20]

- $W_k \leq 0.98$
- An increase of the unit circle (Z-domain) by 10 percent with scaling of the prediction coefficients
- 10 prediction coefficients of bit levels: 8,8,8,8,7,7,7,6,5,5
- Data rate of 3,600 bits/sec.

The prediction coefficients generated with the clipped data LMS algorithm and the above constraints were used to synthesize speech. Test sentences were employed and the playback of the reconstructed speech indicated good speech reproduction and quality, although the latter is a subjective parameter. Thus, a CCD adaptive filter with 10 weights operating at an 8-kHz sample rate is an excellent candidate for this particular application.

The use of the prediction residual of the analysis CCD adaptive filter as the pre-whitened input to a pitch extractor is an important application. The prediction residual signal is the voiced signal with the vocal tract contributions removed. Ideally, this signal corresponds to the source of voiced sounds caused by the vibrating vocal chords at the glottis. Linear prediction implementations usually have access to the prediction residual. However, those speech processing techniques which are based upon the short-time spectrum analysis (e.g., the channel vocoder) do not yield a whitened version of the voiced signal as a by-product of their pro-
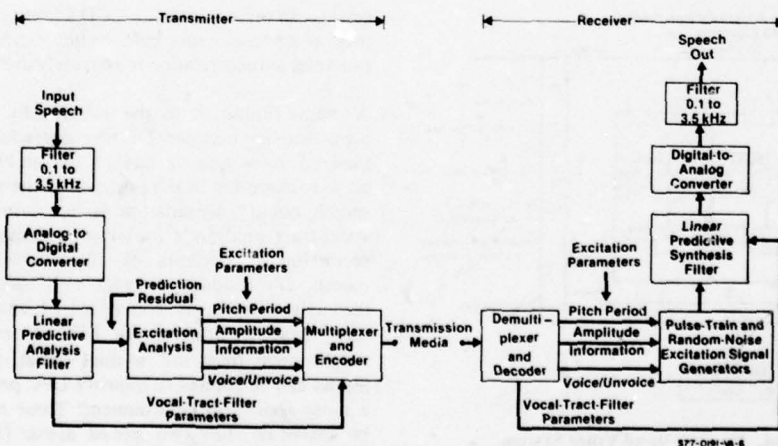
Figure 12. Narrow-Band Voice System

Analysis Filter - Digital Implementation

Analysis Filter - Sampled Data Implementation

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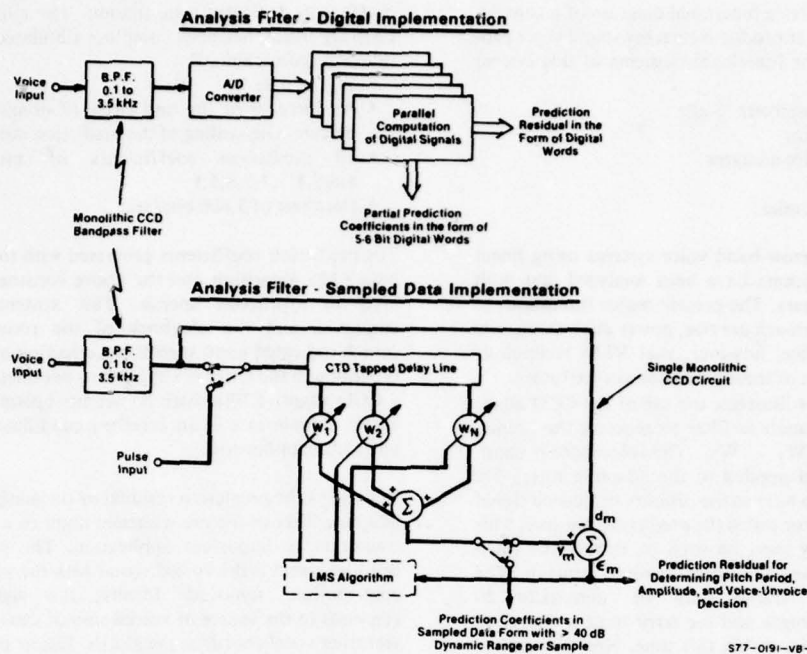
Figure 13. CCD Adaptive Filter for Linear Prediction Analysis of Speech

Figure 14. Narrow-Band Voice System
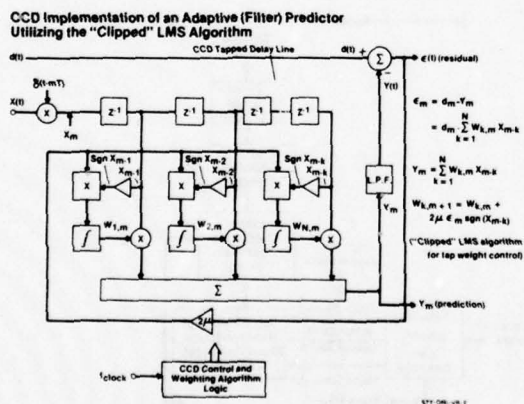
cessing. In these systems, a CCD adaptive filter simply used as a pre-whitener before pitch extraction by, for example, autocorrelation is extremely useful.

A major limitation to the use of LPC in practical acoustical environments is the degradation of synthesized voice quality due to the ambient acoustic noise background in the presence of the speaker. This speech quality degradation is due primarily to the vocal-tract analyzer's inability to compute accurate prediction coefficients of the "uncontaminated" speech. The residual or "whitened" speech signal of the analyzer is likewise contaminated, which causes errors in pitch extraction for LPC systems that synthesize pitch from the residual signal. Several techniques can be applied to improve LPC performance in a noisy acoustical environment. These methods may be classified into two broad areas: (1) acoustical and/or electrical interference mitigation prior to computation of the vocal-tract parameters, and (2)

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algorithms, such as SABER,[21] which attempt to separate the interference in the process of vocal tract computation. Electrical techniques, which mitigate interference prior to analysis, generally require two microphones. One microphone receives speech contaminated with ambient noise while the second microphone "receives" only the ambient noise. These signals are subsequently processed with an adaptive filter of the type described here for noise cancellation. In most practical environments it is difficult to arrange two strategically located microphones. A single microphone scheme can be implemented which will provide interference cancellation. This method assumes a "push-to-talk" microphone (i.e., similar to popular CB sets) is used and a time lapse of 200 to 300 milliseconds exists from activation of the microphone to the commencement of speech. A CCD adaptive filter, constructed of 6 to 20 taps, converges to a least-square estimate of the ambient noise within this 200- to 300-millisecond time lapse. Subsequently, the weights of the filter are fixed during the speech transmission and the filter serves to remove the background interference. One method for holding the weight values might be through the use of a digital memory coupled to MDAC's at the taps of the CCD. This technique assumes the noise environment is stationary in the period of speech transmission. In tests performed with the SABER algorithm, this requirement of noise stationarity did not limit the performance achieved in noise reduction. Figure 15 illustrates a robust LPC system block diagram which includes a noise canceller prior to the analyzer.

5.0 Conclusions

The description of the clipped LMS algorithm for adaptive signal processing has been presented along with a detailed analysis of a 2-tap weight adaptive filter. The 2-tap weight clipped, sampled data algorithm has been reduced to practice using a tapped CCD delay line, MNOS transistors for multiplication and integration, hybrid operational amplifiers, and CMOS logic elements. Experimental results show the algorithm is acceptable for analog LSI implementation. The basic components are amenable to monolithic fabrication. Numerous applications are presented for the CCD-LSI adaptive filter chip with special attention given to voice processing.
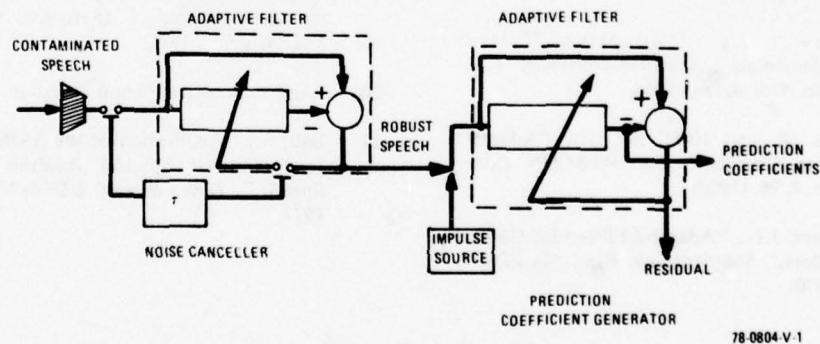
Figure 15. Robust LPC System Front-End

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FULLY INTEGRATED VOICEBAND FILTERS

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Research Ltd.   Research Ltd.

This paper will describe design techniques to achieve a high performance CCD voiceband filter which meets all specifications required for telecommunications applications. The design techniques include the following:

- double-split electrode technique
- balanced charge sensing technique
- compatible input/output scheme
- minimum phase filter design.

The paper will describe the role of each of the above techniques in meeting the required performance specifications of telecommunications systems.

The double-split electrode technique (1,2) will be described in detail and shown to be essential in the design of high performance CCD transversal filters. The key features are reductions of clock sense line capacitance and consequent reduction in common mode signal, and noise pickup, and noise gain. Ohter features of the approach include reduced sensitivity to gain error and reduced tap quantization error.

Closely tied in to the performance of double-split electrode structure is the sensing technique. Since the middle segments of the double-split electrodes are clocked separately from the sensing segments, the sensing circuit must clamp the outer segments to the same level as the clocked segments. Total symmetry is essential in order to maintain clock noise rejection and minimize offsets at the filter output. Methods of achieving this will be discussed.

A compatible input/output scheme is required to ensure that high linearity can be maintained as well as accurate control on device gain. The filter components must be arranged so that all parameters are functions of ratios of device structures which track during fabrication. This is an important requirement especially where absolute gain variations are limited to $\pm .1dB$. The components pertaining to obtaining maximum performance will be discussed.

Finally, the advantages of minimum phase design (3) will be related to telecommunication requirements and CCD transversal filter design criteria. It is shown that minimum phase requires less tolerance and less transfer efficiency to realize the same magnitude response as linear phase filters.

The performance measurements on a fully integrated double-split electrode, minimum phase, low pass filter will be discussed. The filter was fabricated using double-poly silicon gate n-channel MOST process. Some of the measured parameters on this filter were:

Dynamic range	>80dB
Linearity	>50dB
Gain tracking	<.1dB
Filter response passband	$\pm .1dB$
stopband	<-40dB

The CCD transversal approach is shown to be an attractive approach for making high performance integrated filters for voiceband filters. The filters have been successfully integrated with a PCM voice codec (4).

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A CCD/NMOS CHANNEL VOCODER*

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ABSTRACT

The need for security in voice communication is met by converting voice to digital form so that sophisticated digital encryption is possible. Of course, it is very desirable that the digital voice signal be compatible with conventional 3 kHz analog voice transmission bands, hence the vocoder which converts analog voice signals to digital form must employ some form of bandwidth compression to yield data rates down to 2.4 kbits/sec. Linear prediction techniques are commonly used to implement vocoders in essentially all-digital systems, but with current technology such systems are expensive, fairly large, and consume large amounts of power. This paper concerns the application of CCD technology to the vocoder problem using a second much older approach, the channel vocoder. The objective is to demonstrate the potential of analog CCD technology to achieve a low cost, low power vocoder system. Two custom design CCD/NMOS integrated circuits are the key to this approach and the design of these circuits will be reviewed in this paper.

I. INTRODUCTION

Speech signals are well matched to the capabilities of both CCDs and switched capacitor filters. The applications of speech processing systems are presently expanding very rapidly and include such areas as vocoders, speaker verification systems, word recognition, computer generated speech, and many others. The compatibility of CCD and switched capacitor filters with large scale integration promises to have significant impact in lowering the cost and in accelerating the uses of complex speech processing systems.

This paper concerns the development of two speech processing ICs utilizing analog CCDs and switched capacitor filters. These ICs are intended for use in a 2.4 kBPS channel vocoder although the devices are compatible with other uses as well.

The function of this vocoder system is to reduce the data rate of speech transmission to 2.4 kBPS while maintaining high quality and intelligibility in the reconstructed speech signal at the receiver. The block diagram of the system is depicted in Figure 1. This integrated system is a channel vocoder based on a system and algorithm developed in the UK. [1] The two portions of the system which are enclosed in the dashed lines in the figure are being implemented with two custom designed CCD/
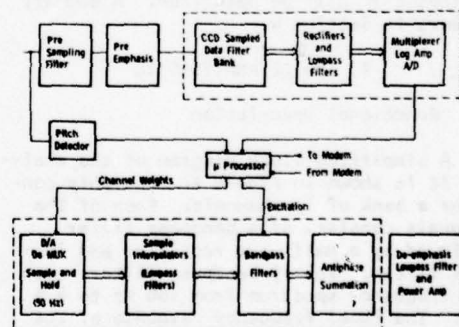
Figure 1. Block diagram of a channel vocoder based on two custom IC functions enclosed in dashed lines.

NMOS integrated circuits, while the remaining functions are implemented with a few simple analog components and five TMS 9940 microcomputer circuits. One of these two special circuits is used for speech analysis and the other for synthesis. Three of the TMS 9940 microcomputers are used to implement a modified Gold-Rabiner pitch tracker.[2] The other two TMS 9940s control the analyzer and synthesizer and interface the modem.

The basic operation of the channel vocoder is to determine periodically (every 20 msec) the spectral envelope of the speech using a filter bank. The nature of the excitation of the speaker's voice (either a periodic pulse train for voiced sounds or a random noise source for unvoiced sounds) is determined by a pitch tracker. These parameters are encoded into a compact digital code and transmitted to the receiver which then synthesizes a signal having approximately the same spectral envelope. The synthesizer uses a filter bank excited by either a periodic pulse train or random noise where the gain parameters of the filter bank, the selection of the excitation, and the pulse period are controlled by the information from the transmitted signal. The vocoder takes advantage of the fact that phase information is relatively unimportant in man's perception of speech sounds.

In the next section of this paper the voice analysis IC will be described. Several of the key circuit techniques used will also be discussed. In Section 3, the voice synthesis IC will be described. A summary appears in Section 4.

2. VOICE ANALYSIS IC

2.1 Functional Description

A simplified block diagram of the analyzer IC is shown in Figure 2. The chip contains a bank of 19 channels. Each of the channels consists of a bandpass filter followed by a half wave rectifier and low-pass filter. The 19 bandpass filters span the frequency spectrum from 180 Hz to 4.1 kHz. The ideal frequency response of the analyzer filter bank is plotted in Figure 3. Each channel output is thus a measure of the energy in the corresponding spectral range. The 19 channels are sampled once every 20 msec and then sequentially multiplexed into

an A/D converter having a logarithmic response. A 5-bit digital code with 1.5 dB steps is thus generated for each of the 19 segments of the spectrum. The chip also contains the necessary clocks and timing circuitry to interface the microprocessor system.
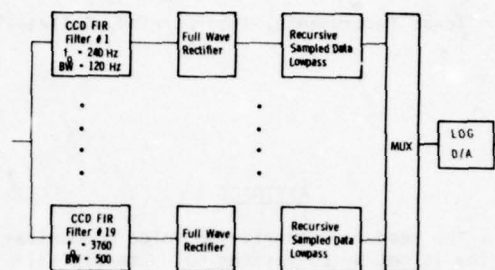
Figure 2. Block diagram of the channel vocoder speech analysis IC

The bandpass filters of the analyzer chip are implemented with 100 stage CCD transversal filters employing the split electrode charge sensing scheme.[3,4] The transfer function of the CCD was designed to approximate that of a second order Butterworth bandpass filter shown in Figure 3.
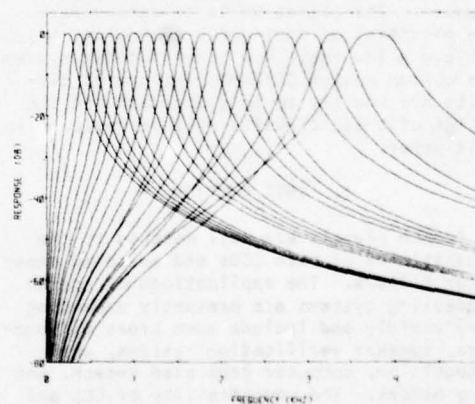
Figure 3. Frequency response of the 19 channels of the speech analyzer filter bank.

The Butterworth characteristic and the expected CCD response are plotted in Figure 4 for one of the channels. A slightly modified version of the Parks, McClellan, Rabiner design program [5] was used to compute the CCD coefficients. It is interesting to note that while the desired transfer function in this case can be implemented with only two complex pole pairs, it takes 100 zeros in the transversal filter to achieve a good approximation. Yet the 100 stage CCD filters and their associated output amplifiers require only one op amp each while second order switched capacitor bandpass filters require two to four amplifiers and thus more power.
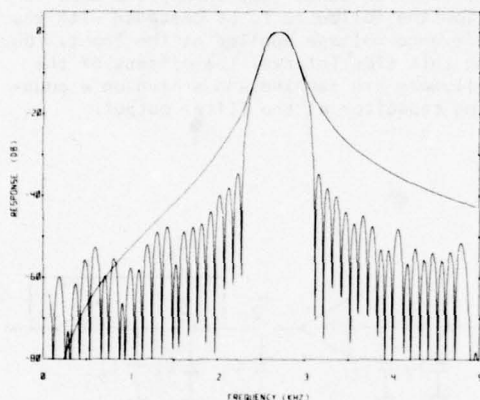
Figure 4. CCD filter response for a typical channel in the vocoder analyzer with a second order Butterworth characteristic superimposed. The band center is 2700 Hz and the 3 dB bandwidth is 330 Hz.

2.2 Circuit Implementation

2.2.1 Analyzer CCD Filters

The CCD filters are fabricated using a four phase, double poly, co-planar electrode structure. The clocking scheme [6] is illustrated in Figure 5. Two of the electrodes ϕ_1 and ϕ_2 are clocked with overlapping 15V clock wave forms at a 10 kHz rate while ϕ_3 is used as a barrier biased at 2V DC and the split electrode sense lines are biased at 8V by the output circuit. The output sensing circuit is shown in Figure 6. An operational amplifier having differential outputs is used

along with two feedback capacitors C_f to perform the differential current integration function required for split electrode CCD filters. The gain of the CCD filter is controlled by the size of the poly-poly feedback capacitors along with the weighting coefficients of the filter. The capacitor size in each of the 19 filters was adjusted for the same in-band gain.
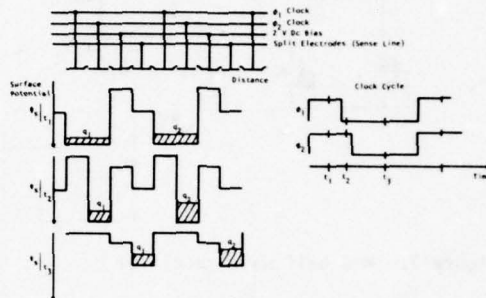
Figure 5. Schematic diagram of the CCD charge transfer process & clock timing.

CCD OUTPUT CIRCUIT
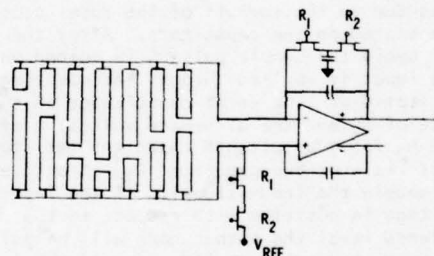
Figure 6. CCD filter output circuit

2.2.2. Analyzer Rectifiers

The bandpass filtered signals are rectified by the half wave rectifier circuit shown in Figure 7. This circuit takes advantage of the sampled data nature of the CCD output signal in order to establish a reference level with low offset. The rectifying action is obtained by using the MOS transistor M_8 to charge capacitor C_2 to the cutoff point of the transistor. The differential amplifier formed by $M_3 - M_7$ and the associated depletion load current sources $M_{11} - M_{13}$ is used as a comparator to achieve sharper

cutoff characteristics. Once each cycle the reset clocks R_1, R_2 and R_3 are turned on.
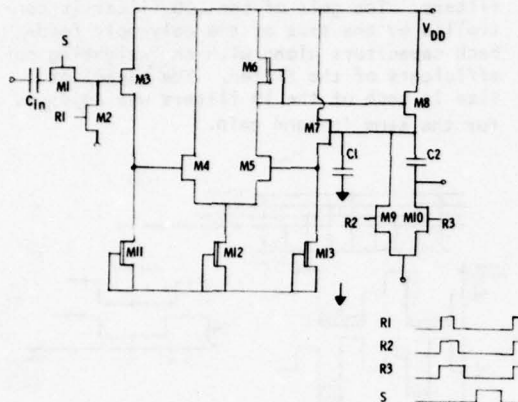
Figure 7. MOS half wave rectifier

This connects the input to a fixed reference and also discharges the output capacitors C_1 and C_2. The turnoff edges of the clocks are staggered in time with the result that offsets due to the turnoff of the reset clocks are stored on the capacitors. After the reset cycle the sample pulse S is turned on and the input is applied through the coupling capacitor C_{IN}. The stray capacitance on the gate of M_3 and the alternate switching of M_1 and M_2 forms a switched capacitor resistor.[7,8] This resistor and capacitor C_{IN} effectively AC couple the input signal. If the input voltage is positive with respect to the reference level the output node will be pulled up by M_8 through capacitor C_2. If the input sample is negative with respect to V_{ref} M_8 remains cutoff and the output remains unchanged. Experimentally we find that the circuit has approximately 10 mV offset which is adequate for this application.

2.2.3 Analyzer Lowpass Filters

After the signal for each channel is rectified, it is lowpass filtered with three pole Butterworth filters having a 35 Hz bandwidth. In this case the area advantage was clearly in favor of the switched capacitor filter approach rather than CCD filters, so these filters are implemented with switches, capacitors, and simple source follower circuits. The filter is shown in Figure 8, where the

source followers are indicated by gain blocks with gain of 0.9 and the MOS transistors used in the switched resistors are indicated as switches. The real axis pole is implemented with the capacitor C_1 and C_2 and buffered by the first gain stage. This part of the filter is operated at the same 10 kHz clock rate as the CCD bandpass filters. In order to save area the second stage of the lowpass filter which provides a complex pole pair is clocked at 1 kHz and uses the first stage as an antialiasing filter. In order to eliminate dc offsets in the lowpass filter, the energy storage elements of the filter are periodically disconnected from the source followers and other switches (not shown) are used to allow the followers to be cascaded with the reference voltage applied at the input. During this time interval the offsets of the followers are sampled and stored on a coupling capacitor at the filter output.
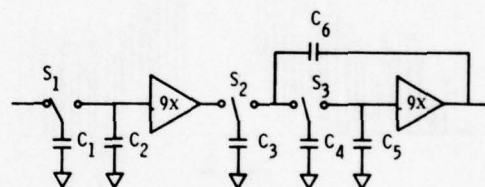
Figure 8. Schematic diagram of a 3 pole lowpass filter implemented with switched capacitors. The capacitor values are: C_1 = 0.50 pF, C_2 = 22.4 pF, C_3 = 1.53 pF, C_4 = 1.00 pF, and C_6 = 15.0 pF.

2.2.4 Logarithmic A/D Converter

The signals from the 19 channels are sequentially multiplexed into the logarithmic A/D converter which provides a 5 bit code at a 1 msec rate. The step size in the converter is 1.5 dB. A simplified schematic of the converter is shown in Figure 9. The operating principle of the device is similar to the charge redistributor A/D converter.[9] A binary weighted capacitor array made of poly-poly capacitors is used to obtain 6dB increments while a polysilicon resistive

divider is used for the 1.5 dB steps. The cycle of the converter is initiated with all switches at the reference position. During this interval the switched resistor is clocked with two nonoverlapping clocks R and S which provide DC feedback around the comparator and stores the comparator offset on the capacitor array. Subsequently the input capacitor $C_{IN} = 2C_O$ is switched from the signal reference to the input signal which causes a negative going charge in the common node of the capacitor array. Then using a successive approximation algorithm the other capacitor switches are selectively switched to the reference voltage line (node A in the figure) causing positive going steps on the common node. After the nearest 6 dB increment is found using the capacitor switches node A is switched to the nearest 1.5 dB increment on the resistive reference divider. Where a conversion cycle is completed the 5-bit code is latched into TTL output buffers and held until the output for the next channel is ready. A data ready pulse is also provided to synchronize the microprocessor.

Figure 9. Simplified schematic of the logarithmic A/D converter

3. Voice Synthesis IC

3.1 Functional Description

A block diagram of the speech synthesizer IC is shown in Figure 10. The input to this chip is a sequence of 20 8-bit digital words at a rate of one per msec. One of these words controls the selection of voiced or unvoiced V/U excitation on the chip which is either a pseudorandom sequence or a pulse

generator whose period is controlled by the data in the excitation word. This excitation word is recognized by nonzero bits in the three MSB positions and it also serves the function of speech frame synchronization. The remaining 19 words of input data all have zeros in the three MSB positions and the five LSB lines are directed to an anti-logarithmic D/A converter. The output of the D/A is de-multiplexed to 19 sample and hold circuits, one for each of the synthesis channels. Each of the synthesis channels consists of a three pole lowpass filter, a modulator, and a band-pass filter. The lowpass filter provides interpolation between the speech frames, and its output is used to modulate the amplitude of the excitation pulses which are applied to the bandpass filter of the corresponding channel. The outputs of the 19 channels are then summed together with every other channel having the opposite polarity in the sum. The reason for the anti-phase summation is to avoid large output pulses which could result from coherent responses of all of the channels and would require a larger dynamic range in the output amplifier. As we noted earlier, the relative phase of the different parts of the speech spectrum is not important in speech perception.

Figure 10. Block diagram of a channel vocoder speech synthesis IC.

3.2 Synthesizer Circuit Implementation

3.2.1 Logic Circuits

All of the logic functions shown in the block diagram of the synthesizer in Figure 10 are implemented with standard NMOS 5V de-

pletion load circuits. For the excitation, either a pitch word is loaded into an eight stage counter which provides periodic pulses with 100 μsec resolution in the period, or a 16 stage shift register is used to provide a $(2^{16}-1)$ length pseudorandom sequence. A 40 kHz single phase clock signal is input to the chip and all other clocks are derived from it.

3.2.2. Demultiplexer, Anti-logarithmic D/A, and Lowpass Filters

The sample and hold circuits and demultiplexing were implemented using MOS switches as gates and using MOS capacitors for storage. Precision gain is not required so buffer amplifiers in the sample and hold circuits are simply source followers. The lowpass filters employed are similar to those used in the speech analyzer described above. The lowpass filtered envelope is modulated by a bank of switches controlled by the excitation. These switches simply connect the bandpass filter inputs to the lowpass filter outputs when a pulse is desired and otherwise leave the bandpass inputs connected to a reference dc level.

3.2.3 Bandpass Filters

In the synthesizer the bandpass filter characteristics are simpler than those in the analyzer. They are simple complex pole pairs resulting in high Q resonant circuits with the same center frequencies as the corresponding analyzer channels. These characteristics would require approximately 150 stages in CCD transversal filters, but can be implemented with only two operational amplifiers and switched capacitors. Each filter implemented this way occupies only $.48$ mm^2 of silicon making it possible to build the entire synthesizer IC in approximately 32 mm^2, including all clocks, the D/A, the excitation pitch counter and noise generator, the filters and the summing output amplifier.

In order to understand the switched capacitor bandpass filter operation we examine first a conventional integrator, then a sampled data integrator and its z-transform, and finally a second order section will be described. Following the analysis of reference 7, a conventional analog integrator is shown in Figure 11a. Its transfer function is

$$H(\omega) = - \frac{1}{j\omega R_1 C_2} \qquad (1)$$
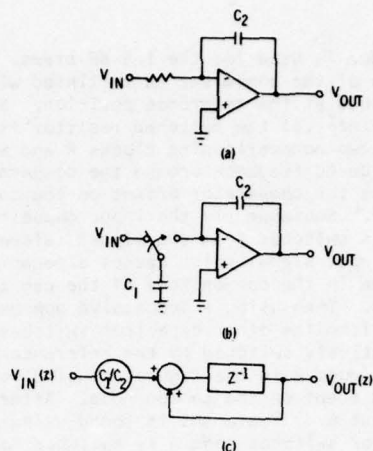
Figure 11. a) Conventional RC integrator, b) Sampled data integrator, c) Z-transform of integrator in (b).

In Figure 11b we have replaced R_1 with a double throw switch and capacitor C_1. This circuit operates in a sampled data mode with the switch alternating at a clock period T_C between the left hand position shown in Figure 11b to the right hand position. In the nth clock cycle, the capacitor C_1 is first charged to the voltage $v_{in}(n T_c)$ is effectively transferred to capacitor C_2. The following difference equation describes the process.

$$C_2 \, v_{out}[nT_c] = C_2 \, v_{out}[(n-1)T_c] - C_1 v_{in}[(n-1)T_c] \qquad (2)$$

The z-transform for this circuit can be written in the form

$$H(z) = - \frac{(C_1/C_2) \, z^{-1}}{1 - z^{-1}} \qquad (3)$$

which can be recognized as the equivalent of a digital integrator.

This integrator forms the basis of many possible filter configurations. [7, 10] The one selected for this application is shown in Figure 12. Two integrators can be seen in the figure. One is formed with the capacitors $a_L C_L$ and C_L and the other by $a_c C_c$ and C_c. A sign inversion is accomplished by adding a second switch to the bottom plate of capacitor so that the polarity can be reversed

when discharging this capacitor into its corresponding integrator. The z-transform of this circuit can be written as

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{-\alpha_i \alpha_c (z-1)}{z^2 - (2-\alpha_c\alpha_T-\alpha_c\alpha_L)z + (1-\alpha_c\alpha_T)} \quad (4)$$

We can see from the z-transform that the frequency response is independent of the absolute values of either C_c or C_L, but depends only on the capacitor ratios α_c, α_L, and α_T. MOS fabrication techniques allow the control of such capacitor ratios to a precision on the order of 0.1% which is adequate for many filtering problems including the one described here.
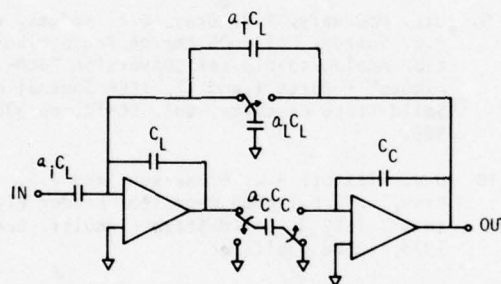
Figure 12. Two pole bandpass filter using switched capacitor integrators.

3.3.4 Operational Amplifiers

The key to successful switched capacitor filters is an NMOS operational amplifier with low power and small silicon area. Recently various NMOS amplifier designs have been reported [11, 12] and the design of the amplifier used in the bandpass filter has incorporated ideas from the previous designs. However,

this amplifier was optimized for small silicon area and low power. The amplifier circuit topology is shown in Figure 13. The principle specifications are listed in Table I. There are 41 of these amplifiers on the speech synthesizer IC.
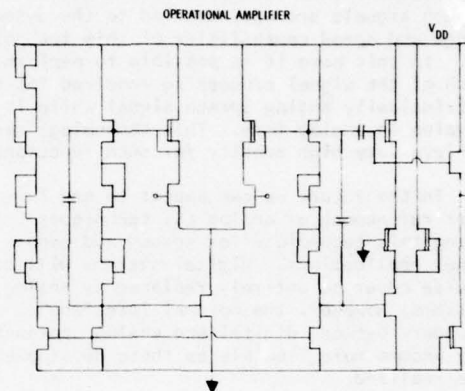
Figure 13. NMOS Operational Amplifier

TABLE I

Operation Amplifier Characteristics

Power	4.3 mW
Gain open loop	1800
Bandwidth	1.6 MHz
Slew rate	2.2V/μsec
Load	10 pF
Phase Margin	56°
Silicon Area	.09 mm^2

4.0 Summary

CCDs and the complementary and compatible switched capacitor filter technology show promise in lowering system size, cost, and power. The two custom analog LSI circuits described in this paper make possible a highly integrated, potentially low cost solution to the vocoder problem. There are many other system problems utilizing speech analysis and/or synthesis in which these ICs could find application, thus further lowering costs. Speech signals are well matched to the dynamic range and speed capabilities of this technology. In this case it is possible to perform much of the signal processing required for the intrinsically analog speech signal while it remains in analog form. This technology can achieve very high density for such functions.

In the future we can expect to see further refinement of analog LSI techniques using this technology for speech and many other applications. Digital systems will of course never be entirely replaced by analog systems, however, the optimal interface boundary between digital and analog approaches may become more flexible as these developments are realized.

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Digitally controlled adaptive CCD filter

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Abstract

The computation and setting of the coefficients of adaptive CCD transversal filters can be delegated to a microprocessor. The information required for setting the filter coefficients is put out in digital form. For the adaptive CCD transversal filters known so far, D/A converters have to be used to convert this information into analog values by which the input signal can be multiplied.

Thus a new adaptive filter was implemented using a CCD transversal filter with parallel-in/serial-out configuration in combination with a digitally controlled weighting scheme for the various filter coefficients. At each input stage a charge packet proportional to the input signal is transferred n times to the collecting CCD electrode, where the number n of transfers determines the tap weighting of each coefficient. With this configuration a combination of analog and digital multiplication was realized. This filter can thus be advantageously combined with microprocessors.

The concept for a novel solution of this type, the realized configuration and the mode of operation of the D/A converter in the input stages of the CCD will be described below. Measurements on an implemented filter network with 25 digitally controlled coefficients are reported and discussed.

1. Introduction

Whereas for many applications it is possible to specify a fixed frequency response for a filter network, it is in other cases more practical not to adapt the filter unless it is to be used for a specific problem and then if necessary to adapt it again if the input parameters change. Such requirements are encountered for instance with modems if the data signals transmitted over the telephone line have to be equalized /1,2/. Whereas with small systems it is still possible to adapt the filters by hand, this would no longer appear practical for fast and complex filter networks. In such cases a filter can only be meaningfully used in conjunction with a main processor capable of executing the algorithm for the filter calculations at sufficient speed.

For electrically controllable filters such as those known from the literature /3/ the digital information of the main processor has to be converted by D/A converters /4/ to allow multiplication with the signal value. If however a CCD transversal filter with parallel-in/serial-out configuration is used, the digital information can be used for directly controlling the input stages. The required D/A conversion is here delegated to the CCD in the sense that a charge packet proportional to the signal value is read repeat-

edly into the CCD channel from each input stage in correspondence with the digital information for the respective input.

2. Overall system

The various circuit elements required for an adaptive filter system are shown in Figure 1. The overall system is controlled by a microprocessor. A first approximation for the filter coefficients is created by the microprocessor and then written into the various storage registers. During this process the various registers are individually accessed via the address bus and the decoder, and the value of the respective filter coefficient, e.g. an 8-bit value, is read in over the data bus. The information stored in the registers is now compared by comparators with the count of a counter which counts during the time interval between two sensed values of the input signal up to a specified number 2^m. This number determines the maximum possible number of read-in pulses per read-in cycle. If the count is greater than the actual value in one of the register, the output of the respective comparator is cut off, thereby blocking the connected CCD input. The value of this coefficient is in this way determined by the clock pulses before the comparator is disabled.

This allows a close connection between the microprocessor and the adaptive filter. The only connecting links required are the decoder, the storage register and the comparators. A rough estimate of the real estate required for an integrated implementation of these connecting elements for a filter with 50 coefficients is 2 mm². In order to be able to read the information required for the optimization into the microprocessor, a link has to be established between the filter and the microprocessor by way of an A/D converter. The microprocessor must have a suitable algorithm allowing the fast

computation of the optimum coefficients for a given problem. The computation only requires weighting with "+1" and "-1" and additions /2/, i.e. arithmetic operations which are relatively fast in comparison with digital multiplications.

For improving the filter characteristics the value of one or more coefficients supplied by the microprocessor can be read selectively into the register and the result of this alteration recorded at the filter output and evaluated anew.

3. Realized configuration

Realization of the proposed adaptive filter system is based on the assumption of the availability of a large variety of suitable microprocessors. Decoder, register and comparators can be in form of discrete devices or integrated on the chip according to available solutions. Thus only the CCD transversal filter with parallel input stages in which D/A conversion takes place (Figure 2) was implemented. The filter is controlled via external comparators, a register and a counter.

A CCD for 4-phase operation with 43 elements was implemented in two-layer Poly-Si gate technology on a real estate area of about 2 x 3 mm². The CCD electrodes have a lenght of 10 μm; on both sides of every fourth CCD electrode there is an input stage with an electrode area of 5 x 5 μm². Two parallel input stages are required in the implemented system to allow the positive or negative weighting of the input signal according to need. To simplify the control of the system the coefficients were interconnected symmetrically with reference to the center. This results in filters with a constant group delay. The output signal of the filter can be sensed either as a charge packet or, via a source follower, as a voltage. An external amplifier has been added behind the source follower so that the signal can be amplified accor-

ding to need.

4. Structure of input stage

4.1 Realized input stage

The realized form of the input stage is shown in Figure 3. The charge is applied by the fill-and-spill method /5/. Each input stage consists of an input diode I_D, two gate electrodes G1 and G2 (see Figure 4) at which there is either the signal or a bias voltage, and the gate electrode G3 with which the number of charge packets to be applied is determined. To realize a positive or negative sign /6/ for the various coefficients one of the two different bias voltages B1 or B2 can be applied to the bias line, which for inputs associated with a CCD electrode is connected on one side of the channel to G1 and on the other side to G2. When the bias voltage B1, which is smaller than the minimum voltage of the input signal, is applied, no charge is able to flow into the input seen on the right in Figure 3b. On the left however a charge packet builds up and is transferred in the CCD channel, which is proportional to the signal, with the result that a positive sign is obtained. If the bias voltage B2, which is larger than the maximum voltage of the input signal, is applied to the bias line, no charge will flow into the input on the left in Figure 3c, whereas a charge packet builds up on the right that is inversely proportional to the input signal, with the result that a negative sign is obtained.

4.2 Input stage with positive and negative weighting

As an extension of the realized solution it would appear practical to realize the input such that both positive and negative coefficients can be realized with one input stage so that each register can store not only the value of the respective coefficient but also its sign with a single bit. A simple logic configuration (Figure 4) can

then be used for applying either the signal or one of the two bias voltages B1 and B2 to the gate G1 or G2 in order to obtain the desired sign.

5. D/A converter

5.1 Mode of operation of D/A converter

Multiplication of the input signal by the values supplied by the microprocessor takes place in the parallel input stages of the CCD. The input signal is sensed at the beginning of the read-in cycle and its value determined. Charge packets proportional to the value of the sensed signal build up in the various input stages and are shifted into the CCD channel. The time required for reading in a charge packet depends on the geometry of the input stage. For the chosen input stage with an electrode lenght of 5 μm it is, according to /7/, theoretically possible to realize a read-in frequency of the order of 8 MHz with an accuracy of 8 bit. Measurements showed however the amplitude of the output signal to diminish at read-in frequencies above 2 MHz. This effect is mainly due to the clock voltages showing up distortions at these high frequencies.

5.2 Calculation of accuracy of D/A converter

The quality of the D/A converter depends not only on its read-in time, which is given by its geometry, but also on the time of the read-in cycle. This time is determined by the CCD clock frequency. The accuracy of the D/A converter can be determined on the basis of the knowledge that if an asymmetrical CCD clock program is chosen about 80 % of a clock cycle will be available for read-in. To realize a D/A converter with 8 bit accuracy, for instance, the CCD clock frequency for a read-in frequency of 8 MHz can not be above 30 kHz.

Measurements with our test circuit

were unable to show this result be-
cause the input frequency was
limited to 2 MHz and, as the coeffi-
cients were externally controlled,
no more than a hundred read-in
pulses could be set.

6. Linearity of input stage

For investigating the linearity of
the input stage of the realized
configuration both the amplitude
and the dc voltage component of the
input signal were varied and the
number of charge packets read into
an input stage was altered.

6.1 Linearity as a function of the input signal

For investigating the linearity of
the input stage as a function of
the input signal, the output signal
was measured as a function of the
value of the input signal for both
positive and negative coefficients.
Figure 5 shows linearity to exist
in the region between the two bias
voltages $B1 = 1$ V and $B2 = 3$ V.

For obtaining a precise measurement
of the linearity a sinewave signal
with an amplitude of 0.25 V was
applied and the dc voltage super-
posed on the sinewave was varied
between 1 and 3 V. The measured
separation between the fundamental
(f_1) and the second (f_2) and third
(f_3) harmonics is shown in Figure
5b, c for both a positive and a
negative input stage. The maximum
seperation between the fundamental
and the second harmonic for both
the positive and the negative in-
put stage was measured to be 42 dB.
It is felt that this is mainly due
to the minimum geometry of the input
stages.

6.2 Linearity as a function of the number of read-in pulses

The relation between the value of
the output signal and the number of
charge packets transferred from an
input stage into the CCD channel
per read-in cycle was also measured.
For this purpose a dc voltage of 2 V
was applied to the input and the

number of read-in pulses varied
between 0 and 99 (Figure 6). These
measured points fit the transfer
characteristic of the output stage -
measured with a seperate method -
very well.

7. Realization of a lowpass filter

To demonstrate the applicability of
our circuit concept to filters a
lowpass filter was realized. The
required filter coefficients were
determined with the aid of a com-
puter program /8/ and then rounded
off to integral values between -99
and +99. To simply control of the
filter only 25 of the 43 realized
coefficients were used. The filter
was operated with a clock frequen-
cy of 10 kHz. According to the
calculations (Figure 7a) the devia-
tions in the passband of 0 to 1 kHz
should be smaller than $\pm$ 0.1 dB and
an attenuation of at least 32 dB
should be present in the stopband
starting at 2 kHz.

The recorded curves in Figure 7b
show this response to have been
satisfactorily realized in the pass-
band. Although the attenuation in
the stopband agrees with the calcu-
lations, a discrepancy is to be no-
ted between the computed and the
recorded curves. This discrepancy
is probably influenced by inaccuracy
of the filter coefficients and by
transfer inefficiency within the
CCD.

The agreement between the recorded
and the computed curve can be de-
monstrated more clearly by choosing
an example in which the attenuation
in the stopband is smaller. A
corresponding frequency response
was calculated by increasing the
absolute value of all the coeffi-
cients by three read-in pulses per
cycle. The choice of these non-
optimum coefficients leads to vari-
ations in the passband of $\pm$ 1 dB and
the attenuation in the stopband is
now no more than 22 dB. This may be
seen from both the calculated fre-
quency response (Figure 8) and the
recorded curve, which is consistent
with the calculated values.

To measure the linearity and random noise of the adapted filter a sine-wave signal with an amplitude of 0.5 V on which a dc voltage of 2 V was superposed was applied to the input of the filter, whose frequency response is shown in Figure 7. A separation of about 40 dB between the fundamental and the second and third harmonics was measured (Figure 9). The random noise was measured with only the dc voltage of 2 V at the input; for a window of Δf = 300 Hz the random noise was 64 dB below the signal amplitude.

8. Concluding remarks

The described digitally controlled filter is a transversal filter that is particularly suitable for combination with the microprocessor. According to the theoretical calculations it is possible, assuming a clock frequency of 30 kHz, to realize a D/A converter with 8 bits in the input stages of the configuration. Using this configuration a lowpass filter with an attenuation of more than 42 dB was implemented. In order to expand the configuration into an adaptive filter system the possibility of integrating the required connecting links such as the decoder, the register and the comparators on a single chip is being contemplated as the next step.

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Fig 1 Overall system of an adaptive filter network

Fig. 2 Digitally-controlled CCD transversal filter as test device with 43 coefficients

Fig. 3 Input stage
a) Realized configuration
b) Bias voltage B_1 + signal voltage U_S = positive sign
c) Bias voltage B_2 + signal voltage U_S = negative sign

Fig 4 Drive circuit for input stage with positive or negative sign

Fig 5 Linearity of input stage
a) Input characterics for positive and negative input stage
b) Linearity of positive input stage $\hat{u}_S \cdot 0.25$ V
c) Linearity of negative input stage $\hat{u}_S \cdot 0.25$ V

Discrete Functions	Transformation
	Convolution
	Cross-correlation
	Auto-correlation
	Fourier transform
	Fourier transform
	Fourier transform

Fig. 8 Calculated and measured frequency response of a filter with non-ideal coefficients

Fig. 6 Measured output voltage as function of the number of read-in pulses
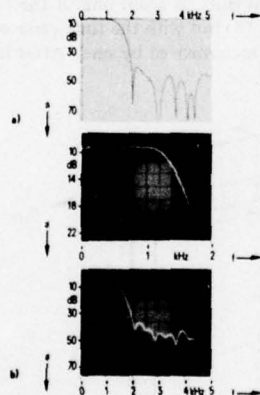
Fig. 7 Realized lowpass filter
a) Calculated frequency response
b) Measured frequency response in passband and stopband
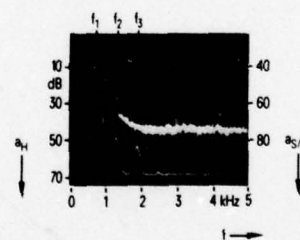
Fig. 9 Harmonic attenuation a_H and signal to noise ratio $a_{S/N}$ (noise per 300 Hz) of a realized lowpass filter

Some of the forms of the matrix $h_{m,n}$ used to perform various linear transformations are

Impulse Response	Transformation
h_{m-n}	Convolution
h_{n-m}	Cross-correlation
f_{n-m}	Autocorrelation
$\cos(2\pi mn)$	Cosine transform
$\exp(-2\pi imn)$	Fourier transform
$\exp(-mn)$	Laplace transform
$2\pi J_o(2\pi mn)n$	Hankel transform

The EOP, as shown schematically in Figure 1, performs any of these transformations as determined by the mask inserted between the LED and the CCD. That is, each of the M columns of the mask and CCD performs one of the M sums of products of Eq. (3). The following paragraphs qualitatively show the EOP's operation. References 4 and 5 contain a more rigorous analysis.

In the EOP, the multiplications indicated occur as light passes through a partially transparent mask containing the matrix $h_{m,n}$ as its transmittance function. The intensity of the light emanating from the mask is indeed the product of the irradiance of the original light and the intensity transmittance of the mask. Summation occurs through the ability of the CCD to convert these photons into charge packets, with a direct linear relationship between total light impinging on a cell and the amount of charge accumulated. By shifting the charge packets vertically upward by one resolution cell per input sample to the

LED, addition of the proper terms through the addition of these charge packets is accomplished.

To illustrate the principal of operation consider the most trivial cases in which M = 1 (i.e., consider only a single column of the mask and CCD) and N = 3. The light source is consecutively intensity modulated by three input samples f_1, f_2, and f_3. This light illuminates a mask with transmittance values h_1, h_2, and h_3 and falls upon the three CCD cells c_1, c_2, and c_3. Since the incoming light floods the mask, at the end of the first period the charge in cells c_1 through c_3 is proportional to f_1h_1, f_1h_2, and f_1h_3 respectively. After a shift of packets from c_1 to c_2, c_2 to c_3, and from c_3 out to the horizontal shift register, and another flood illumination by the input signal f_2, the charge in cells c_1 through c_3 is proportional to f_2h_1, $f_1h_1 + f_2h_2$, and $f_1h_2 + f_2h_3$. Another shift and illumination yields three charge packets proportional to f_3h_1, $f_2h_1 + f_3h_2$, and $f_1h_1 + f_2h_2 + f_3h_3$. Upon the next shift, this last value is shifted into the horizontal shift register and read out of the CCD. It should be recognized as one of the sums of products of Eq. (3). By extension, it can be seen that an M $\times$ N resolution-cell CCD, with an appropriate mask can be used to generate a series of M sums of N products.

To continue the trivial example considered above, if a fourth input sample modulates the LED and a fourth shifting of charge packets takes place, the resulting values in c_1 through c_3 will be proportional to f_4h_1, $f_3h_1 + f_4h_2$, and $f_2h_1 + f_3h_2 + f_4h_3$. This last value, which will be read out of the CCD on the next vertical shift, is again one of the sums of products of Eq. (3) but with the time variable of the input sequence incremented by one. After the initial
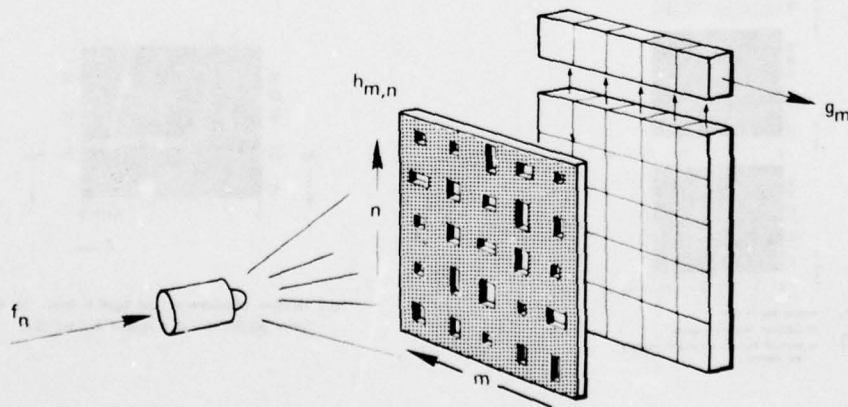
Figure 1. An Electro-Optical Processor (EOP).

THE EOP – A CCD-BASED ELECTRO-OPTICAL PROCESSOR

Anthony C.H. Louie   Keith Bromley   Thomas E. Keenan

Naval Ocean Systems   Naval Ocean Systems   Naval Ocean Systems
Center   Center   Center

Introduction

The electro-optical processor (EOP) developed by the authors is a compact, flexible device designed for use in many signal processing applications. Prior advances have been described in references 1–6. This paper will provide an overview of the history and mathematical basis of the device, present the current state of implementation, and indicate promising new investigation areas.

The EOP consists of an incoherent light source (e.g., an LED), a photo-generated mask, and an area-array charge coupled device (CCD). The package which encloses these elements is approximately two cubic inches in volume. Supporting circuitry is contained on three printed circuit cards. The current implementation is capable of performing 5×10^9 analog multiplications per second.

Development History

During the mid-1960's the scientific literature on optical signal processing emphasized the usefulness of *coherent* optical methods in performing various mathematical operations such as two-dimensional Fourier transforms and matched spatial filtering. Investigations in this regard have continued, at an increasing pace, with good results achieved. Somewhat later, investigators, disturbed by the expense, size, and critical environmental controls usually necessary in coherent systems, recognized that in some applications a non-coherent approach could be substituted. This involves simply decomposing all complex bipolar signals and operations into their real non-negative parts, as is done in digital computers, thereby eliminating the need to operate directly with complex quantities.

Early in the development of non-coherent optical processors, systems utilizing television cameras and line-array CCD's in conjunction with oscillating mirrors were successfully demonstrated.[1,2,3] The availability of area-array CCD's operating in the shift-and-add (or time-delay and integration) mode permitted removal of the oscillating mirrors.[4,5,6] But even with this elimination of the mechanical moving parts these experimental systems still required a significant amount of space to accommodate the condensing and imaging optics necessary to image the mask onto the face of the CCD. Now, the masks are fabricated directly onto the CCD obviating the need for any lenses and thereby allowing non-coherent processing modules to be packaged in just a few cubic inches.

Mathematical Basis

The generalized equation for a linear transformation

$$\int h(m,n)\, f(n)\, dn = g(m) \qquad (1)$$

can be rewritten in its discrete form as

$$\sum_{n=1}^{N} h_{m,n} f_n = g_m \quad . \qquad (2)$$

This can be further stated as a series of sums of products,

$$\sum_{n=1}^{N} h_{1,n} f_n = g_1 \quad ,$$

$$\sum_{n=1}^{N} h_{2,n} f_n = g_2 \quad ,$$

$$\vdots$$

$$\sum_{n=1}^{N} h_{M,n} f_n = g_M \quad . \qquad (3)$$

start-up transient, each new input sample to the EOP produces a set of sums of products terms of Eq. (3) but where the summation takes place over the *previous* N input samples. In other words, the EOP performs *sliding-window* transformations. Or, in a pattern recognition operation, the EOP generates the complete cross-correlation *function* (i.e., the cross-correlation *value* for all time delays) between the input and each member of the library of reference signatures on the mask.

It was mentioned earlier that signal decomposition was required in those classes of linear operations which call for both real and imaginary and/or positive and negative components. In the EOP, this decomposition is achieved by using separate areas of the mask for each component, and by biasing the light source, with the results appropriately combined by electronic circuitry at the output of the CCD.[6]

Current State Of Development

In 1977, RCA Laboratories (David Sarnoff Research Center, Princeton, New Jersey) under contract to the Naval Ocean Systems Center (San Diego, California) fabricated masks onto RCA's commercially available model SID 52501 CCD. These devices have N = 512 by M = 320 resolution cells on 1.2 mil centers. The first step in the process was the preparation of a photolithographic mask containing the desired 512 by 320 element matrix of apertures $h_{m,n}$. The remaining steps consisted of (1) depositing a protective oxide layer on the CCD structure, (2) depositing an opaque 1200 Å thick chromium film onto this layer, (3) imaging the photolithographic mask onto this film and etching away the mask apertures using standard photoresist techniques, and (4) covering the resulting device with a protective 10,000 Å thick SiO_2 layer. The range of aperture sizes achieved in this effort was 100 discrete distinguisable levels and improvements in the technique are in progress to push this to about 256 discrete levels.

Figure 2 shows a corner of the resulting "masked CCD". It is interesting to note the three-phase electrode structure of the horizontal shift register at the top of the photograph and the electrode structure (3 electrodes per resolution cell) of the vertical registers showing through the transparent apertures of the mask.
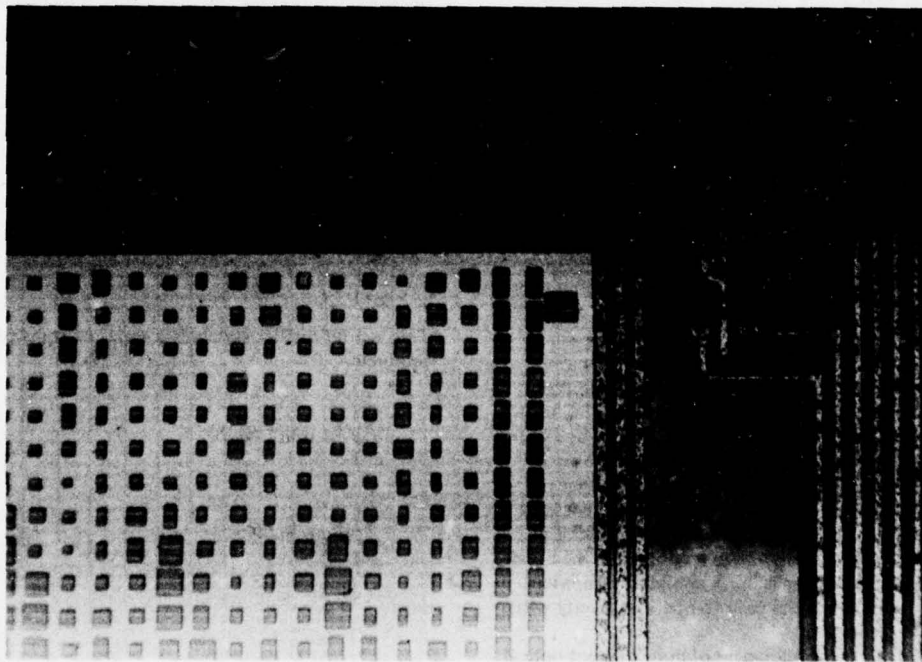
Figure 2. Photomicrograph of a corner of the mask/CCD combination.

With such a "masked CCD" the only remaining component in Figure 1 is the illumination device. Successful results have been obtained with the Monsanto MV-4 visible LED. The housing which holds the LED and CCD also serves as an optical cavity to help provide a uniform illumination across the CCD surface. Several optical cavity geometries are currently being theoretically and experimentally investigated with respect to maximizing uniformity and efficiency in a minimum size. As discussed more fully in reference 7, both the cylindrical and spherical geometries with appropriately placed baffles appear capable of reducing illumination nonuniformities across the CCD surface to under 1% in a housing size of 2 cubic inches.

This processor, with a cylindrical cavity geometry, is currently being tested and evaluated. Factors which adversely affect performance and which therefore need to be measured and controlled, are

- LED linearity,
- spatial uniformity of illumination,
- CCD spatial variations in sensitivity,
- optical crosstalk between CCD cells
- CCD charge transfer efficiency, and
- CCD dynamic range.

Expected performance parameters are

$$v_{in} = v_{ver} = 32,000 \text{ samples/sec}$$
$$v_{hor} = 10,240,000 \text{ shifts/sec}$$
dynamic range > 50 dB, and
nonlinearity $< 1\%$.

Such a processing module has a processing rate of $32,000 \times 512 \times 320 \approx 5 \times 10^9$ multiplications/sec.

The following section discusses the external circuitry designed to drive this EOP unit. No attempt has been made to miniaturize this circuitry; instead the intention has been to produce a general-purpose module in which changes in timing and operation could be incorporated by simple rewiring or changing a few components without the need for new printed circuit boards. This modular design approach, in which the circuitry used to operate the EOP as, say, a Fourier transformer is only a slightly modified version of that used to operate the EOP (with a different mask) as, say, a multi-channel cross-correlator, has saved considerable time in fabricating and verifying new processing systems.

An Overview of System Implementation

In the present implementation, the external circuitry required to operate the EOP is partitioned into three functional subsystems. These are: (1) master timing, (2) processor driving, and (3) signal conditioning. As their names imply, the master timing circuit provides the required synchronization signals for the overall system, the processor driver controls the LED operation and generates the necessary clocking waveforms for the CCD, and the signal conditioner refines the CCD read-out to be suitable for display and/or further processing. Each subsystem occupies one 10 in. by 4 in. printed circuit card. In the following paragraphs, the function and design of each card is described in detail.

Master Timing

There are two functions for the master timing card. First, it defines the clocking intervals for CCD operation. Therefore in this respect, the design is device dependent. The RCA CCD (SID52501) employed requires both vertical and horizontal clocks to operate. The alternating intervals of vertical and horizontal clocks comprise the Horizontal Gate as shown in Figure 3. The vertical clock is active only between the horizontal clock intervals.

Secondly, the master timing provides the markers required to relate the CCD read-out to the mask columns or references. The CCD read-out is the computational result, g_m, from the EOP; that is, it is a sequence of M-element vectors in the form of

Figure 3. Horizontal Gate.

a time-varying analog waveform. These markers enable the system to recognize which point in time on this analog waveform represents the result of the running sum of products of the input sequence f_n and the mth mask column. The numbers and kinds of timing markers required are application dependen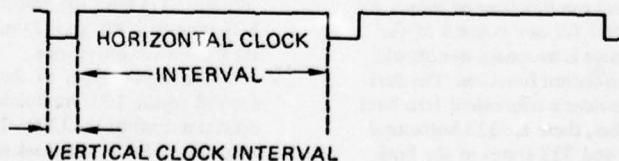t. The card under discussion is designed for general-purpose usage, in that only minor wiring modifications are required to provide the markers appropriate for, for example, spectrum analysis, finite impulse response (FIR) filtering, or cross-correlation operations.

This card provides the following outputs:

(1) Horizontal Gate, shown in Fig. 3. This defines the active horizontal clock interval with a duration of 323 horizontal clock pulses and the active vertical clock interval with a duration of 7 horizontal clock pulses. (Each horizontal or vertical clock pulse results in one shift along the horizontal or vertical register respectively. However, as will be discussed later, a vertical clock pulse occupies 7 horizontal clock periods.)

(2) Valid Row Gate. This defines the location of the desired rows of the CCD output. In many applications only certain rows of outputs are wanted. For example, in an EOP performing a 512-point Fourier transform with a 75% window-overlap factor, only every 128th row of output Fourier coefficients, g_m, would be desired.

(3) Valid Column Gate. This defines the location of the desired columns in the CCD read-out line. In many applications, only a specific sequence of columns are wanted. For example, in a spectrum analyzer, one may be interested in only a subset of the frequency components, or in a cross-correlator, one may wish to ignore the columns used to obtain normalization constants and zero levels.

(4) Normalization & Dark-Level Pulses. These are time signals indicating where the normalization value and dark-level value occur on a line basis. The former is simply the sum of the previous N samples of the input signal and can be obtained simply by letting $h_{m,n} = 1$ for one column of the mask. This value is necessary in normalizing a cross-correlation function. The dark-level value provides a convenient zero level. As stated earlier, there are 323 horizontal clock pulses, and 322 states in the horizontal register of the CCD. The one extra clock pulse is for shifting out the video

black level (containing only thermally generated "dark current") to be used for dc restoration.

(5) Frame Synchronization Pulse. This occurs at the start of each 512-line frame and has a duration of one line (i.e., one period of the Horizontal Gate). A Frame Time is the time required to shift a charge packet from the bottom to the top row of CCD cells. When the electro-optical processor is operated in the so-called TV mode, for initial check out purposes, the Frame Synchronization Pulse is used as the input to the LED so that the LED flashes on only once during the entire frame. Conveniently, this results in an image of the mask being read out from the CCD (i.e., each mask column has been correlated with a Dirac delta function thus the correlation output is the mask pattern itself).

The circuitry to provide these outputs is shown in Figure 4. It consists of two sections: the horizontal clock section and vertical clock section — each composed of counters, decoders and combinatorial logic.

The basic horizontal timing is maintained by a set of horizontal counters. They provide 330 distinct clock periods. With this configuration, any of the 330 clock periods composing the line can be pinpointed by the use of decoders and logic circuits. In this manner, the various horizontal timing signals are generated. Furthermore, the horizontal section produces a vertical pulse occurring at the line rate. This pulse is used to increment the line counters in the vertical section to maintain 512 distinct line periods. The counter output is decoded to produce the Frame Synchronization Pulse and the Valid Row Gate. Additionally a high frequency clock running at four times the horizontal clock frequency is available for producing the three-phase horizontal clocks in the processor driver card.

Processor Driver

The second card, called the processor driver, contains: (1) the LED modulation circuitry, (2) the EOP module itself, and (3) the circuitry to generate the CCD drive waveforms.

The input signal to the processor system is applied to the LED modulator which controls the optical output of the LED. The EOP module contains the LED and the masked CCD enclosed in an optical cavity, as described in an earlier section. The waveform circuitry is divided into the horizontal and
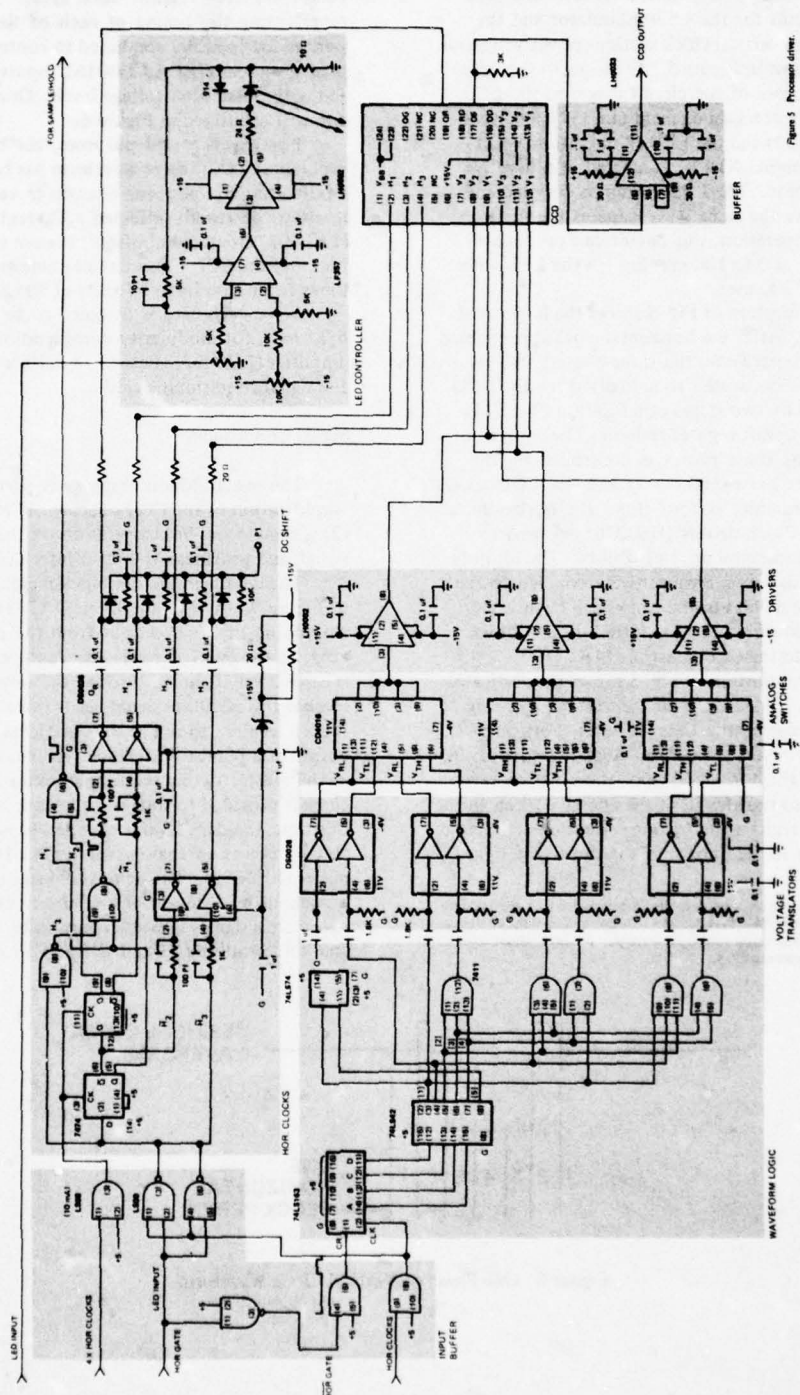
Figure 5 Processor driver.

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vertical clocking sections. The former produces the three-phase, two-level horizontal clocks and the latter produces the three-phase multi-level vertical clocks.*

The circuit for the LED modulator and the horizontal and vertical clock sections of the processor driver are shown in Figure 5. As shown in the upper right hand corner of the circuit diagram, the LED driver consists of a gain element (LF357), a current driver (LH0002) and the LED (Monsanto MV4 or Texas Instruments XL12) connected in a negative feedback fashion. The LED current is sampled and forced to have the same waveshape as the input voltage. In operation, this circuit can produce a current pulse of 0 to 100 ma through the LED with a rise time of 200 nsec.

The top portion of Fig. 5 shows the horizontal clock section. After the horizontal clocks are enabled by the Horizontal Gate, the three-phase two-level clocking waveforms used to actually drive the CCD are generated by two stages of a flip-flop (74LS74) connected in a shift-register fashion. The amount of overlap among these phases is controlled by the phasing of the horizontal clocks and the 4X clocks (i.e., clocks running at four times the horizontal clock rate). Clock drivers (DS0026) are used to provide the horizontal drive capability. The outputs of the clock drivers are capacitively coupled to the CCD so that a dc bias to the clocks can be inserted. The entire waveform can be shifted up and down with respect to the CCD substrate bias.

The lower portion of Fig. 5 shows the vertical clock section. Each cycle of the vertical clocking waveform occupies the time of seven horizontal clock periods. Thus the vertical clock period is seven times that of the horizontal clock (i.e., It takes seven times longer to transfer all of the charge packets in the CCD vertical registers up by one resolution cell than to transfer those in the horizontal register to the right by one cell).

*The processor driver circuitry described herein is designed for use with the aforementioned RCA SID 52501 CCD. For a more detailed discussion of the required waveforms than space permits here, please refer to the RCA specifications sheet.

The Horizontal Gate enables a binary counter to maintain the seven district horizontal clock periods comprising each vertical clock cycle. The signals representing the timing of each of these distinct periods are logically combined to control a set of four analog switches (RCA CD4016), inputs to which are fed with the desired voltage levels. One of such waveforms is illustrated in Figure 6.

For experimental purposes, the circuitry to generate the CCD drive waveform has been made very flexible thereby allowing changes in various voltage levels to be readily effected. Current amplifiers (LH0002) are used as buffers between the switch outputs and the CCD. This circuit exhibits rise and fall times from –2 volts to +7 volts of 50 nsec.

Since each card is designed to be an independent unit, for modularity considerations, a buffer amplifier (LH0033) is used to interface the CCD with the signal conditioning card.

Signal Conditioner

The signal conditioning card performs: (1) amplification of the CCD output, (2) dc restoration, (3) a sample-and-hold operation on the amplified signal; and provides (4) output interfacing capability.

The detail circuit and block diagrams are shown in Figure 7. A vido amplifier (μA733) is used for amplifying the CCD output from the ten millivolt range to the one volt range. Since the CCD output is capacitively coupled through the amplifier, the dc level of this resulting signal needs to be re-established. It is convenient to utilize the dark level of the CCD output as a point of reference. As mentioned earlier in the master timing section, an extra horizontal clock is provided to shift out the dark level. During this time, the dark level is clamped to negative one volt by use of an analog switch (DG 187) and amplifier (LH0033). The dc restored signal is still contaminated by feed-through of the clocks, so these extraneous signals must be removed by using a sample-and-hold amplifier (Datel SHM-2) to obtain the
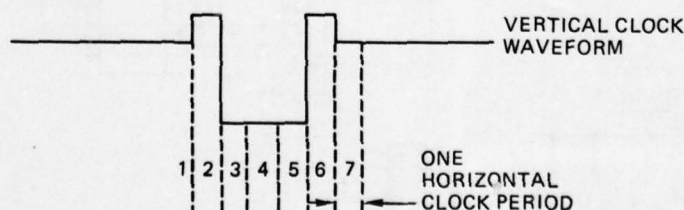
Figure 6. One Phase of Vertical Clock Waveform.
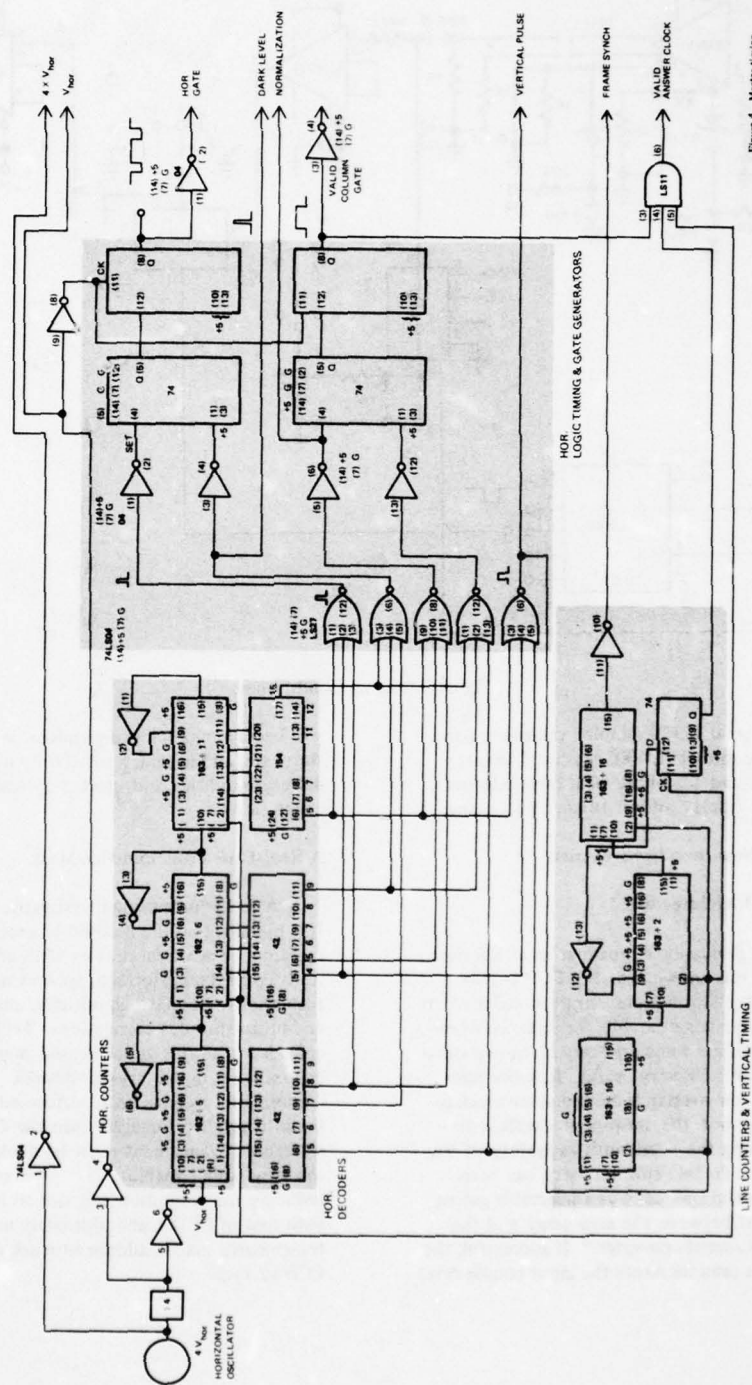
Figure 4 Master timing.

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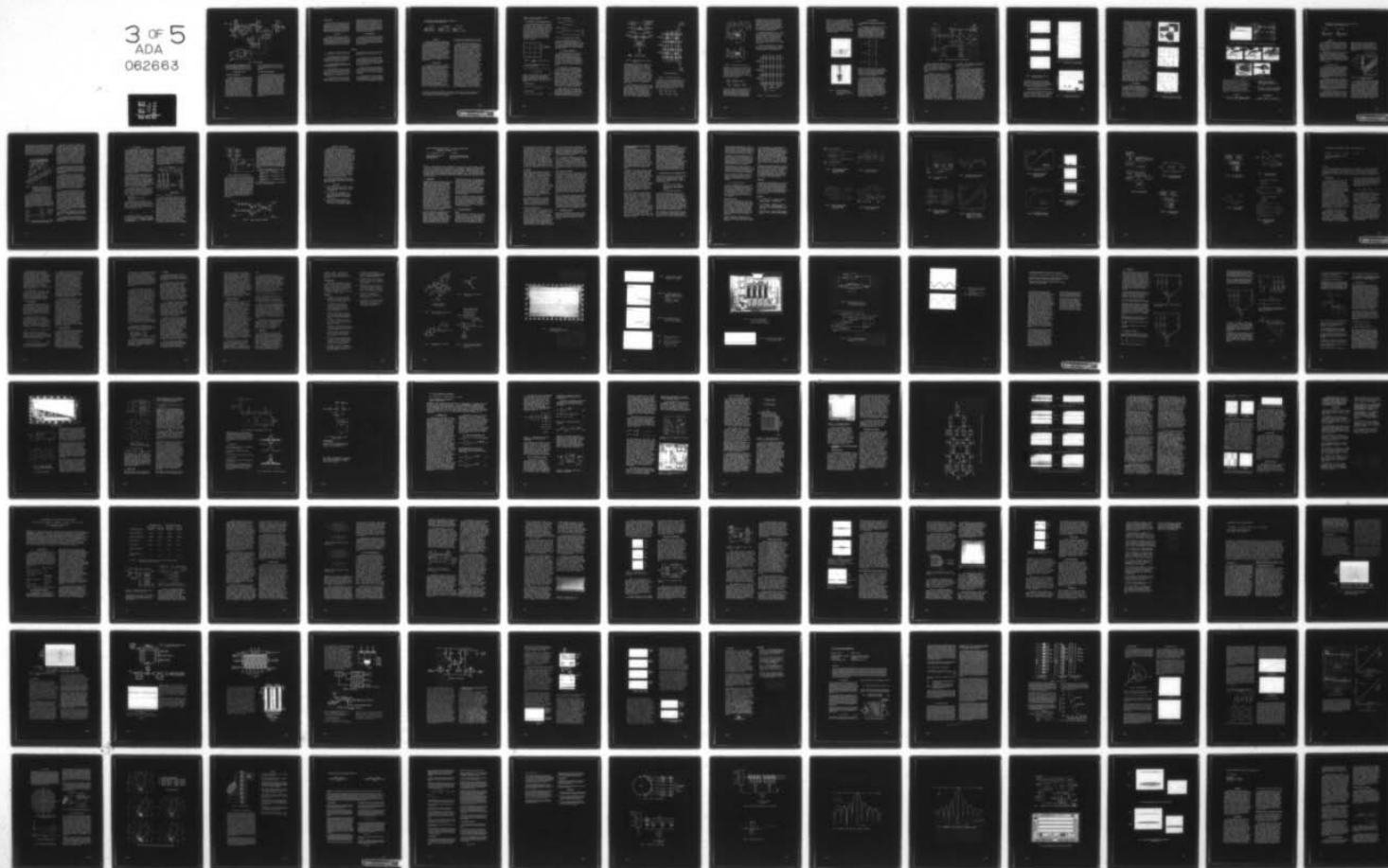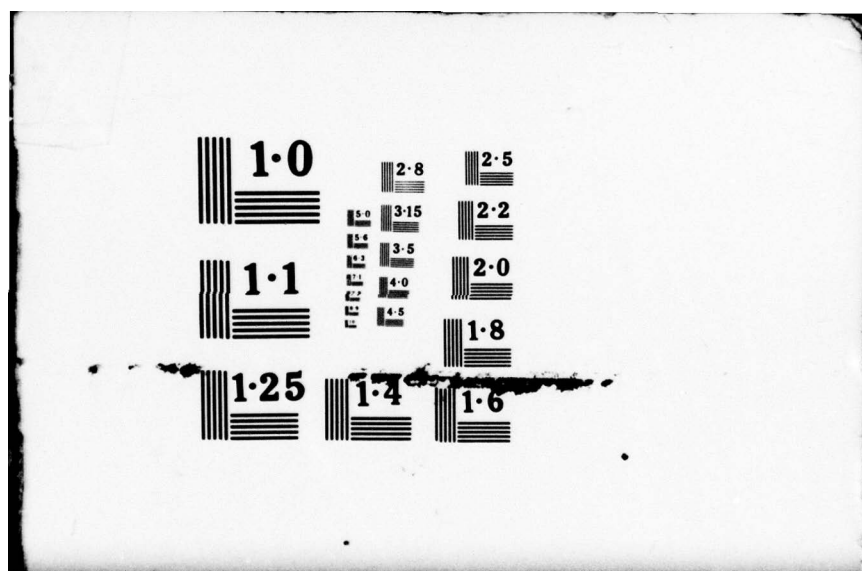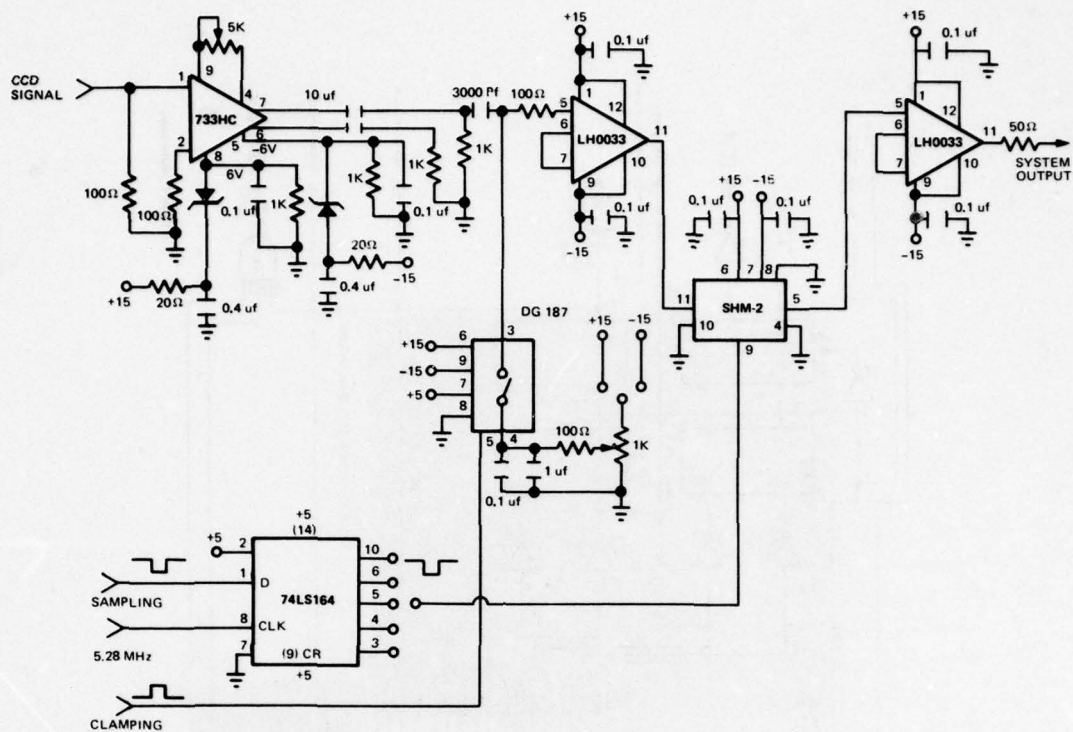
Figure 7. Signal Conditioner.

desired analog signal — 320 sampled values per row. Again a buffer amplifier (LH0033) is used to interface the sample-and-hold unit with any external load for output display and/or further processing.

New Investigative Areas

A Modified CCD Architecture

During the discussion of the mathematical basis for the EOP, it was shown that the EOP performs *sliding-window* transformations. In those cases where large window overlap is desirable, for instance when an incoming signal has some arbitrary unknown starting point, this feature is very useful. In those cases where little window overlap is desired some mechanism for flushing out the unwanted coefficients (thereby increasing the bandwidth capability of the EOP) is desired. To this end, industry has been approached for solutions, such as a selectable gating function inserted between the area array and the output parallel to serial converter.[8] If successful, the vertical shift rate (and therefore the input sample rate)

will become much less dependent on the horizontal shift rate, and in fact, limited only by CCD shift drive capabilities and electro-optical input signal generation.

A Real-Time Programmable Mask

Another promising investigative area is the mask. It is obvious that if a method of generating masks in real time or near real time existed, additional operations could be performed, such as non-linear transformations, recursive algorithms, adaptive solutions, and multi-stimulus correlations. Technologies being considered at this time include matrix-addressed transmissive liquid crystal devices. Laboratory demonstrations have been performed using a Hughes liquid crystal cell imaged onto the CCD, but considerable advancement must be made in expanding the grey scale capability (i.e., dynamic range), in reducing the resolution cell size to be compatible with that of CCD's, and ultimately in fabricating the transmissive matrix-addressed mask directly on the CCD surface.

Digital Capability

The last area to be discussed is that of digital operations with this unit. Historically, optical processing has been considered only applicable to analog problems with accuracies corresponding to about 8 bits, but work is proceeding with mask design and supporting algorithms to permit digital operations with any desired degree of accuracy.

Conclusion

The EOP is a compact, low-cost, low-power, high-speed signal processing module capable of performing a larger variety of useful linear operations with processing rates greater than 10^9 multiplications per second (depending on the array size and maximum vertical shift rate of the CCD used). General-purpose modules, each consisting of a two cubic inch EOP and three cards of external circuitry, have been fabricated and are now undergoing test and evaluation in a variety of application areas. Also, further development work is planned to increase the EOP's input rate from the present 32 kHz to the MHz range, to provide real-time programmability of the mask, and to allow the performance of digital operations with arbitrary accuracy.

Acknowledgements

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APPLICATION OF CHARGE-COUPLED DEVICE TECHNOLOGY TO TWO-DIMENSIONAL IMAGE PROCESSING*

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Abstract

This paper describes the application of charge-coupled device (CCD) technology to two-dimensional image processing. The processing operations discussed are widely used as preprocessing functions for more complex image understanding techniques. Algorithms such as edge detection, local averaging, and unsharp masking[1,2] have been implemented directly in the charge domain using extensions of the analog transversal filtering techniques previously demonstrated. The design concepts and circuit layouts are discussed together with the performance data on test imagery and "real-time" video.

1. Introduction

In the past several years, there has been a significantly increased interest in image enhancement and image understanding both for commercial systems (such as industrial inspection) and for military sensors. The processing algorithms and techniques developed have generally been implemented on general-purpose digital computers, and, in general, the processing times required to perform even relatively simple operations, such as local edge detection, have limited their use to non-real-time applications. The Sobel edge-detection scheme[3] described here, for example, requires approximately 5×10^6 operations per frame and might take 5 to 10 sec on a PDP-10 machine. This is two to three orders of magnitude slower than is required for "real-time" video (≈ 7.5 MHz).

Since low-level or preprocessing operations typically require the greatest computation time, one would generally want to use the preprocessor to dramatically reduce the data rate. This would allow the higher level operations (such as the so-called syntactic operations) to be performed at much lower throughput. The aim of this work is to investigate the feasibility of performing several commonly used preprocessing operations in CCD circuitry and thereby to increase the processing speed to allow real-time operation. CCDs were choosen both because they have inherently low power-delay products (which allow very high circuit densities) and because many modern sensors are themselves CCDs. In this way, the preprocessing functions might be incorporated directly into the sensor as options. This is the basis of the so-called "smart sensor" philosophy. The functions described here are edge detection, local averaging, adaptive stretch, binarization, and unsharp masking. The formulations of each of these algorithms is given in Section 2. Where appropriate, we have tried to structure the processing in the form of analog transversal filters to achieve optimal-speed and circuit density. This has required the development of two-dimensional filtering operations and novel circuit techniques to perform operations, such as absolute value determination, directly in the charge

domain. This should provide optimal dynamic range and linearity.

2. Definition of Processing Algorithms

Five preprocessing operations have been implemented. Each is based on a kernel of 3 x 3 pixels, shown in Figure 1. The first test circuit is a CCD implementation of the Sobel edge-detection algorithm.[3] This circuit was chosen because it demonstrates two operations important to image processing: (1) the possibility of achieving a two-dimensional convolution with arbitrary weightings and (2) the ability to perform nonlinear functions such as the absolute magnitude operation.
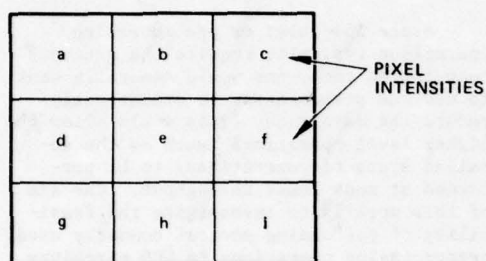
Figure 1. Schematic of the basic 3 x 3 kernel.

The Sobel algorithm operates on the full array and evaluates

$$S(e) = 1/8 \ [\,|(a + 2b + c) - (g + 2h + i)| + |(a + 2d + g) - (c + 2f + i)|\,] \qquad (1)$$

for each picture element. This output is a measure of the edge components passing through the kernel and is independent of both the polarity of the edge and, to a large extent, its orientation. The other operations are

Local averaging:

$$f_m(e) = 1/9 \ [a + b + c + d + e + f + g + h + i] \qquad (2)$$

Unsharp masking:

$$S_u(e) = (1 - \alpha)e - \alpha \, f_m(e) \qquad (3)$$

Adaptive binarization:

$$S_b(e) = \begin{cases} 1 \text{ for } f_m(e) \le e \\ \\ 0 \text{ for } f_m(e) > e \end{cases} \qquad (4)$$

Adaptive stretch:

$$S_a(e) = \begin{cases} 2 \text{ Min } \{e, r/2\} & \text{for } f_m(e) \le r/2 \\ \\ 2 \text{ Max } \{(e, r/2), 0\} & \text{for } f_m(e) > r/2, \end{cases} \qquad (5)$$

where r is the maximum pixel intensity.

All of the above operations can be obtained by combinations of three basic functions: the local means $f_m(e)$, the edges $S(e)$, and the center pixel intensity. Each of these functions can be obtained directly from the CCD analog transversal operations described below.

3. Device Descriptions

The CCD implementation of two-dimensional edge detection and local mean algorithm is an important aspect of many real-time image-processing applications. Further, since the functions discussed in Section 2 can be derived from combinations of center pixel intensities, local means, and edges, only the CCD edge detection and local mean circuits will be described in detail.

The CCD Sobel circuit consists of a 3 x 3 two-dimensional transversal filter, an absolute value operator, and a summing circuit. Figure 2 is a functional block diagram for the circuit. Three lines of analog video signal are fed into the 3 x 3 CCD Sobel transversal filter. Two differential outputs are obtained and amplified before taking their absolute values and summing. The final output $|a+2b+c - (g+2h+i)| + |a+2d+g - (c+2f+i)|$ provides edge information about the image (as is shown in Section 4). Other input and output points are also available for individual circuit tests, as indicated in Figure 2.

The CCD Sobel circuit has three parallel signal channels for the three analog video lines of the image. The inputs are of the Tompsett fill-and-spill type. The two-dimensional processing results from the appropriate inter-connection of the eight
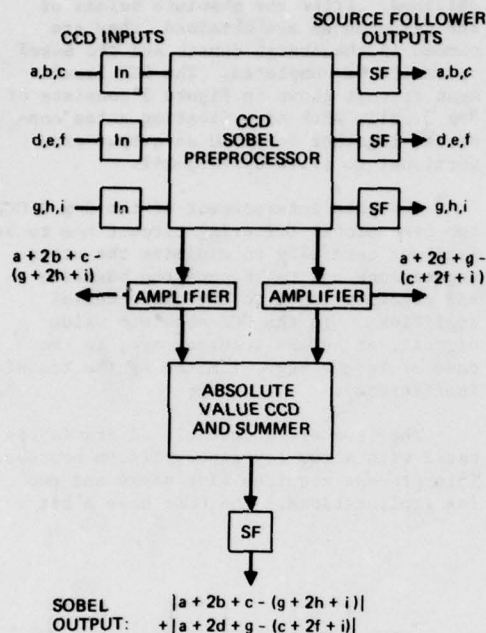
Figure 2. Block diagram for CCD Sobel operator.

floating gates of the three-channel split-electrode transversal filter. Figure 3 shows that the output in each of the four bus lines is proportional to the charges under the connected gates (a, b, c, etc.). The necessary weightings (1, 2, 1, etc.) are achieved by varing the floating gate area. The differences between the weighted sums are obtained through the output differential amplifiers. Each output, therefore, represents an orthogonal edge component. These components then act as inputs to the gates of the CCD absolute value circuit shown in Figure 4 to achieve the two-dimensional Sobel output.

The CCD absolute value circuit operates using a novel technique that allows a charge storage that is equivalent only to the input signal magnitude and is independent of signal polarity. During the input phase, ϕ_{INA} is pulsed low first (high surface electron potential in an n-channel CCD) and then settles high (low surface electron potential). When the signal voltage V_{SIG}
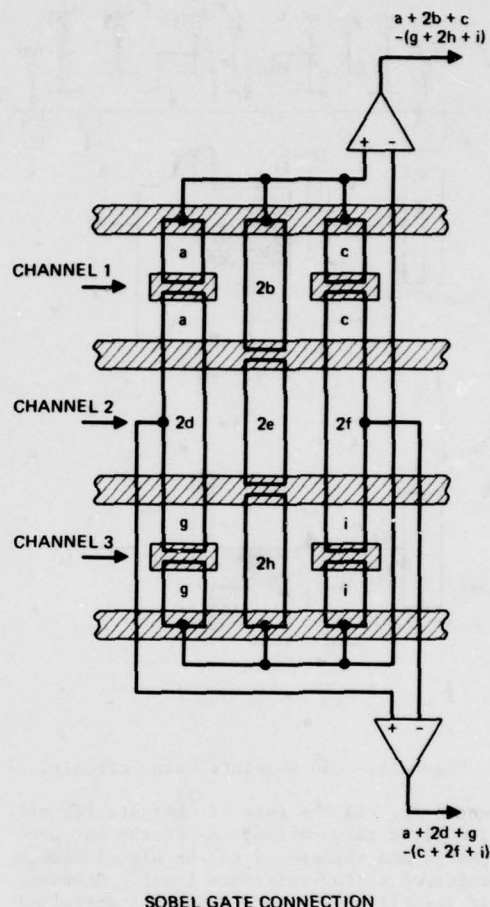
SOBEL GATE CONNECTION

Figure 3. CCD Sobel preprocessor.

is less than the reference voltage V_{REF} set by the REF gate, the electrons will fill the potential well under the gates B2 and FZ, as shown in Figure 4(a). During the output phase, ϕ_{OUTA} is pulsed high and the charge packet is transferred to the summing output. This charge is proportional to

$$\left\{ \left(V_{FZ} - V_{REF} \right) \left(A_{FZ} + A_{B2} \right) + \left(V_{REF} - V_{SIG} \right) \left(A_{FZ} + A_{B2} \right) \right\} ,$$
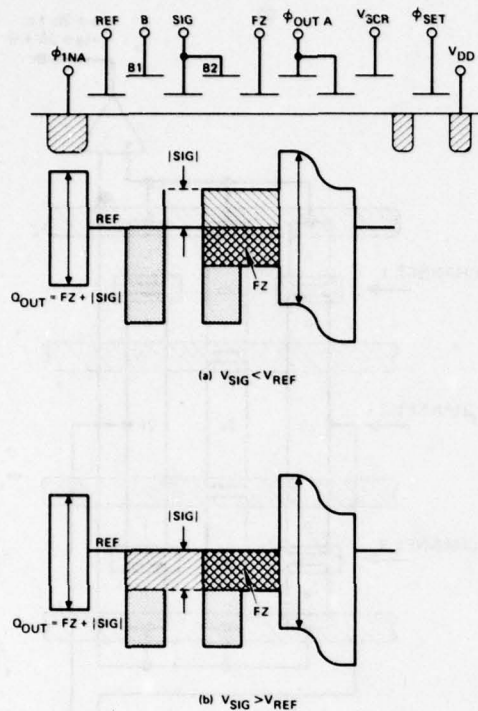
Figure 4. CCD absolute value circuit.

where A_{FZ} is the rate of the gate FZ, etc. The first term corresponds to the fat zero charge and the second to the signal charge referred to the reference level. However, if V_{SIG} is higher than V_{REF}, the potential well under B1, SIG, B2, and FZ will be filled, as shown in Figure 4(b). The output charge is proportional to

$$\left\{ \left(V_{FZ} - V_{REF} \right) \left(A_{FZ} + A_{B2} \right) \right.$$
$$\left. + \left(V_{SIG} - V_{REF} \right) \left(A_{SIG} + A_{B1} \right) \right\}$$

If the gate areas are fabricated such that $A_{SIG} + A_{N1} = A_{FZ} + A_{B2}$, then the output charge will always be a fat zero plus the charge proportional to the magnitude of the signal with V_{REF} as reference point. That is, a charge output corresponding to

the absolute value of the input signal is obtained. After the absolute values of the differences are obtained, they are summed in the charge domain and the Sobel operation is completed. The CCD local mean circuit shown in Figure 5 consists of 3 x 3 cells with nine floating gates connected together to yield an output proportional to a+b+c+d+e+f+g+h+i.

The gate interconnect of the 3 x 3 CCD two-dimensional filtering circuit has to be laid out carefully to minimize the stray capacitance and to balance the positive and negative input to the differential amplifiers. In the CCD absolute value circuit, speed and accuracy are, in the case of $V_{SIG} > V_{REF}$, limited by the transfer inefficiency.

The CCDs are N channel and are fabricated with a two-layer polysilicon process. This process requires nine masks and two ion implantations. The CCDs have a bit
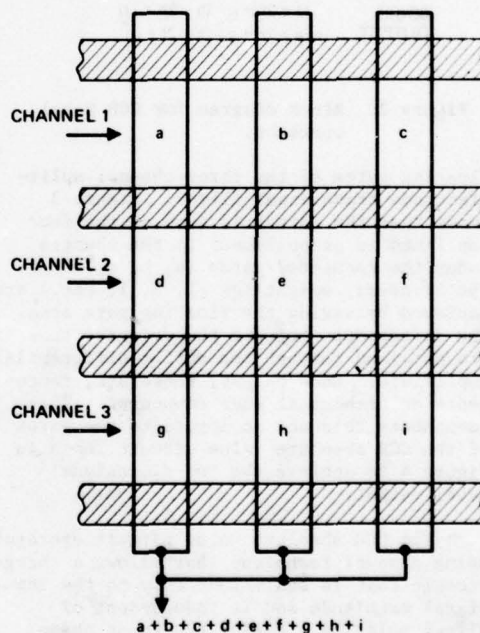
Figure 5. CCD local mean circuit.

length of 27 μm, and the minimum feature size is 2.5 μm. This results in a total area of 0.7 mm^2 for the Sobel (see Figure 6(a)), of which 0.15 mm^2 is the transversal filter. This compares with a total area of 0.6 mm^2 for the mean filter (Figure 6(b)). To achieve the necessary capacitance balance between the two difference outputs, additional metal was added, as Figure 6 shows.

(a)

(b)
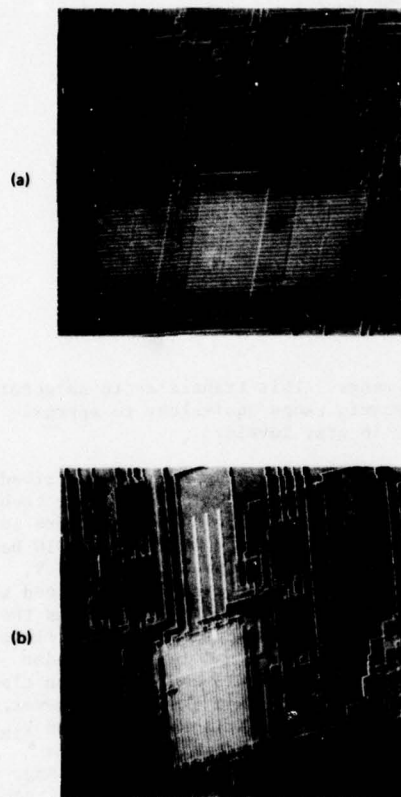
Figure 6. Photomicrographs of (a) the edge detection circuit and (b) the local mean filter.

4. Test Results

a. Measurement of Electrical Characteristics.

The two basic functions of the CCD circuits, arithmetic operations (such as absolute magnitude determination and summation) and transversal filtering, have been tested independently and the transfer characteristics measured. The weighting functions of the transversal filters for the Sobel edge detection and local mean evaluation, for example, can be written as:

$$S_x = 1/8 \begin{bmatrix} 1 & 2 & 1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix}$$

$$S_y = 1/8 \begin{bmatrix} 1 & 0 & -1 \\ 2 & 0 & -2 \\ 1 & 0 & -1 \end{bmatrix}$$

$$W_m = 1/9 \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$

where S_x and S_y provide the x and y components of the edge values, and W_m provides the mean. Both the impulse response and the linearity of these operations have been determined using the microcomputer-based test set-up shown in Figure 7.

Here the microcomputer is used to provide flexible and programmed data inputs to the CCD circuits. These data are then clocked through the devices, and the output is stored in the computer memory. This provides an accurate and rapid means of characterizing the device performance as a function of the various input parameters. The speed and accuracy of this system are basically determined by the computer cycle time and the analog-to-digital converters. The machine described here has a basic cycle time of ≈ 2 μsec and can provide an 8-bit quantization, resulting in a maximum CCD clock speed of ≈ 30 kHz.
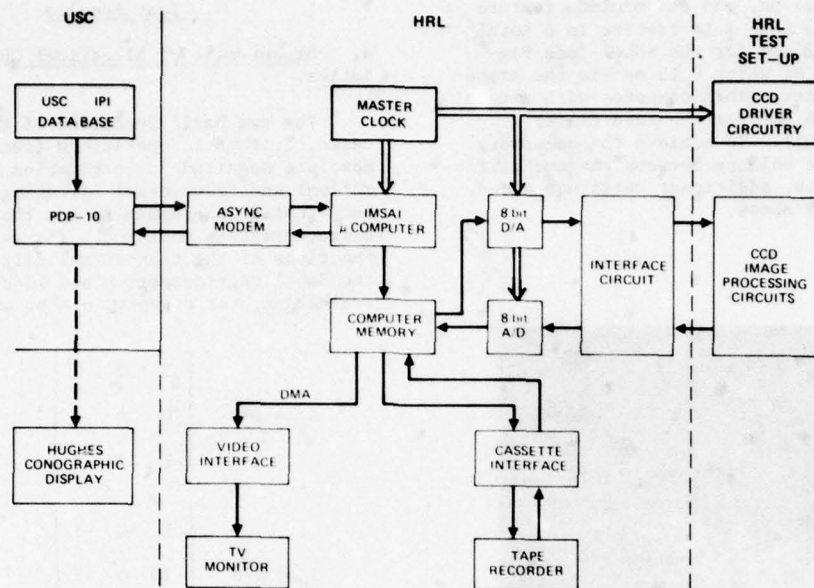
Figure 7. Microcomputer-based test facilities.

When a single input pulse with a duration of less than one-half clock cycle is used as the input, the output is equivalent to the impulse response of each component of the filters. Examples of this for the Sobel operation are shown in Figure 8.

An additional benefit of this test set-up is that a unique pattern of either analog or digital data can be generated and used as the input to the CCD circuit and the output data gated so as to uniquely determine the operation of any tap within the array. For example, if an input that linearly increases with time is clocked into the array and the output is gated so as to measure only the nth output pulse in each cycle, the weighting W_n of the nth floating electrode in the array can be uniquely determined. Measurements made in this way are shown in Figure 9, which shows the output voltage directly as a function of the input for each of the nine floating gates in the Sobel filter. The slope of each input/output characteristic gives the tap weighting for each tap. From this, inputs can be shown to be linear over approximately

a 3-V range. This translates to an accuracy and dynamic range equivalent to approximately 16 gray levels.

The absolute value circuit described in Section 3 was tested using a similar technique; the results are shown in Figure 10. Here the input voltage on the gate SIG has been swept over a range of 0 V to 10 V, and the characteristic can be explained with reference to Figure 4. Initially, as the signal voltage is increased, charge flows over the input gate and is stored under gates FZ and B1. This charge is then clocked out as the clock phase changes. However, as the input voltage is increased beyond V_{in1} (Figure 9), the bucket size decreases linearly, resulting in the linear change in voltage out (AB). When the input voltage reaches V_{REF}, the bucket size is a minimum equivalent only to the fat zero. Increasing the input further causes some of the charge previously trapped under B1 to be clocked out. Thus, the output characteristic again changes linearly from B to C. Hence, when the input signal is operated about V_{REF}, the output changes linearly in proportion to $|V_{SIG} - V_{REF}|$, the output polarity being

S_x

1, 2, 1

1, 0, −1

S_y

−1, −2, −1
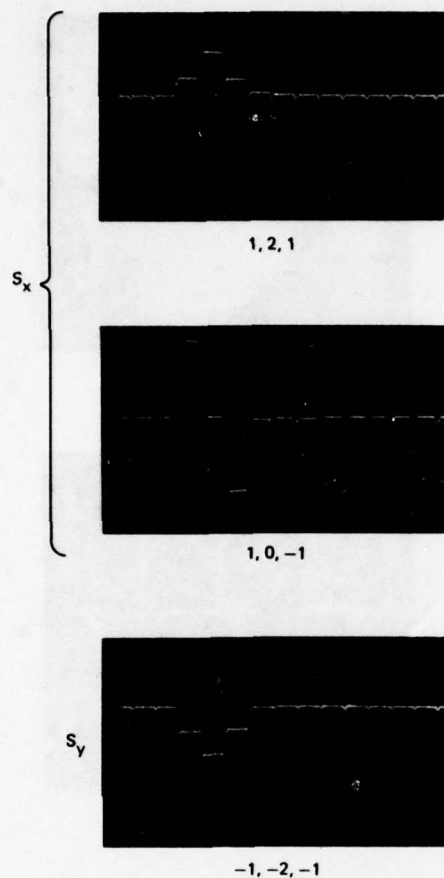
Figure 8. Measured impulse response of CCD Sobel filter.

OUTPUT VOLTAGE

2

1

0

−1

−2

1 V   INPUT VOLTAGE

Figure 9. Measurement of the weighting functions for Sobel operators.

independent of V_{SIG}. The input voltage swing, as shown in Figure 10, is approximately ± 2 V, resulting in an output change of some 400 mV. This is again equivalent to an accuracy of approximately 4 bits.

b.   Performance Evaluation of the Processor.

The processor has been tested on true two-dimensional imagery using both a stored data base and a real-time input from a commercial vidicon. The use of a stored data base allows most of the problems associated with

OUTPUT VOLTAGE

A   B   C

500 mV

V_{IN1} V_{REF}

1 V

INPUT VOLTAGE

Figure 10. Transfer characteristic of absolute value circuit.

the sensor, such as illumination, resolution, and signal-to-noise ratio, to be separated from the evaluation of processor performance. The maximum data rate of this system, however, is limited to about 30 kHz. In this mode, the imagery to be processed is first digitized and stored in the computer memory, as shown in Figure 7. (In practice, a very large data base is available on magnetic tape and has been used extensively in the performance evaluation.) The stored data are then clocked out of the random access memory in synchronism with the CCD clocks and converted to analog data before entering the processor. The processed data from the CCD are converted again to digital format and stored in the computer memory in the form of 128 x 128 four bit words. Direct memory address is then used to refresh a standard video monitor.

An example of this is shown in Figure 11 for a two-dimensional test pattern. A comparison of the output (Figure 11(b)) with the computer simulation (Figure 11(c)) shows that an accuracy of approximately four bits is preserved. An example of its operation on a real image is shown in Figure 12.

In addition to the tests on stored data, we have interfaced the processor directly with a commercial vidicon camera. The standard operating frequency of this "real-time" video is ≈ 7 MHz, providing 525 x 525 picture elements at 30 frames/sec. At present, we have operated our CCD processor at a maximum clock rate of 4 MHz, which provides the full 525 vertical resolution elements but about a three-to-one resolution loss in the horizontal direction. An example of the performance in both the local-averaging and the edge-detection modes is shown in Figure 13. Two other functions, unsharp masking and binarization (both of which are performed in real-time by our CCD processor), are also shown.

5. Conclusions

The concepts and design details of a CCD image processor that performs two-dimensional linear and nonlinear operations are discussed. Our results indicate that it is feasibile to use a CCD integrated circuit approach for the image preprocessor. The operations described are used as the basis for higher-level syntactic type of image processing, which is becoming

(a)

ORIGINAL

(b)

CHIP TEST

(c)

COMPUTER TEST
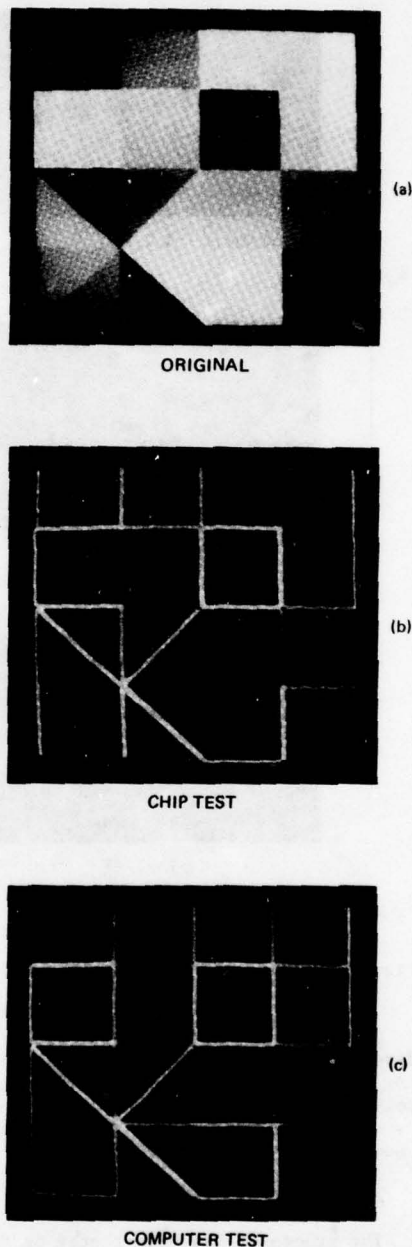
Figure 11. Example of processor operation on stored test data (at 30 kHz).
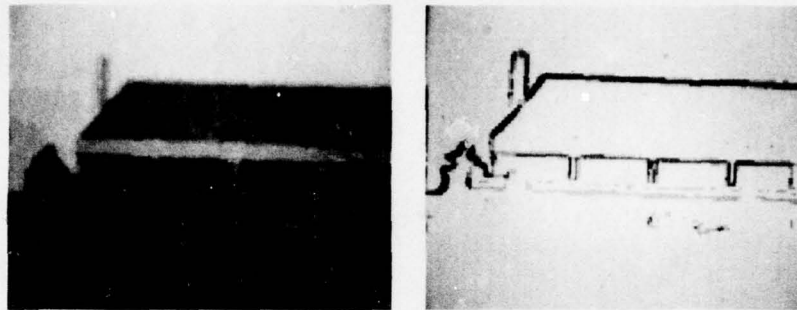
Figure 12.   Example of processor performance operating on stored imagery.

ORIGINAL IMAGE   LOCAL AVERAGING   EDGE DETECTION

UNSHARP MASKING   BINARIZATION
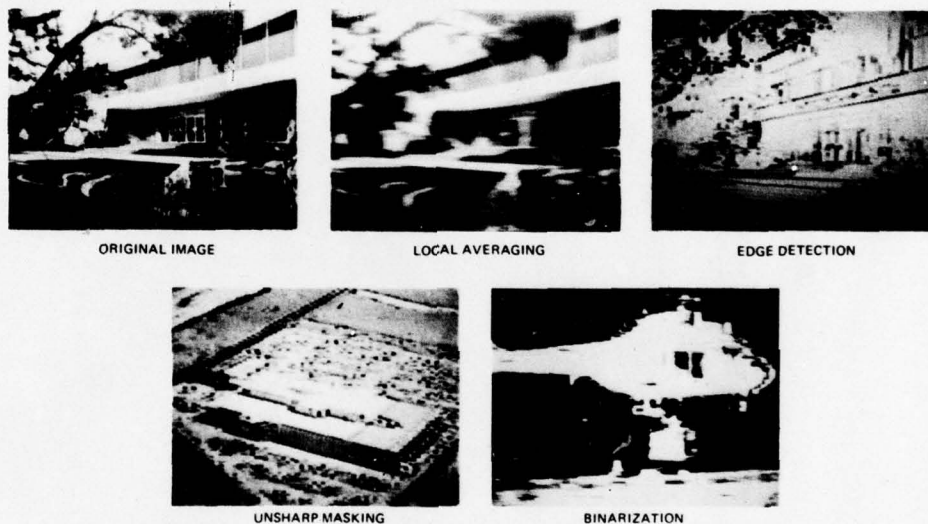
Figure 13.   Performance of processor at real-time data rates.

increasingly important in military systems for target acquisition and tracking. Typically, however, most of the processing time is taken up in the "preprocessing" type operations, and our present indications are that the CCD techniques are able to operate with at least 4-bit accuracy at speeds 100 to 300 times faster than the conventional general-purpose processor used to date.

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Acknowledgement

The Development and Application of a Digital Charge Coupled Logic (DCCL) Arithmetic Unit

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Systems Group   Systems Group

ABSTRACT

An arithmetic unit chip is described which combines the inherent low power dissipation of CCD's with the accuracy of 16-bit digital arithmetic. A technique for electrically changing a 32-bit adder to a 32-bit subtractor or an exclusive-OR function is also described.

The arithmetic unit operates as a pipeline system requiring 40 clock cycles to process data; a programming technique for overcoming this limitation is discussed. The paper also includes a description of how the arithmetic unit can be organized to implement an analysis filter for linear prediction encoding of voice.

DCCL ARITHMETIC UNIT

Previous papers [1]-[3] have described in detail how logic and arithmetic functions such as AND, OR, exclusive-OR, complement, half-adders and full-adders are designed in Digital Charge Coupled Logic (DCCL). In this paper we describe how these functions are interconnected with continuous CCD transfer channels to form a DCCL/LSI pipeline arithmetic unit.

In pipeline DCCL arithmetic, where it is required to begin processing a new word each successive clock cycle, the 2's complement number system is ideal for addition or subtraction. However, in order to perform multiplication, it is best to convert the 2's complement notation to signed binary numbers. To illustrate, a 16 x 16 multiplier-adder will be briefly described.

The two 16-bit input words to the array enter the multiplier in parallel and are formed into their partial products by 256 AND gates (as shown in Figure 1). The partial products are added by an array of full-adders and since the carry from the least significant product column propagates through 31 other columns gaining a clock phase delay in each column, the product is skewed a total of 32 clock phases from the least significant to the most significant product.
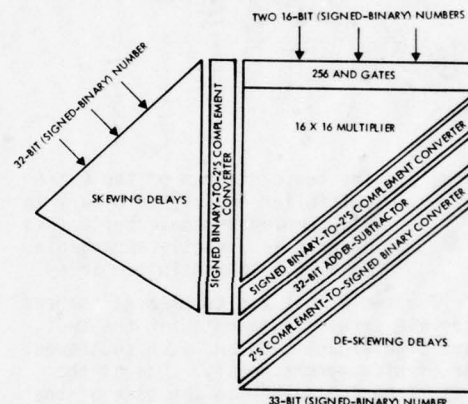
Figure 1. Block Diagram of the DCCL Arithmetic Unit

The 32-bit product from the multiplier and the 32-bit data word are both converted to 2's complement notation before transferring to the adder/subtractor. In converting negative numbers from signed binary to 2's complement, it is necessary to complement and increment by adding a binary-one to the least significant bit. In a DCCL pipeline system, the incrementing is carried out by parallel interconnected half-adders, with each word-bit being incremented on successive clock cycles as shown on the logic diagram of a 6 x 4 multiplier of Figure 2. The blocks marked CD in Figure 2 are charge

duplicating cells that generate two separate charge packages that are of the same binary value and size as their input packet. The skewed product from a multiplier matches the skewed input to the number converter, however, the 32-bit input data arrives synchronously, and results in having to skew the input data word with CCD delay lines.
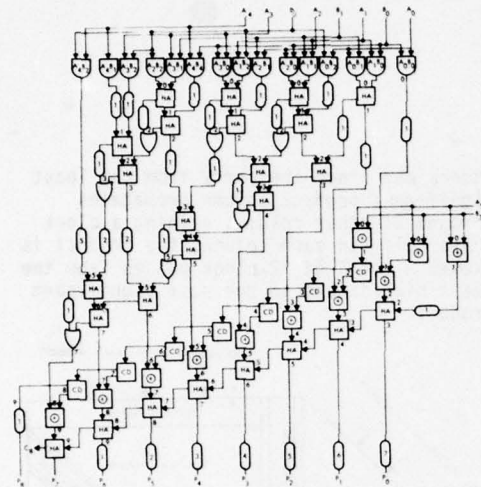
Figure 2. The logic diagram of the 6 X 6 multiplier and signed binary to 2's complement converter. This diagram is directly expandable to a 16 x 16 multiplier array.

The two 32-bit 2's complement numbers enter the array skewed but with the two least significant bits and each subsequent pair of bits synchronously. One of the words; (the subtrahend in the case of the subtract mode) is transferred into one of the input ports of each of the 32 exclusive-OR gates. A control line, K, determines the binary value of the input to the other input port of the exclusive-OR gates as shown in Figure 3.
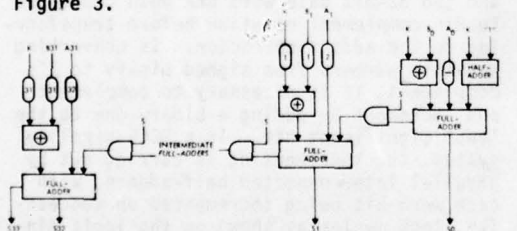
Figure 3. Logic Diagram of DCCL 32-Bit Adder/Subtractor/Exclusive-OR Array

When control line K is switched so that a binary zero is entered into the exclusive-OR gates, the data is transferred through the exclusive-OR without being changed. However, when the control line K is switched so that a binary one is entered into the exclusive-OR gates, the data is complemented. The control line K, is also transferred into one input terminal of a half-adder and a binary one input packet is transferred into the other half-adder input during each clock period. The half-adder will generate a binary-one charge packet from its carry-out port each clock period when $K = 1$ and a binary-zero charge packet from the carry-out port when $K = 0$.

The carry-out port of the half-adder is connected to the carry-in port of the least-significant-bit full-adder in the array. Thus when $K = 1$, the input data (the subtrahend) is complemented and the difference is incremented by one.

The output from the 32 exclusive-OR gates and the other 32-bit input data are transferred into two of the three inputs of each of the 32 full-adders as shown in Figure 3. The carry-out port of each full-adder is connected to the carry-in port of the next more significant full-adder. Each pair of bits are added (or subtracted) in turn, at each subsequent clock phase. Therefore the most significant pair are acted upon, 32 clock phases after the least significant pair.

In order to be able to switch the function of the array from add/subtract to exclusive-OR, two input AND gates are inserted between the carry-out and carry-in ports of each full-adder. A control line S controls the value of the value of the binary input to the other input port of the AND gates. When S is at the binary zero value, the carry channel is inhibited, and the array output is the exclusive-OR. When S is at the binary-one value, the carry-bits are enabled and the array output is the add/subtract. There are no clock phase delays through a DCCL AND gate, so this extra functional capability does not require more skewing.

The skewed 2's complement output of the adder array is then changed back to the signed binary to 2's complement converter described above.

The output from the number converter is still in a skewed format and required an array of shift registers in order to synchronize the output data.

APPLICATIONS

In order to match the performance of the CCD chip presented in this paper, at an operating speed of 5MHz, a general purpose computer requires a 200ns instruction cycle time. Within this 200ns, a 16 x 16 multiply, followed by a 32-bit add must be performed. To prevent the necessity of a faster operating speed, the computer must be fully pipelined, instruction access and data access must occur simultaneously with arithmetic processing. The existing ALU technology for implementation of a multiplier/adder at this data rate requires a power dissipation in excess of 20W, whereas the equivalent throughput is obtained by the CCD processor presented in this paper at a power dissipation of approximately 1W. Consequently, spacecraft and other low power, high density applications lend themselves to the use of this chip.

Although the shift register nature of CCD's does not allow efficient programming of arbitrary algorithms, as would occur in a general purpose computer, certain processes with wide applications are readily implementable in CCD. Furthermore, programming and scheduling techniques allow efficient implementation of general purpose algorithms. Some of these algorithms and techniques are discussed in the following paragraphs.

The pipeline nature of the CCD ALU chip allows efficient computational through-put for those tasks allowing many multiplies or adds in parallel, where one arithmetic operation is not a function of succeeding operations. Examples of such functions are:

Correlation
Discrete Fourier Transform
Delay Line

Incorporating into the CCD chip the additional facility of latching the 32-bit output from the adder and adding this latched value, rather than the other 32-bit input value, to the output of the multiplier facilitates correlation. Here,

$$\emptyset_j = \sum_{i = j + 1}^{k} X_i X_{i - j} \qquad (1)$$

is calculated by loading $X_{j + 1}$ and X_1 into the multiply portion of the chip, followed by $X_{j + 2}$ and X_2, etc. The complete correlation is accomplished in $(k - j)$ clocks in addition to the chip delay.

A network of 61 correlators depicted in Figure 4 is required for pitch extraction in the process of linear prediction for voice data bandwidth reduction. This correlation network consists of 61 independent calculations of a 16 x 16 multiply preceeding 61 calculations of a 32-bit add to partial accumulation. Even without the additional facility mentioned above, the three operands (two 16-bit multiplicands and the 32-bit partial accumulation for each of the 61 correlations) are loaded into the chip at each clock and the updates occur at the maximum chip through-put rate.
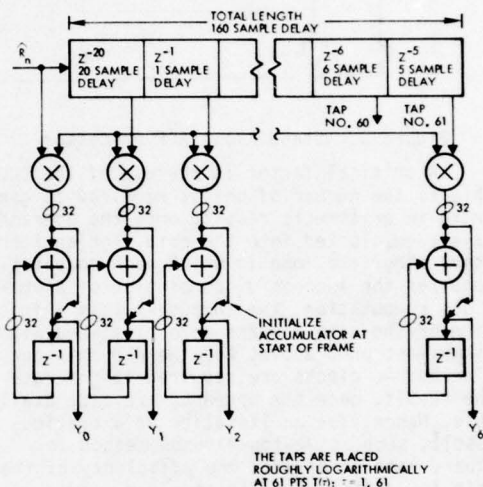
Figure 4.   ACF Network

A study on the CCD implementation of the auto-correlation function resulted in the conception of a stand alone processor, depicted in Figure 5. The dashed line of Figure 5 contains that portion of the processor implementable by the CCD ALU considered in this paper. The circulating shift register/MUX complex, which is CCD realizable, allows computation of correlations of arbitrary lags in a straight forward manner via equation (1). This stand alone processor eliminates the need for address generation, as would occur when computing many partial correlation updates as each data sample arrives. It also reduced the processing memory bandwidth, since the shift registers maintain all the needed sampled data. Furthermore, this processor can be implemented in parallel with a general purpose computer. This method is consistent with the correlation techniques on the existing TRW voice processors.
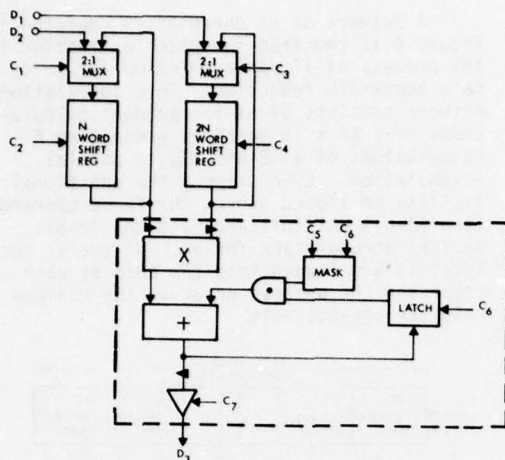
Figure 5.   Stand Alone ACF Processor

A critical factor in the use of the CCD chip is the number of shifts required to generate an arithmetic result, once the operands have been clocked into the chip. For an iterative algorithm, one in which each computation requires the successful completion of a previous computation, the through-put is a fraction of the case for the more pipelined algorithms mentioned above. For the ALU chip considered, 40 clocks are required to generate the result, once the operands are made available. Hence, for an iteration on a previous result, such as Newton-Raphson method for square root or divide, the efficiency of the chip is 1/40th the efficiency for, say, correlation.

The pipeline restruction can be overcome however, if the computational requirements is for a number of processes to occur in parallel. A practical example is the implementation of the analysis filter for linear prediction encoding of voice. The computational requirements for this application are depicted in Figure 6. Ten complete analyzer filters must be implemented between voice samples, where the residue from one filter constitutes the input to the next filter in line. Since only 15 to 16 complete iterations through the CCD ALU are feasible between voice samples, the calculation of the complete 10-stage analyzer filter is impossible in a straight forward manner.

However, the computation can be accomplished in the following manner:

Analyzer Stage 1 is performed on voice sample S_i

Analyzer Stage 2 is performed on voice sample S_{i-1}

Analyzer Stage 10 is performed on voice sample S_{i-9}

with the complete 10 stage filter being accomplished on voice sample S_{i-9}.
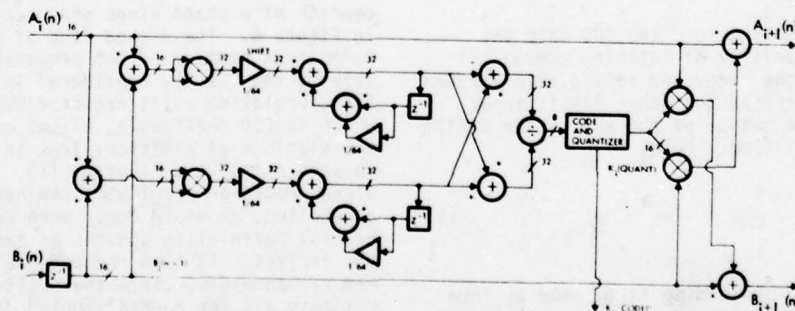
Figure 6.   Applicable Voice Algorithms

ADDRESSING CONSIDERATIONS

Incorporation of this CCD ALU chip into a general purpose CPU requires some addressing considerations. The output of the CCD ALU may be required for re-insertion into the chip or the output may be placed into data memory. Since operands are loaded 40 instructions prior to the occurence of the arithmetic result, the intended store address may not be known at the time that the result is available. Although the intended use of the data may be known at the time the operands are placed into the chip, it is only in the case of highly deterministic programs that instructions are known 40 stages in advance. Here, the addressing problem is alleviated with the incorporation of an address shift register of length 40. The storage address is calculated simultaneous with the retrieval of operands and this store address is placed into this shift register. The store address is available from the shift register at the same time that the arithmetic result became available from the CCD ALU.

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DESIGN, OPERATION AND APPLICATION OF A HIGH-SPEED CHARGE COUPLED
PROGRAMMABLE TRANSVERSAL FILTER

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ABSTRACT: A monolithic 511-tap CCD programmable transversal filter (PTF) designed to function as a pseudo-noise matched filter is described. It is designed to operate at a sampling rate of 8 MHz; it is organized for staggered dual-channel operation. Experimental results on a 127-tap prototype are reported, including a 56 dB output dynamic range at 8 MHz and a 60 dB dynamic range at 4 MHz. Linearity over this range was good to ± 1%. The application of the PTF type of device in spread spectrum communication systems is discussed. Particular examples are JTIDS (Joint Tactical Information Distribution System) and the GPS (Global Positioning Satellite) system.

I. INTRODUCTION

Charge coupled device technology, due to the simplicity with which it provides delayed, sampled, analog signals and can perform a large number of multiplications of these signals with weighting coefficients, has been widely used in various kinds of transversal filter designs. Numerous split-electrode transversal filter designs have been reported; these utilize a near-continuum of weighting coefficients, (Ref. 1). When the tap weight coefficients take on binary values of + 1 of - 1, the device is a binary-analog matched filter, generally used to convolve an analog signal with a binary pseudo-noise (PN) code, (Ref. 2). When the binary code is electrically alterable, the filter is called a programmable transversal filter (PTF) which is used as a PN matched filter (PNMF). This type of filter finds application in spread spectrum receivers used for anti-jam, multiple access, and precision navigation systems.

This paper describes a high-speed CCD PTF which is organized for staggered dual-channel operation. A functional block diagram of the device is shown in Figure 1. After first loading binary codes into the two MOS shift registers the analog input signal is sampled and then transported through the tapped CCD delay line; simultaneously the odd and the even sample

correlations take place. The staggered tap architecture offers both the layout advantage that the pitch of the MOS shifter register can be twice that of the CCD delay line, and several operational advantages. These include (1) allowing the PTF to respond to incoming analog waveforms which are encoded by a pair of interlaced orthogonal PN codes, and (2) multiplexing a single PN code into the two reference registers so that the maximum code loading rate is twice that of a single MOS register.

Section II describes the design and the operation of the PTF device. Some experimental data are presented in Section III. Based on the results of a prototype PTF device (PTF-1), the linearity characterisitcs of a tapped buried channel CCD are examined. In Section IV, some applications of the PTF to coded commuications are presented.

II. DESIGN AND OPERATION

General

A block diagram of the monolithic PTF circuit is shown in Figure 2. The circuit consists of a tapped CCD delay line, two static MOS registers, two binary latches, two tap-summing networks, two pairs of buses, four signal output circuits, and other support circuitry. FET switches in the summing network connect

each tap to one or the other of two buses. Thus, tap weights of + 1 and - 1 are realized. The latches which control these switches temporarily store a first set of logic states from the MOS register so that the PTF can function while a second set is being loaded. The MOS register is split into an odd-tap register and an even-tap register. The associated bus pairs have independent outputs. In addition to the correlation outputs, there are correlation magnitude outputs for the two channels. The magnitude signals are used for initial signal acquisition and for synchronization. Other support circuitry includes the clock generators and drivers for the MOS shift registers and the CCD structure.

CCD and MOS

The CCD delay line consists of a surface channel injection port, buried channel tapped stages and a gated-charge-integrator output amplifier. A cross-section view of the CCD delay line is shown in Figure 3. The register design is of the two-phase implanted barrier type and is operated 1-1/2 phase. Two barrier gates and two well gates form one cell. In each cell, one barrier gate and one well gate are tied together to form the clocked phase ($\emptyset_T$). The other barrier gate is tied to a dc source and the other well gate is the tap. The potential of the tap is controlled by the summing network and bus circuits. The length of each cell is 32μm making the total length of the 512 stage delay line equal to 16.38mm. The CCD delay line is designed to run at 8 MHz.

For the MOS shift registers, a 3-phase seven transistor quasi-static MOS shift register cell configuration is employed, (Ref. 3). Two clocks are needed for loading the code, while the third clock is used to provide the latch function.

Bus Output Charge Sensing

A functional schematic of bus sensing circuit is shown in Figure 4. In operation, the dc level of the buses is maintained by a pair of reset switches, which are closed during a portion of each transport clock ($\emptyset_T$) high period. After the reset switches are opened, the buses are floating. Thus, when the transport clock goes low, i.e., at the moment when the charge packets are moved under the sense electrodes, signal voltage develops between the buses. This differential voltage is proportional to the correlation coefficient

of the PN code and the signal amplitude in the CCD register at the time. In the correlation output circuit, the bus voltages are first sampled by two sample and hold switches and then sensed by a differential voltage amplifier. The differential amplifier is followed by a 3-stage source-follower output buffer.

For the correlation magnitude circuit the bus pair is connected to a one-stage CCD register with two inputs which are complementary. One CCD input or the other always contains charge proportional to the magnitude of the bus voltage difference. The two CCD inputs are combined after one clock of delay. This circuit provides high common mode rejection of transients on the buses.

Clock Timing and Waveforms

Master clocks f_1 and f_2 are supplied to the PTF for the MOS shift register and the CCD, as shown in Figure 2. All clock and driver signals are produced by clock generators on the monolithic PTF circuit. There are five MOS shift register clocks controlled by f_1 and four CCD clocks controlled by f_2. Four MOS shift register clocks load the two registers in interlaced mode, and the fifth holds the codes in place. The four CCD clocks are the transport clock ($\emptyset_T$), the sampling clock ($\emptyset_S$), the reset clock ($\emptyset_R$) and the sample-and-hold clock ($\emptyset_{SH}$). The relative timing is shown in Figure 5. $\emptyset_S$ drives the input diode, injecting charge when it is low. The $\emptyset_T$ and $\emptyset_R$ functions have been described above.

$\emptyset_{SH}$, the inverse of $\emptyset_S$, samples the bus signals during its high period and holds them for the low period. Three bus signal waveforms exhibiting the positive correlation, no correlation and negative correlation cases are also displayed in Figure 5. With the aid of the $\emptyset_{SH}$ clock, output signals are valid for a full clock cycle. However, the magnitude correlation is delayed one clock period because of the one-stage CCD employed in each detection circuit.

III. EXPERIMENTAL RESULTS

Laboratory measurements were made with a prototype PTF (PTF-1), a 128-cell, 127-tap CCD PN matched filter without peripheral circuitry. A circuit schematic of the PTF-1 is shown in Figure 6.

Linearity Characteristics of the Tapped, Buried-Channel CCD

One source of nonlinearity is known to be the variable distances between a charge packet, its overlying tap, and its underlying neutral substrate as the size of the charge packet varies. These variations effect the fraction of the charge in the packet that is mirrored on the tap. In this circuit the nonlinearity of concern is between the signal voltage input and the induced signal charge on the taps. In the initial characterization of this device we also measured the nonlinearity relative to the peak displacement current in the buses associated with the induced signal charge.

The schematic for current sensing is shown in Figure 7. The bus output, V_{OB}, as well as the CCD current, plotted against input voltage, is shown in Figure 8. Here the input signal is a square wave representing the code 11110000... The amplitude of the signal is V_{in}; the signal is applied to the IG gate of the CCD. Since a surface channel structure is used for the CCD input, a relatively linear characteristic is observed for current versus V_{in}. However, a pronounced nonlinearity is exhibited in the lower portion of the V_{OB} versus V_{in} plot. This nonlinearity is attributed to the relationship between bus voltage and signal charge.

The plot in Figure 8 also suggests that when a proper offset voltage is applied between the IR and IG gates the nonlinearity can be minimized. In Figure 9, V_{OB} is plotted as function of V_{in} for the bias conditions $V_{IR} - V_{IG}$ = 1.3 V, 1.5 V, and 1.7 V. Comparing Figure 8 and Figure 9, it is noted that a significant improvement in linearity is achieved in the latter. In order to obtain more accurate linearity data, differential linearity characteristics were also investigated. A typical linearity plot is shown in Figure 10. It is seen that better than 1% linearity has been realized in this buried channel structure over a major portion of the CCD charge range, i.e., over a 1.1 V input range. It is within this range that the following dynamic range characterization was made.

Multiple Access and Dynamic Range

Figure 11a. shows simultaneous autocorrelations of two overlapping PN signals differing in power by 24 dB. The two codes are both 127-chip maximal codes; the PTF-1 was operated at 4 MHz. One autocorrelation is at a 60 dB measured S/N; the other is at 36 dB. The peak-to-peak input signal in this test was approximately 1 volt. Figure 11b. shows the same two signals with an expanded scale to illustrate autocorrelation of the weaker signal in the proximity of the stronger signal. Figure 11c. shows the same two signals with the vertical scale expanded even further to show the CCD noise level against which the signal autocorrelations are measured. CCD clock noise has been suppressed by a correlated-double-sampling charge sense circuit.

IV. APPLICATION OF THE CCD PN MATCHED FILTER

The CCD PNMF is particularly suited to certain classes of coded communications sometimes referred to as "spread spectrum". These communications systems are used for their desirable properties of

- . Resistance to enemy jamming
- . Multiple access with randomized combinations of time and code division
- . High resolution navigation

Two important examples of these are: JTIDS (Joint Tactical Information Distribution System) and the GPS (Global Positioning Satellite) system. JTIDS is an airborn network allowing simultaneous communication using multiple data pulses, each coded by a 32-element binary pseudo noise (PN) code. Binary elements of code are called "chips", with "bits" reserved for binary data. The GPS uses very long PN code sequences correlated for a large time-bandwidth product so as to give large processing gains needed for worldwide navigation using the weak satellite-transmitted signals.

These systems can be characterized by the use of "non-repeating" PN codes which the receiver must synchronize to within some range-time ambiguity. The use of PN matched filters helps

to assure rapid synchronization. Also, by being tolerant of some timing ambiguity, PN matched filters lead to receiver simplification. Because it is a monolithic device, the CCD PNMF is well suited both for filters of long code length and for arrays of filters.

An example of spread spectrum modulation is shown in Figure 12 for MSK (Minimum Shift Key) modulation used in many systems, JTIDS being a current example. Binary data and a higher speed binary PN code are multiplied and phase-modulated onto an IF sinosoidal signal, converted to RF and radiated.

A typical receiver is shown in Figure 13. The receiver signal, downconverted to IF, is spectrally filtered by a "chip matched filter" and synchronously demodulated to baseband as in-phase (I) and quadrature (Q) components.

A pair of identical CCD PNMF's, programmed with the PN code correlates the I and Q signals. The autocorrelation R(t) is produced by the two filters as I and Q components,

$$R(t) \cos \emptyset \text{ and } R(t) \sin \emptyset$$

where $\emptyset$ is a random phase angle. Squaring, or taking the magnitude, and summing recovers $|R(t)|$, the autocorrelation magnitude. This noncoherent demodulation is used for synchronization and where data is modulated as a pulse position. Using the PTF-2 in this application, one of the monolithic circuits would be required for each of the I and Q channels.

Other PNMF Circuits

Figure 14 shows a CCD PNMF for correlation of a 32-chip PN code modulated in MSK, which is a version of CPSM (Continuous Phase Shift Modulation). The PN chip modulation in MSK is in two groups offset by T sec with each chip 2/T wide. The CCD shown is designed for the minimum 1/T sampling rate, containing 32 CCD delays and 32 taps. Figure 15 shows a CCD PNMF with 64 CCD delays, 32 taps and 2/T sampling for double the sampling resolution.

Figure 16 shows how the sampling loss is reduced by increasing the CCD sampling rate from 1/T (5 MHz in this JTIDS case) to 10 MHz, or more.

It is often necessary to noncoherently sum several PNMF autocorrelations by first squaring and then summing through appropriate delays. When this is done there is a loss in signal due to charge transfer inefficiency in the PNMF's which depends on the number of autocorrelation pulses being summed. The loss also depends on the SNR of the individual PNMF autocorrelations. This latter relationship is shown in Figure 17. Here a 1024-chip PN code correlation is analyzed for the case of 32 subcorrelations (32 groups of 32 chips each).

The arraying of several CCD PNMF's for increased sampling resolution is shown in Figure 18. For a 5 MHz chip rate PN code, 10 MHz sampling (2/T) gives 100 ns resolution. Two CCD's with 10 MHz sampling, offset 50 ns (T/4), can achieve 50 ns resolution. 25 ns resolution can be obtained by analog interpolation or using four CCD PNMF's each clocked at 10 MHz, but staggered in 25 ns delays (T/8).

CONCLUSION

A monolithic 511-tap CCD PNMF circuit has been designed which includes peripheral circuits. It is designed to operate at a sampling rate of 8 MHz. Excellent performance was reported on a 127-tap prototype, including a 60 dB output dynamic range at a 4 MHz sampling rate. A discussion of spread spectrum applications of this type of circuit has shown how filtering actually is done.

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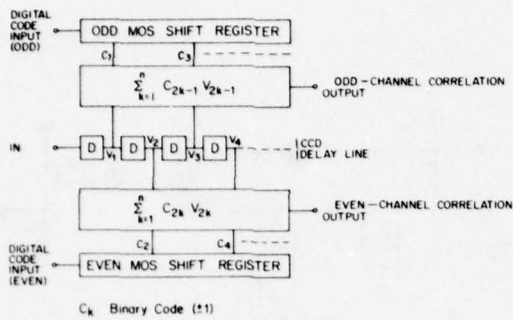
FIGURE 1   FUNCTIONAL BLOCK DIAGRAM
OF THE PROGRAMMABLE
TRANSVERSAL FILTER
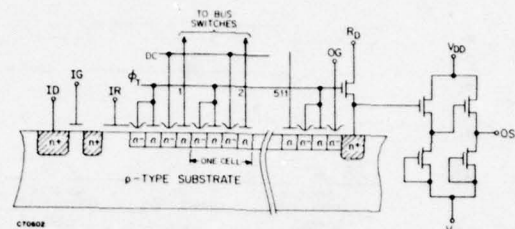
FIGURE 3   CROSS-SECTION VIEW OF
THE CCD DELAY LINE
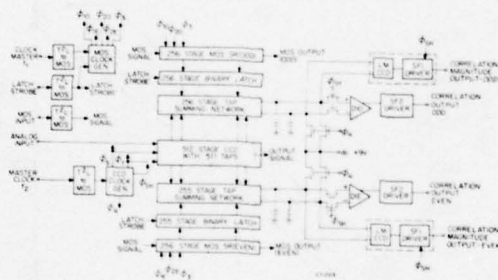
FIGURE 2   COMPLETE BLOCK DIAGRAM
OF THE PROGRAMMABLE
TRANSVERSAL FILTER
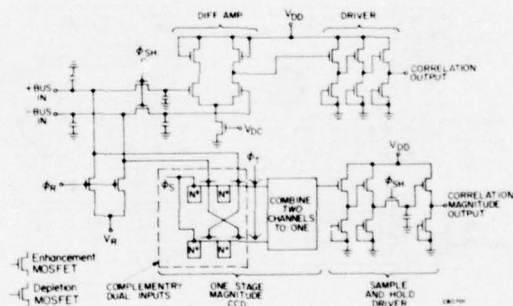
FIGURE 4 PTF BUS OUTPUT SENSING
CIRCUIT SCHEMATIC
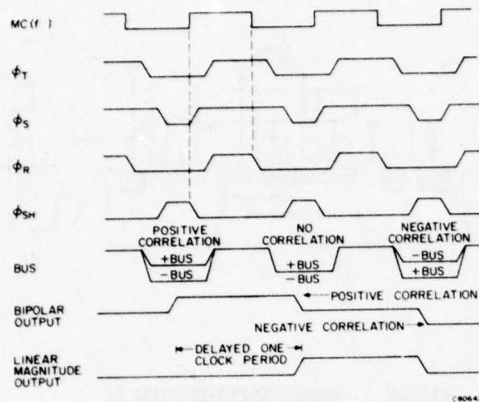
FIGURE 5 PTF CLOCK AND SIGNAL
WAVEFORMS

FIGURE 7 OFF-CHIP BUS OUTPUT CURRENT
SENSING FOR THE PTF-1

FIGURE 6 CIRCUIT SCHEMATIC OF THE
PROTOTYPE PROGRAMMABLE
TRANSVERSAL FILTER
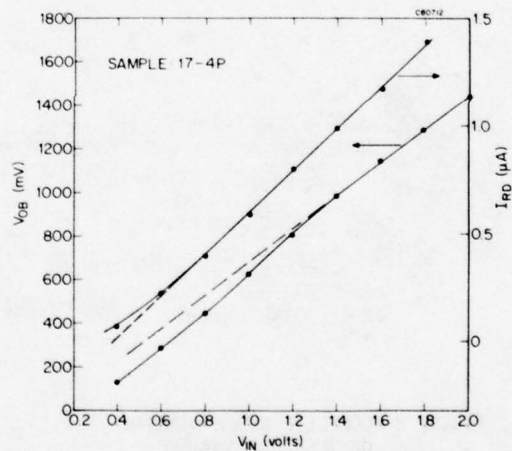
FIGURE 8 BUS OUTPUT, V_{OB}, AND CCD
CURRENT, I_{RD}, VS. INPUT
VOLTAGE, V_{in}. (THE DEVICE
SATURATES AT V_{in} = 2.2 V)
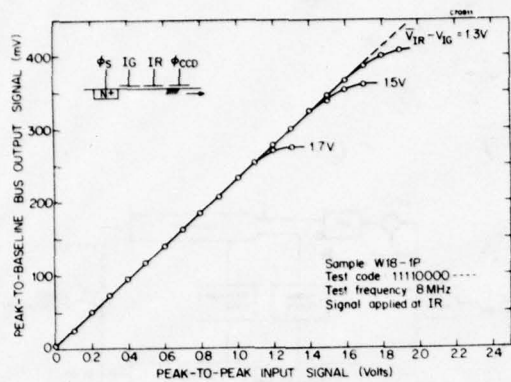
FIGURE 9 LINEARITY OF THE PTF-1
AT THREE DIFFERENT
BIAS CONDITIONS

(A) SIMULTANEOUS AUTOCORRELATION OF TWO OVERLAPPING PN ENCODED SIGNALS
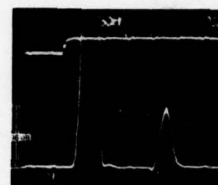
(B) VERTICAL SCALE EXPANDED TO SHOW RESOLUTION OF WEAKER INPUT SIGNAL
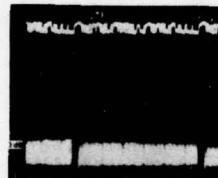
(C) VERTICAL SCALE EXPANDED AGAIN TO SHOW CCD INTERNAL NOISE LEVEL

FIGURE 10 DIFFERENTIAL GAIN VS.
APPLIED OFFSET VOLTAGE

FIGURE 11 CCD PN MATCHED FILTER
AUTOCORRELATION
PERFORMANCE OF THE
PTF-1 AT 4 MHz

A. BLOCK DIAGRAM

B. SIGNAL
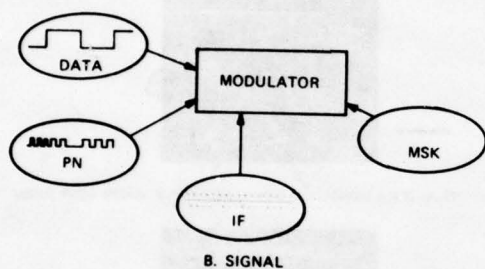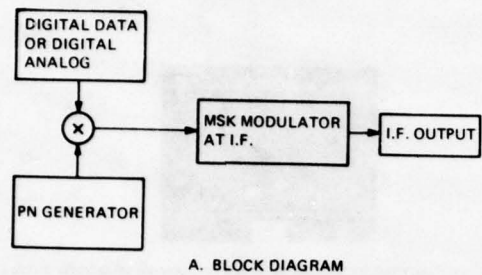
FIGURE 12 MSK MODULATION
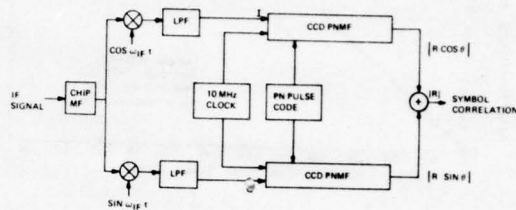
FIGURE 13 SYMBOL DEMODULATION
(10 MHz RESOLUTION)
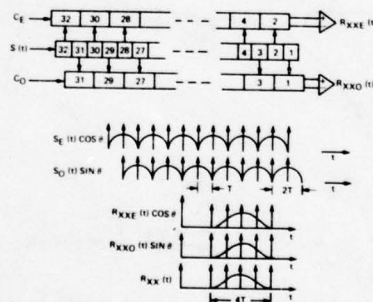
FIGURE 14 CCD PNMF FOR CPSM
(1/T SAMPLING)
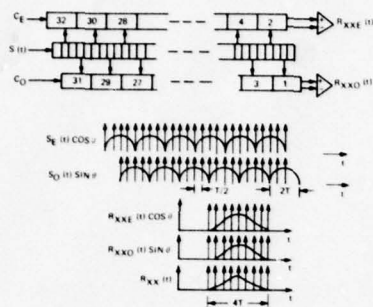
FIGURE 15 CCD PNMF FOR CPSM
(2/T SAMPLING)
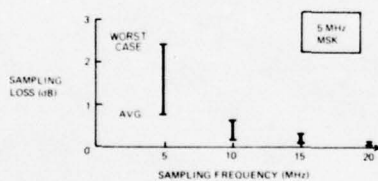
FIGURE 16 CCD PERFORMANCE
LIMITATIONS
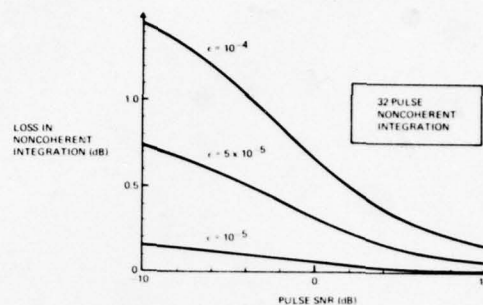
FIGURE 17 CCD CHARGE TRANSFER
INEFFICIENCY (ϵ)

(a) INTERPOLATIVE 25 NSEC RESOLUTION
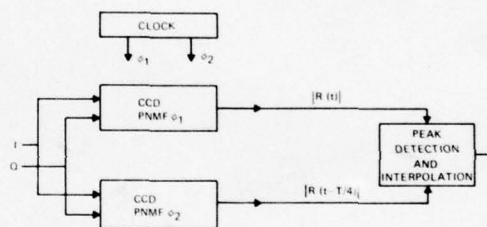
(b) DIRECT 25 NSEC RESOLUTION
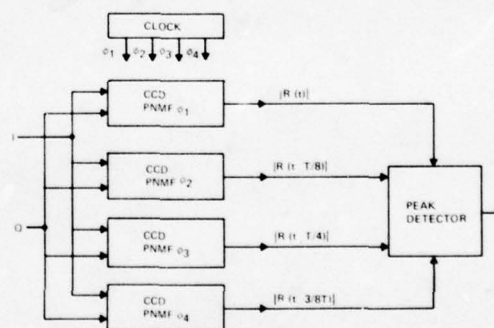
FIGURE 18 INCREASED SAMPLING
RESOLUTION WITH
CCD PNMF'S

A PROGRAMMABLE CCD TRANSVERSAL FILTER; DESIGN AND APPLICATION

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ABSTRACT

A CCD-based programmable transversal filter is described. The filter incorporates analogue weighting coefficients and multipliers in an economic structure, suitable for high-density integration. The performance of a monolithic, 64-point prototype device is discussed, and a 256-point chip, which is currently in development, is reported. The limitations of this structure are considered with regard to several potential application areas.

I. INTRODUCTION

State-of-the-art CCD and linear MOS circuit techniques now permit the realisation of electrically programmable analogue filter elements in monolithic form (1). These low-power, light-weight devices have broad application in sonar, radar and communication equipment, where one such filter element may be programmed to perform a variety of matched-, frequency- and statistical-filtering functions. The economic advantage of a single, programmable design over dedicated-function filters is a clear incentive to development. However the possibility of a simple interface to a digital processor, able to intelligently control the filter function in real time, adds a new dimension and makes these devices uniquely attractive in many applications requiring filter adaptability. It is the purpose of this paper to describe a particular realisation of this important filter type.

One plausible filter architecture, capable of monolithic realisation, is shown in Figure 1. This structure is a direct realisation of a Transversal Filter (2) with alterable weighting coefficients. A CCD element forms a tapped-delay line *signal* register which gives a parallel output of a time sequence of signal samples. These are multiplied by a set of weighting coefficients, stored as voltages in a register of MOS capacitors, the multiplication being performed by a single MOS transistor at each filter point. All products are simultaneously summed to produce the filter output, $\{o\}$. It is easily shown that

$$o(nT) = \sum_{m=1}^{N} s(nT - mT)r_m \qquad (I.1)$$

where $\{r\}$ represents the reference (or weighting) sequence and $\{s\}$ is the sampled input (or signal) sequence. Equation (I.1) is often referred to as the convolution sum, since it represents the convolution of the signal $\{s\}$ with the reference $\{r\}$, which itself defines the impulse response of the filter.

This sequence of reference voltages may be most easily programmed from a common analogue input bus, under the control of a digital selector. Naturally information stored on the capacitors is volatile and must be refreshed periodically, implying the use of an additional non-volatile (digital) memory. Despite the requirement for two levels of memory however, this parallel structure is favourably compact because of the smallness of the analogue multiplying elements in comparison with digital components.

The CCD signal delay line may be implemented using any non-destructive tapping technique. We have used the Floating Gate Reset (FGR) (3) configuration with encouraging success. Charge packets are sensed capacitively, via an isolated (floating) CCD electrode, followed by a high input-impedance MOST buffer amplifier. FGR tapping may be combined with a feedback linearisation scheme at the input (3), employing a dummy tap and a single operational amplifier to linearise the overall transfer function, and automatically achieve unity gain.

The advantages of this simple filter structure are that it is extremely compact (allowing many filter points to be integrated on a single chip), and that identical stages (and devices) may be directly cascaded through the CCD signal register to form much larger filters.

II. MULTIPLICATION

The performance of previous filter realisations has suffered largely because of poor stability and accuracy in the multiplication elements. We describe here 4- and 2- quadrant multiplication techniques based upon a single MOS transistor which are both more stable and more accurate than previously reported matched transistor circuits (4,5).

We begin with an MOS transistor operating in the triode region with a virtually grounded source, at a potential V_{r_o}, as shown in Figure 2. Now apply one multiplicand voltage V_r to the drain, with respect to the source, and apply also a voltage V_{s_o} (equivalent to a signal zero) to the gate. Then, from simple MOS theory,

$$I_{D_o} = \beta_m([V_{s_o} - V_T] V_r - \frac{V_r^2}{2}) \quad (II.1)$$

where β_m is a process dependant gain constant and V_T is the transistor threshold voltage. If we now *change* the gate voltage by the second multiplicand, V_s, the *change* in drain current, ΔI_D, is simply :

$$\Delta I_D = \beta_m V_r V_s \quad (II.2)$$

It is easy to show that this product is valid for all sign combinations, thus realising 4-quadrant multiplication.

An output circuit is shown in Figure 3 which may be used to sum the currents from all multiplier transistors, and to detect the absolute change in current, ΔI_D. The circuit is time multiplexed, using two phases. During the first phase, signal zeros are switched into the multiplier gates and the output voltage is zeroed via a feedback loop, which bleeds the current I_{D_o} from the summing bus, through resistor R_{B}^o. During the second phase, the desired signal values are switched onto the multiplier gates, and the output from the current summing amplifier is the sum-of-products term required. Within the filter realisation, signal-zero switching is easily achieved through the floating-gate-tap reset transistor, whilst the reference voltages are applied to the multiplying transistor drains.

If signal information at d.c. (0 Hz) is not required (as is often the case in practice) then 2-quadrant multiplication is sufficient, we may remove the time-multiplex requirement and simply a.c. couple the output from the current summing amplifier, to detect the required output changes about an arbitrary zero. This arrangement is clearly much simpler and requires no switching operation, which in practice implies a faster realisation. The current summing amplifier itself may be a simple common-base bipolar transistor stage (off-chip). The single-transistor, time-multiplexed multiplying technique described here has been used with considerable practical success in a prototype programmable filter realisation, to be described. It is notably stable, easy to implement, and more accurate than a matched-transistor realisation.

III. DEVICE REALISATION

We have used these filter techniques to realise a prototype 64-point programmable transversal filter, and to design an improved 256-point filter, currently in development. Circuit details of the prototype filter cell are shown in Figure 4. A 3-phase CCD structure in metal-gate technology (6) was used, with two CCD stages between taps, on a pitch of 56 μm. Selection of reference update points is achieved via a NOR gate at each point, which decodes an externally-supplied reference address. Provision is also made for feedback linearisation of the reference

coefficients via a multiplexed feedback bus. Power dissipation is approximately 5 mW per cell (320 mW per chip) and speed is limited in practice, by complex timing waveforms, to sampling up to 100 kHz. All peripheral circuits (such as linearising amplifiers and clock drivers) are off-chip. Figure 5 shows a drawing of this prototype device, which measures 184 mils by 136 mils and practical results are reported in Section IV.

A new filter design is currently in development and includes several major improvements. A 2-phase CCD structure in double-level polysilicon technology (7) is to be used, with taps at every CCD stage on a new pitch of 28 μm (exactly half that used previously). This small pitch is made possible in part because of the self-aligning property of the MOS transistors fabricated on this process. Reference points are now updated serially, using a digital shift register selector, in order to reduce the pin-count. Power dissipation is cut to 1 mW per cell and a signal bandwidth of 10 MHz (sampling at 20 MHz) appears feasible from simulations. This should be more readily achieved in practice due to greatly simplified drive requirements. The active layout area of a 256-point block measures 144 by 124 mils, and is configured as 2 x 128 point filters, which may be cascaded, or run in parallel as quadrature channels. Input and output operational amplifiers are to be included on-chip in the signal channel, so that cascading is by means of a single wire.

The amplifiers are based on the switched-capacitor differential stage (8), including a single high-gain invertor to meet the following specifications :

Open loop gain	40 dB
Power dissipation	6 mW
Max clock frequency	2 MHz
Layout area	20 mils^2 (24,000 μm^2)

This form of operational amplifier is most suitable in these applications, in that it is automatically chopper-stabilised and requires no external compensation or adjustment. The additional layout area involved is minimal.

IV. RESULTS

The following results relate to a characterisation programme carried out on the prototype 64-point filter, using the time-multiplexed, 4-quadrant multiplication technique.

A suitable guide to noise performance may be obtained by examination of the impulse-response, of which a typical example is given in Figure 6. Under these conditions only one filter point is active at any time, whilst all points constantly contribute noise. From this example, the impulse response is found to have a dynamic range of 34 dB. Since this result must vary according to the number of filter points, a more meaningful figure may be obtained by referring it to a filter with a single point, which in this case gives a value ; D_{f_p} = 52 dB.

It is possible to use this parameter to derive the dynamic range of the complete filter with any arbitrary reference. For example, the best condition occurs for the matched filtering of two square waves, when all points contribute maximum power at the output. The corresponding dynamic range for matched square-waves using the 64-point device is thus 70 dB, which we have verified independently by measurement.

A good indication of filter accuracy is given by the stop-band performance of the device in a frequency-filtering mode. Figure 7(a) shows the frequency response of the filter having the impulse response shown in Figure 8, ideally a Hamming-weighted low-pass filter with stop-band suppression around -50 dB. The average stop-band attenuation achieved in practice is approximately -34 dB and indicates an equivalent multiplier accuracy (9) of approximately 2%. Figure 7(b) demonstrates improved stop-band performance, by a factor of 6 dB and was achieved by adjusting the reference coefficients to correct the observed impulse response, as described in Section V.

Use of the device in matched-filter mode is demonstrated in Figure 8 , where the centre trace shows a reference 'chirp' and the upper trace shows a corresponding signal chirp (from the

64th CCD tap, available for cascading). The output (lower trace) is clearly close to the ideal sinc form. A more testing (higher time-bandwidth) matched chirp result has been obtained from a 256-point filter shown in Figure 9 (a). This filter dissipates 3W and is constructed on a printed-circuit board measuring 6.3 x 9.2 ins, using 4 cascaded 64-point devices. Figure 9 (b) shows the correlation peak obtained by matching chirps of full Nyquist bandwidth (TB = 128), the output peak being a single impulse in this instance. Charge transfer inefficiency ultimately limits the maximum TB that may be processed. Independant simulations (10) of this effect show that correlation peaks remain usefully uncorrupted for TB up to 1000 with c.t.i. at 10^{-3} per tap.

V. ADAPTIVE FILTERING

We present in this section two circuit techniques which allow the filter to automatically achieve an optimal response, regardless of any inherent errors. The first technique, which we have called *iterative reference adaptation*, is used to achieve exactly, a specified impulse response. The control loop, shown in Figure 10, is formed around a micro-processor, which is used to monitor the filter output and apply a correction to the reference coefficients held in digital memory. The impulse response of the filter is monitored and compared to the existing reference coefficients, which are corrected if they deviate from the ideal value. Thus any ideal impulse response may be realised to a specified accuracy, regardless of multiplier and other circuit imperfections (11). The filter architecture described, with a static reference register, is ideally suited to this adaptation technique which can permanently trim out all coefficient weighting errors. It has been computed that an adaptation time of 1 second is sufficient to correct the impulse response of the 64-point filter to an equivalent accuracy of 8 bits.

Once corrected, the new reference values might be transferred to a PROM module on a dedicated filter board, to realise a stand-alone, accurately programmed filter. The microprocessor adaptation system would remain as a single laboratory facility for servicing these modules.

The second adaptive system is a realisation of the Widrow LMS algorithm (12), which may be used to force a desired filter output from an arbitrary input by rejecting all other signal components. A block diagram of the system is shown in Figure 11. The filter is supplied with two inputs, the signal input, s(t), and the desired filter response to this input, d(t). The objective is to force the filter output, r(t), to resemble d(t) as closely as possible, by adapting the reference weight vector $\underline{H}$ using the algorithm :

$$h_k(T + 1) = h_k(T) + 2\mu\epsilon(T)\ s(T - k)$$

where μ is a selected convergence factor, and $\epsilon(t) = d(t) - r(t)$; the subscript k denotes tap position and the term in brackets is the time index; T is normalised in units of one delay time.

This filter has been implemented using the 64-point prototype programmable device (13) and Figure 12 demonstrates its response to a sinusoidal wave at 1 kHz, contaminated by another signal at 5.4 kHz. The desired output is the 1 kHz sine and it can be seen that considerable rejection (35 dB) of the interfering signal takes place at the output (Figure 14(b)). The weight vector is shown in Figure 14(c) and forms the expected sinusoid.

In other performance tests this filter is found to compare well with published simulation results. Although the filter architecture is not optimised for the implementation of this algorithm, the device principles could be applied to a dedicated, adaptive chip design.

VI. CONCLUSIONS

We have shown how novel, linear MOS design techniques may be combined with state-of-the-art CCD technology to realise a monolithic programmable filter with great application potential. A prototype 64-point filter has been fabricated and has demonstrated useful performance characteristics in both frequency- and matched-filter configurations, and in adaptive modes. An improved 256-point filter chip is now in development which promises reduced power consumption (1 mW per point) and increased processing band-width

(possibly 1 MHz). The devices are relatively simple to drive and may be directly cascaded for matched filter applications up to time-bandwidth products of 1000.

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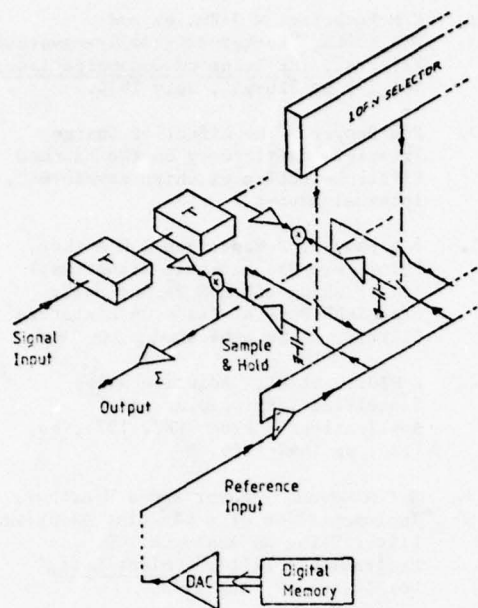
Figure 1   Block Diagram of Programmable
            Filter Architecture

Figure 2   MOS Multiplier Transistor
            Nomenclature

Figure 3   Multiplication and Summing
            Circuitry
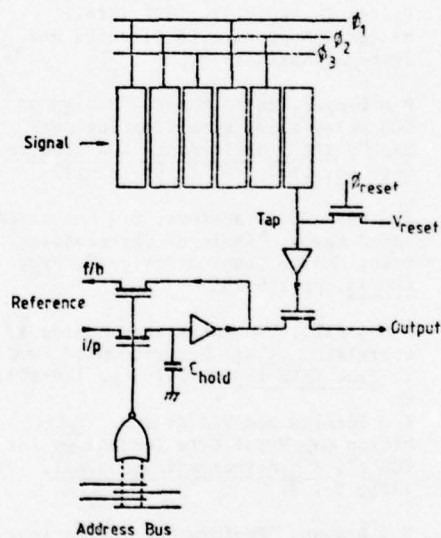
Figure 4   Circuit Diagram of Prototype
            Filter Cell, 3-Phase Metal
            Gate CCD.

3B-16
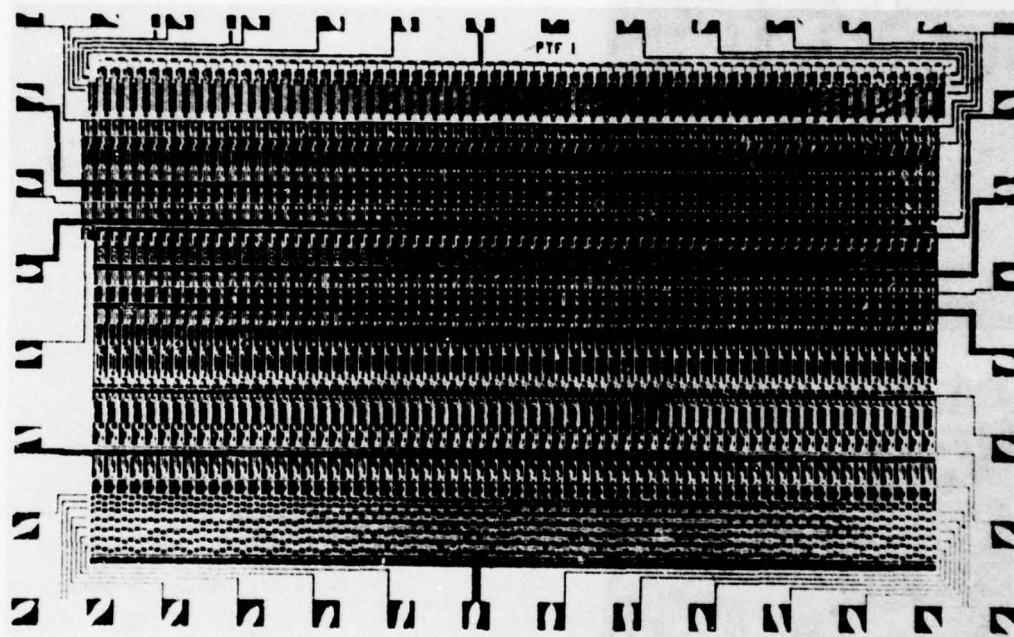
Figure 5   Prototype 64-Point
Programmable Filter, Die Size
184 x 134 mils

Figure 6 Impulse Response, Hamming
Weighted Low Pass Filter,
Pass-Band 0 – f_c/8 Hz
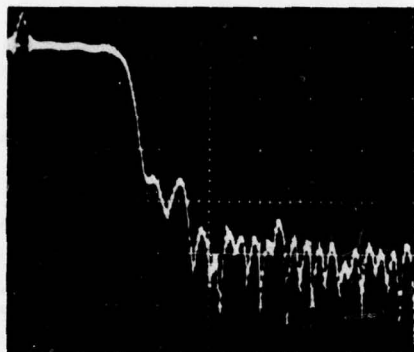
Figure 7(a) Frequency Response of
Hamming Weighted Low Pass
Filter; Reference Directly
Applied.

Horizontal : 1 kHz/cm
Vertical : 10 dB/cm
f_c = 16 kHz
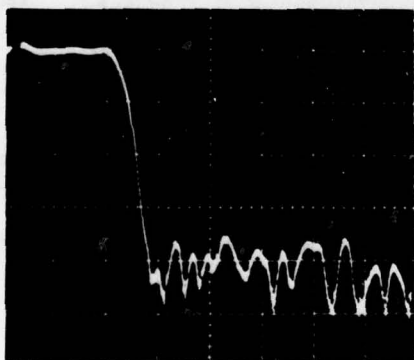
Figure 7(b) Frequency Response as
Above but With (Visually)
Corrected Impulse Response
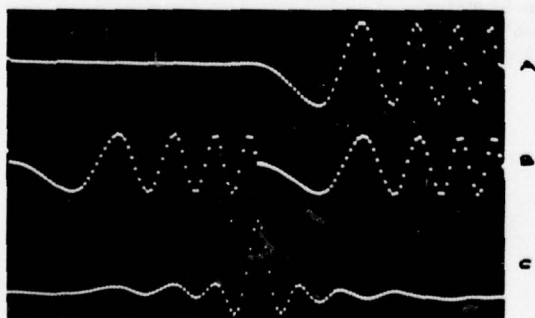
Figure 8 Matched Filtering of a 64-
Point Chirp Waveform
0 – f_c/8 Hz.

(a) Signal at 64th CCD Tap 1V/cm
(b) Reference Waveform 5V/cm
(c) Filter Output 5V/cm

Horizontal : 2 ms/cm

3B-18
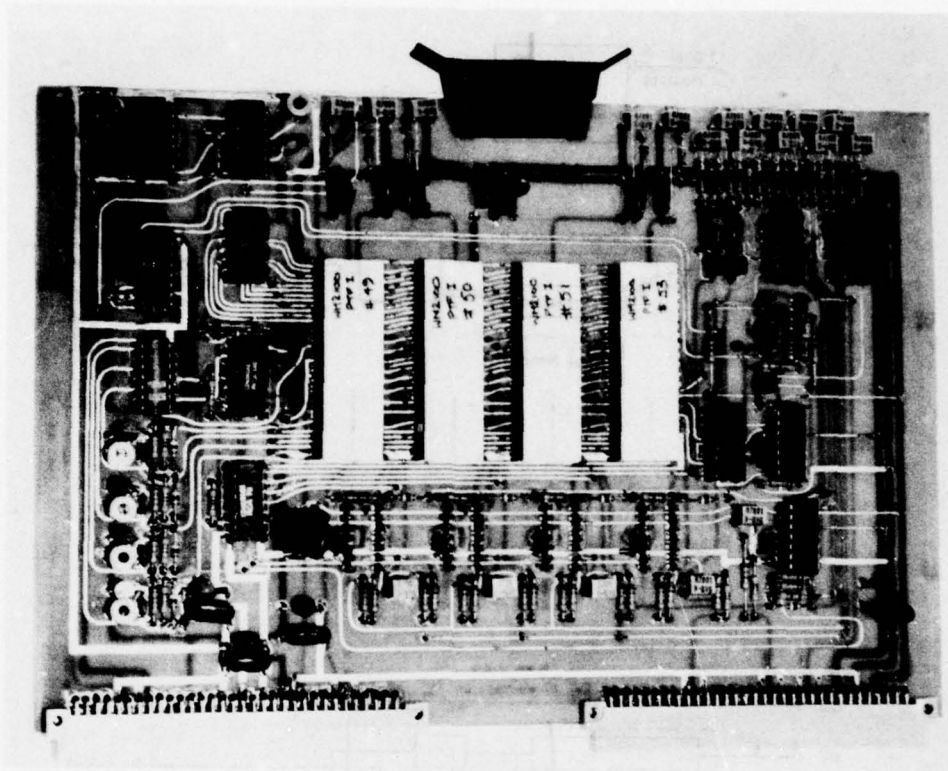
Figure 9(a)   256-Point Programmable
Filter Board Containing 4
Cascaded 64-Point Prototype
Devices with Drive Electronics
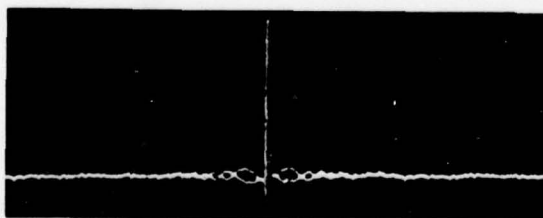
Figure 9(b)   Matched Filter Response to
256-Point Chirp Waveform
$0 - f_c/2$ Hz (TB = 128)
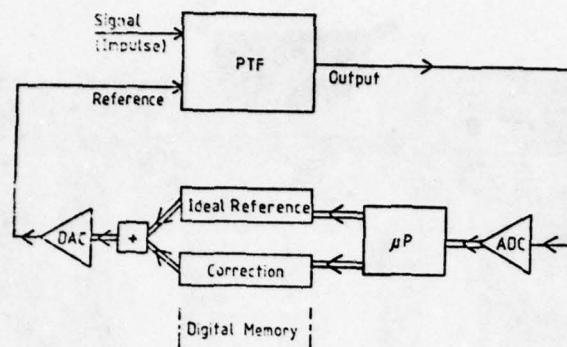
Figure 10   Block Diagram of Control
Loop for Adaptive Correction
of Reference Coefficients
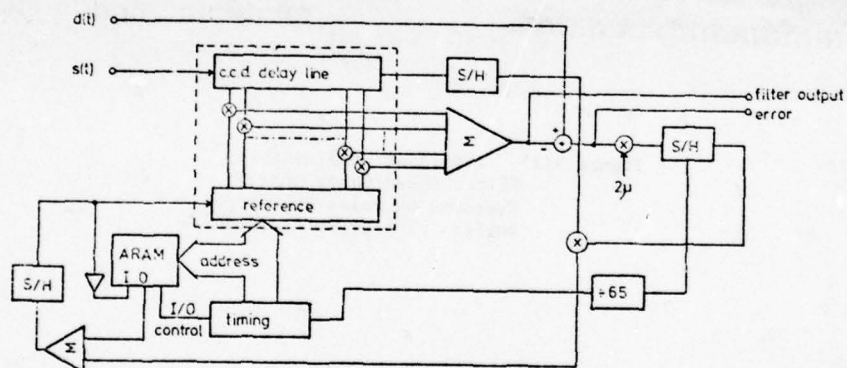
Figure 11   Block Diagram of Adaptive
Filter, Based on Widrow LMS
Algorithm
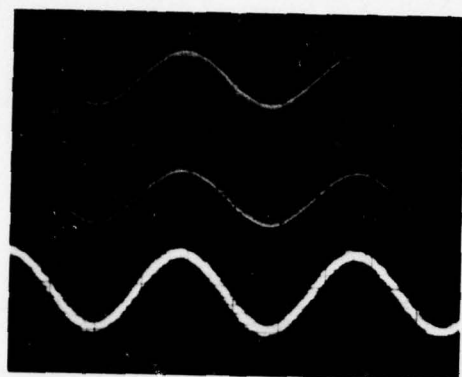
Figure 12 Adaptive Filter Response to
          1 kHz Sinewave with 5 kHz
          Interference.

(a) Contaminated Input Signal
(b) Output Signal
(c) Adapted Tap Weight Vector
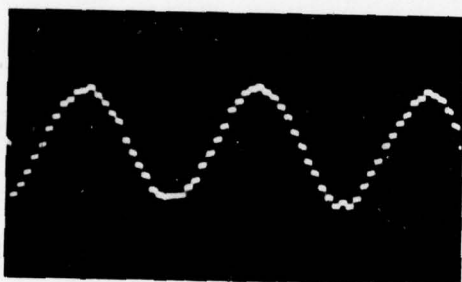
PROGRAMMABLE TRANSVERSAL FILTER USING CCD COMPONENTS

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Over the past few years, CCD transversal filters have demonstrated their ability to perform several signal processing functions. The normal method of fabricating these devices involves the definition of the required weighting function in the electrode structure. Thus the technique is only applicable where (1) large volumes of a particular filter function are required and (2) there is no operational requirement to change the filter function. There are many filtering applications which are suited to CCDs but these requirements are not fulfilled. This device is aimed at applications with bandwidths below approximately 20 kHz (e.g. Sonar, Audio and Radar range bin processing) which fall into these categories. These applications do not normally utilise the bandwidth available from CCDs and in this device this bandwidth is traded for external programmability. Within the performance limitations any function which can be carried out with a transversal filter can also be realised with this device.

The transversal filter block diagram can be reconfigured such that the filter tap weight coefficients can be stored in a R.O.M. and applied to the input signal by means of a multiplying D.A.C. A CCD can then perform the necessary signal delay and summation functions. In this way the filter characteristic can be changed simply by changing the R.O.M. Alternatively, if some alterable form of storage is used, the filter characteristic can be operationally modified. A micro-processor can conveniently be used here to calculate the necessary changes in weighting coefficients and thus make an adaptive filter.

A CCD chip has been designed to perform the delay and summation function. The R.O.M. and multiplying DAC are readily available at low cost. This paper describes the concept of the device and the design of the CCD chip. At the time of writing, however, experimental results were not available.

1. INTRODUCTION

Where a fixed filter function is required a CCD split electrode transversal filter offers a low power, low weight, and, if the quantities are large enough, a low cost solution. However, if (i) the quantities do not warrant the production of a specialised mask set or (ii) there is an operational requirement to change the filter function the split electrode filter is not suitable. Such applications can be satisfied with a CCD analogue correlator structure using analogue multipliers. The problems involved with such a system include:-

(a) four quadrant analogue multipliers must be provided and these will limit the effective accuracy of the weighting coefficients. The dissipation of the multipliers will also be significant.

(b) the on chip storage time for the analogue reference channel will be limited.

Thus provision must be made for some more permanent form of storage for the weighting coefficients and a system of periodic refresh. Filter configuration considerations apart, it is often convenient to use a DAC and store the coefficients in digital form, either in a R.O.M. or as calculated by a microprocessor as part of an adaptive system.

These problems are not insoluble. The alternative presented here is based on the fact that CCDs are well suited to:-

(a) series to parallel data stream conversion and

(b) merging of charge packets to perform summation.

2. PRINCIPLE OF OPERATION

Fig. 1 shows the transversal filter block diagram as adopted by the split electrode CCD filter. This system is described by:-

$$V_{out} = \sum_{n=1}^{N} a_n \, s(t - [n-1]\tau)$$

where s(t) is the input signal and τ is
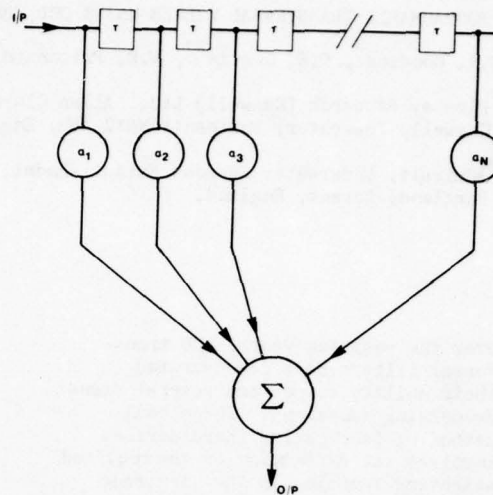
Fig. 1 Block diagram of conventional transversal filter
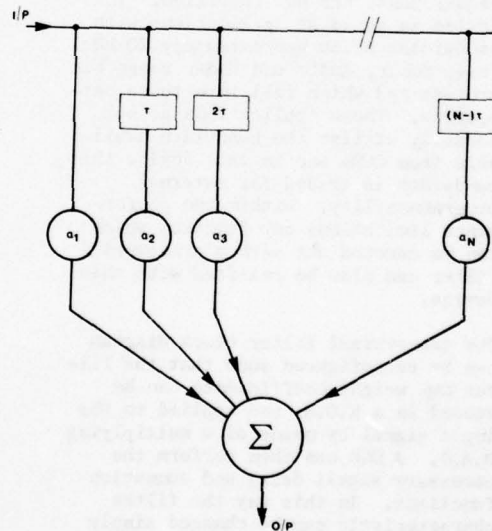
Fig. 2

the stage delay (clock period). This series realisation can be converted into the parallel realisation of Fig. 2. This is functionally the same as Fig. 1 but, of course, requires many more delay elements.

For most filtering applications the reference is stationary or quasi-stationary. This means that the delay elements and multipliers can be interchanged (Fig. 3).
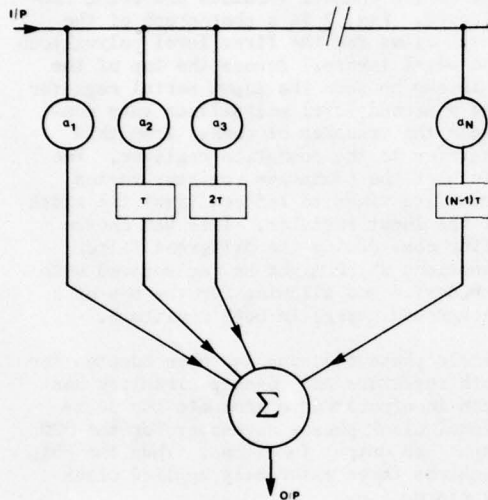
Fig. 3

This scheme is not very attractive since it involves a large number of multipliers and delay elements. The delay and summation elements of Fig. 3 can, however, be rearranged (Fig. 4) to reduce the number of delays without changing the function performed.

N multipliers are still required. However, for applications of modest bandwidth one multiplier can effectively be multiplexed. This can be achieved (Fig. 5) by using a CCD to transport the N outputs of the multiplier to the correct summation elements (Fig. 4).
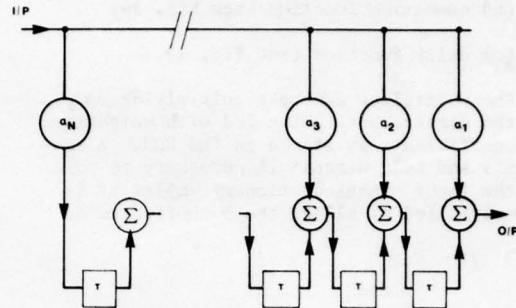
Fig. 4

This system is again described by:-

$$V_{out} = \sum_{n=1}^{N} a_n \; s(t - [n - 1] \tau)$$

This scheme can now be partitioned as shown in Fig. 6. The CCD chip performs the following functions:-
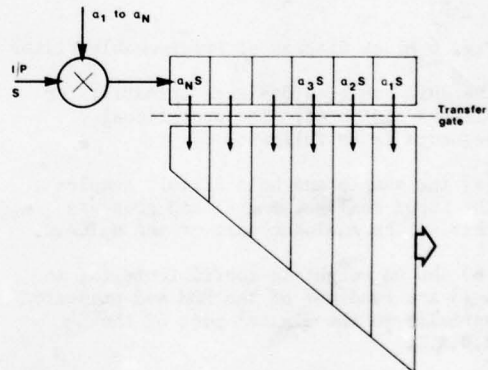
Fig. 5

(a) serial to parallel conversion necessary to multiplex the multiplier,

(b) summation function (see Fig. 4),

(c) delay function (see Fig. 4).

The multiplier can be a multiplying DAC, the digital port being fed with weighting coefficients as stored in the ROM. A sample and hold circuit is necessary to hold the input signal stationary whilst it is multiplied by all of the N coefficients.
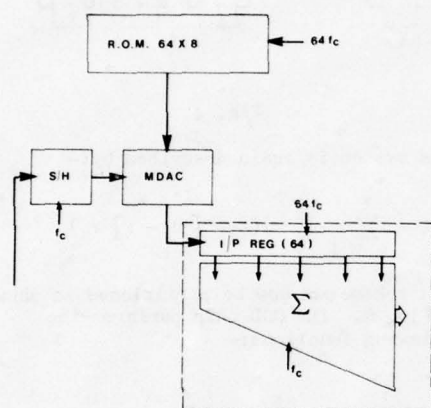
Fig. 6 Block diagram of Programmable Filter

The chip has been designed primarily for filters of $N = 64$. The operational sequence is as follows:-

(a) the sample and hold circuit samples the input analogue signal and presents this to the analogue port of the M.D.A.C.

(b) the 64 weighting coefficients (a_1 to a_{64}) are read out of the ROM and presented serially to the digital port of the M.D.A.C.

(c) the CCD i/p register is clocked so as to sample the 64 M.D.A.C. output products.

(d) the 64 products are transferred to the summation CCD register.

(e) the summation CCD is clocked once,

thus advancing its contents by one stage.

(f) a new sample of the analogue i/p signal is taken by the sample and hold circuit and items (b) to (e) are repeated.

3. CCD CHIP DESIGN

The chip has been designed for the two-level polysilicon gate N channel CCD process which incorporates an auto aligned implanted barrier. Both surface channel and buried channel versions are being fabricated. Fig. 7 is a photograph of the check films for the first level polysilicon and metal layers. Across the top of the chip can be seen the input serial register and a second level polysilicon gate controls the transfer of charge from this register to the summation register. The width of the summation register varies from five times to fifteen times the width of the input register. This was chosen after considering the different filter functions which might be implemented with the device and allowing for the use of a background charge in both registers.

Single phase clocking has been adopted for both registers and on-chip circuitry has been incorporated to generate the additional clock phases necessary for the CCD input and output functions. Thus the chip requires three externally applied clock waveforms i.e.

(a) summation register at f_c,

(b) input register at Nf_c and

(c) parallel transfer clock at f_c.

The chosen value of N is 64, so conceivably on-chip divider circuits could have been incorporated to generate the summation register clock and parallel transfer clock from an applied clock for the input register. As will be seen later, chips can be cascaded to make filters of length greater than 64, thus changing the required division ratio. For this reason the slow clocks were not generated on chip. The serial input register requires an input technique which has a linear voltage to charge conversion, because any error here will have an effect similar to weighting coefficient error. Since the
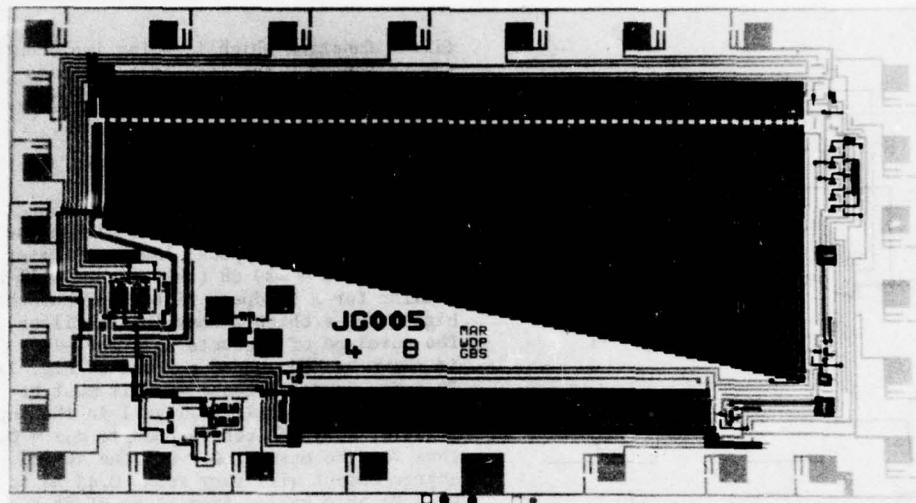
Fig. 7 Chip Layout
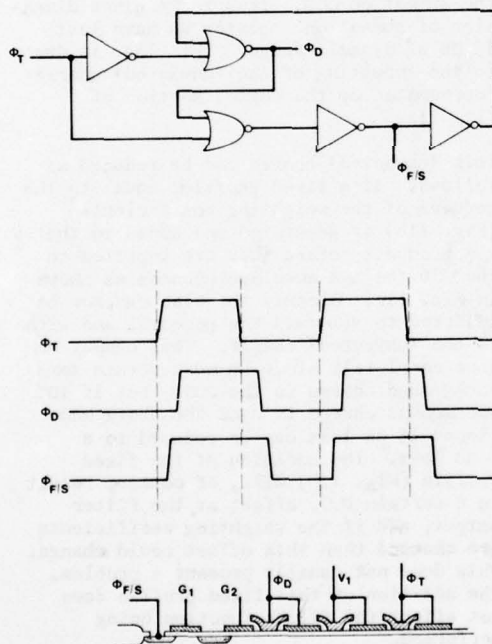
Fig. 8 CCD Input Scheme

operating frequency of 4 MHz was regarded as too high for the phase referred technique (Ref 1) to exhibit good linearity, the fill spill technique was chosen. The gating circuitry shown in Fig. 8 generates the fill and spill clock which is applied to the input diode, and a delayed clock which is applied to the first stage of the CCD. This arrangement is necessary to preserve the correct timing.

Fig. 9 shows the timing of all the clock waveforms associated with the output of the summation CCD register and the following sample-and-hold circuit, and the gating circuitry used to generate them. The output buffer circuit is designed to have good linearity as this is particularly important when chips are cascaded. The chip also incorporates several bias chains in order to further reduce the number of peripheral components required to operate the device.

Fig. 7 also shows an additional 64 stage CCD to be on the chip. This is provided for cascading purposes. By using this delay as shown in Fig. 10, a 128 stage filter can be constructed, and this principle can be extended to even longer filters. The problem, of course, is that as the filter is lengthened the available bandwidth is reduced. Since the maximum designed frequency for the input serial
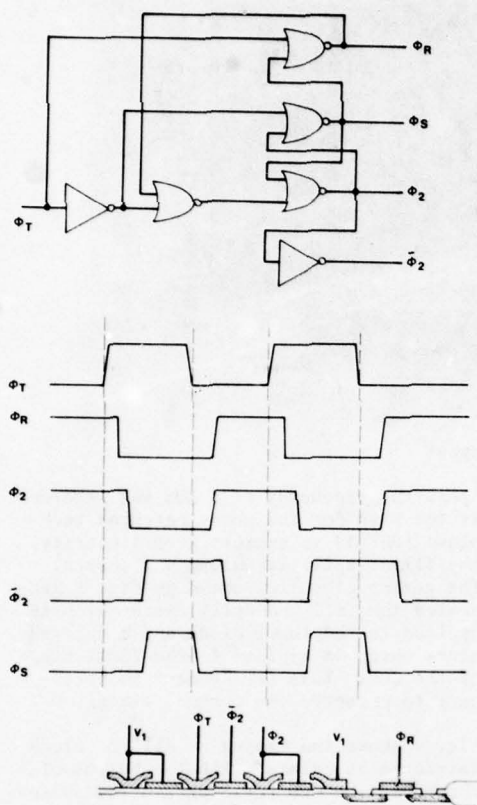
Fig. 9 Output Scheme

register is 4 MHz, $f_c = 4 \dfrac{MHz}{N}$ i.e. 60, 30, and 20 KHz for a 64, 128 and 192 stage filter respectively. The cascading delay line adopts the same output scheme as the summation register (Fig. 9) and since it operates at a relatively low clock frequency the phase referred input technique (Ref 1) has been used. The phasing of the input has been arranged such that this input can be connected directly to a summation register output.

4. DYNAMIC RANGE

The output dynamic range available will depend upon the gain of the particular filter function which is being implemented. Let us consider the case of a low pass filter. If we define gain as:-

$$G = \frac{1}{s(t)N} \sum_{n=1}^{n=N} a_n \, s(t - [n-1]\tau)$$

where $s(t)$ is an input signal within the passband, then a typical low pass filter might have $G = -20$ dB (this figure will be similar for a bandpass filter and somewhat higher for a chirp Z convolution filter). The envelope of products $a_n s$ for $-1 < s < +1$ is shown by the shaded portion of Fig. 11a. In order to accommodate this, it must be arranged that a half full well in the input register (say $q/2$) corresponds to $a_n s = 0$. Thus for the case of $G = 0.1$ the summed charge output will vary from 0.45 Nq to 0.55 Nq as s varies from -1 to +1 at a frequency within the passband. This means that the peak to peak range of the output signal can only be $\dfrac{0.1}{0.55}$ (i.e. approx -15dB) of the total signal handling capability of the summation CCD. Thus for a given dimension of summation register we have lost 15 dB of dynamic range. This loss is due to the inputting of the 'unwanted' charge represented by the dotted section of Fig. 11a.

This 'unwanted' charge can be reduced as follows. If a fixed profile, equal to the modulus of the weighting coefficients (Fig. 11b) is generated and added to the a_ns products before they are inputted to the CCD the a_ns envelope becomes as shown in Fig. 11c. Clearly the bias can now be adjusted to subtract the pedestal and with it the 'unwanted' charge. This cannot be done completely since we must retain some background charge in the CCDs, but if 10% background charge is used the above mentioned 15 dB loss can be reduced to a 6 dB loss. The addition of the fixed profile (Fig. 11b) will, of course, result in a certain D.C. offset at the filter output, and if the weighting coefficients are changed then this offset could change. This does not usually present a problem. The addition of this fixed profile does not affect the filter function being performed.

This scheme is relatively simple to implement (see Fig. 12). The only additional
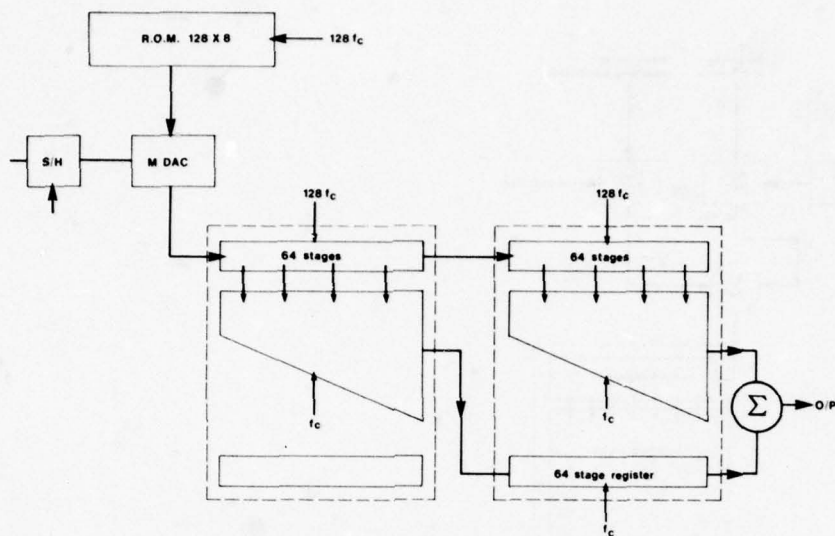
Fig. 10 Cascading of programmable filter chips

component required is a second M.D.A.C.
The weighting coefficients are already
available and their modulus can be obtained
by omitting the sign bit. Summation of
the outputs of the two MDACs is also sim-
ple since MDACs normally provide current
outputs.

5. CONCLUSIONS

System functions which can be implemented
with the device include:-

(a) low pass and bandpass frequency
filtering,

(b) chirp Z filters for spectral analysis,

(c) correlation,

(d) adaptive filtering (including adaptive
equalisation).

The flexibility of the approach has crea-
ted interest particularly in the sonar
field, where many different filter func-
tions are required but only in small
quantities.
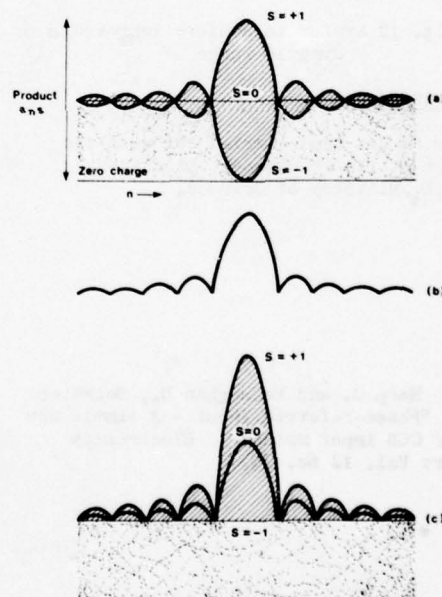
Fig. 11 Charge profile in CCD input register
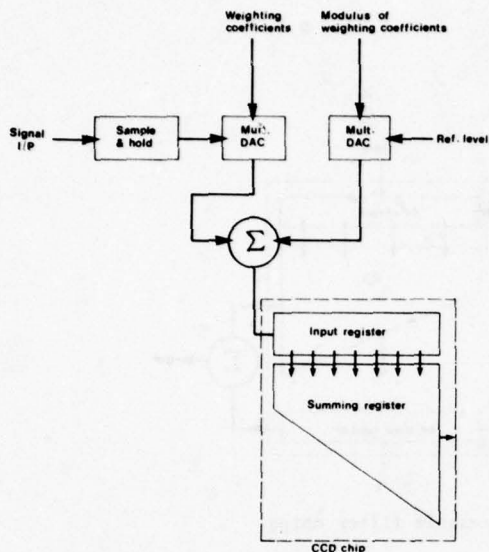
Fig. 12 System to achieve improved
dynamic range

*Ref 1 Harp G. and McCaughan D., December
1976 "Phase-referred Input – A simple new
linear CCD input method". Electronics
letters Vol. 12 No. 25.

A CCD TWO DIMENSIONAL TRANSFORM

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ABSTRACT. The two-dimensional transform is recognized as a valuable tool for processing two dimensional signals. It has applications in bandwidth reduction systems, image enhancement systems, correlation trackers, seismic array processors, and radar and sonar systems. A 32 x 32 point discrete Fourier transform has been built using two low power CCD integrated circuits – a 32 point DFT IC and a 32 x 32 point reformatting CCD memory. The detailed design and operation of this two dimensional transform breadboard are described.

I. INTRODUCTION

Since the introduction of the charge-coupled device (CCD) in 1970[1], the CCD has become an important element for implementing many signal processing functions, one of which is spectral analysis via the chirp Z transform (CZT) algorithm.[2-3] This algorithm for obtaining the discrete Fourier transform (DFT) is ideally suited to CCD implementation as the bulk of the computation may be performed in CCD transversal filters. In 1977, a monolithic 32 point CCD DFT IC which implements the chirp Z transform algorithm was designed and fabricated.[4] With this chip a 32 point one-dimensional DFT may be obtained in 64 µs with a power dissipation of 600 mW. Although the one-dimensional DFT has many applications, there are a variety of applications which require the processing of two dimensional signals such as obtained from images, seismic arrays, and sonar and radar systems. The two-dimensional DFT may be realized via the one dimensional DFT by first transforming the rows of a two dimensional array and then transforming the columns of the resulting two dimensional array.[5] To implement this, the data output of the first transformation must be reformatted to become the input data for the second transformation. In 1978 a 32x32 point corner turning memory (CTM) using a novel two dimensional charge transfer structure was designed and fabricated. This CCD CTM is ideally suited to perform the reformatting operation.

This paper describes the implementation of a 32 x 32 point two dimensional discrete Fourier transform using the 32 point CZT IC and the 32 x 32 point corner turning memory. Section II reviews how the two dimensional DFT may be implemented with one dimensional DFTs. Sections III and IV describe in detail the 32 point CCD CZT IC and the 32 x 32 point CCD corner turning memory. Section V presents the results of implementing the two dimensional DFT with these two CCD ICs.

II. THE TWO DIMENSIONAL DFT

The DFT of a finite area sequence $f(m,n)$ is

$$F(k,\ell)= \sum_{m=o}^{M-1} \sum_{n=o}^{N-1} f(m,n) e^{-j2\pi(\frac{km}{M}+\frac{\ell n}{N})} \quad (1)$$

The two dimensional DFT can be interpreted in terms of the one dimensional DFT by expressing Equation (1) as

$$F(k,\ell)= \sum_{m=o}^{M-1} G(m,\ell) e^{-j2\pi\frac{km}{M}} \quad (2)$$

where

$$G(m,\ell)= \sum_{n=o}^{N-1} f(m,n) e^{-j2\pi\frac{\ell n}{N}} \quad (3)$$

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The function $G(m,\ell)$ corresponds to an N-point one dimensional DFT for each value of m, i.e, it consists of M one dimensional transforms, one for each row of $f(m,n)$. The two dimensional DFT $F(k,\ell)$ is then obtained by performing N one dimensional transforms, one for each column of the sequence $G(m,\ell)$. Thus, the two dimensional transform can be implemented as shown in Figure 1.

INPUT → 32 PT CZT → 32 X 32 CORNER TURNING MEMORY (CTM) → 32 PT CZT → OUTPUT
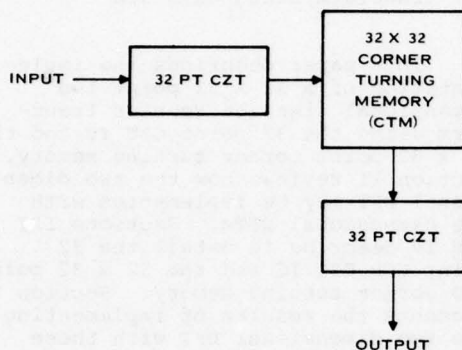
Figure 1. Implementation of Two Dimensional Discrete Fourier Transform.

A one dimensional transform is performed on the rows of the signal using a CCD CZT IC. The resulting complex Fourier coefficients are stored row by row in two CCD corner turning memories. Next these coefficients are read out column by column into a second CCD CZT IC which completes the calculations for the two dimensional transform.

III. 32 POINT CCD CZT IC

A monolithic 32 point DFT using the chirp Z transform algorithm has been designed and fabricated using an N channel, two level polysilicon coplanar electrode process. Goals of the design included the elimination of all external support components and operation of the transform IC at a 1 MHz data rate. Small size,

low weight, low power, and high speed are achieved with total integration.

The chirp z transform algorithm is derived by starting with the definition of the discrete Fourier transform:

$$F_k = \sum_{n=o}^{N-1} f_n e^{-j\frac{2\pi kn}{N}} \qquad (4)$$

and making the substitution:

$$2nk = n^2 + k^2 - (n-k)^2 \qquad (5)$$

The chirp Z transform equation results:

$$F_k = e^{-j\frac{\pi k^2}{N}} \left[\sum_{n=o}^{N-1} (f_n e^{-j\frac{\pi n^2}{N}}) e^{j\frac{\pi(k-n)^2}{N}} \right] \qquad (6)$$

Equation 6 has been factored to emphasize the three operations which make up the CZT algorithm: (1) pre-multiplying the time signal with a chirp (linear FM) waveform, (2) filtering in a chirp convolution filter, and (3) postmultiplying the Fourier output by a chirp waveform. This is illustrated in Figure 2.

IN f_n ⊗ y_n ⊗ $e^{+j\frac{\pi n^2}{N}}$ ⊗ F_k OUT

$e^{-j\frac{\pi n^2}{N}}$ Down Chirp — Filter having up chirp impulse response — $e^{-j\frac{\pi k^2}{N}}$ Down Chirp
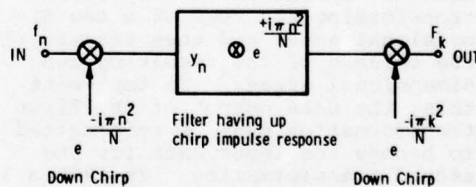
Figure 2. Schematic of Chirp Z Transform Algorithm.

The chirp Z transform IC is divided into two sections. The first section contains the multipliers which are implemented using multiplying digital-to-analog converters (MDACs). Analog input signals applied to the MDAC reference terminals are multiplied by binary coded chirp waveforms stored in a ROM. External digital inputs are provided to bypass the ROM for multiplicaton by other waveforms. Differential MDAC analog inputs, and uncommitted outputs allow maximum flexibility in total system configuration.

The second portion of the chip performs the chirp filtering operation. Four 63 stage transversal filters are needed to implement the complex chirp convoluton required by the CZT algorithm. The weighting coefficients for the sine and cosine chirp filters are:

$$h_k^{\cos} = \cos \frac{\pi k^2}{32} \qquad k = 0, 62$$

$$h_k^{\sin} = \sin \frac{\pi k^2}{32} \qquad k = 0, 62 \qquad (7)$$

The coefficients are realized using the split-electrode technique.[6] The CCD filters are two phase, coplanar electrode structures with ion implant wells.[7] Operational amplifiers provide differential inputs and outputs for the CCD filters, again for the purpose of versatility. In practice, the filters are loaded with 32 time domain data samples, and then the input is blanked while the convolution is performed. Thus, a single chip yields a DFT output with a 50% duty cycle. In this mode of operation, the 4 MDAC's provided can be multiplexed to do both pre- and post-multiplication. If 100% duty cycle output is required, two chips are used, and the 8 MDAC's included are sufficient for the needed multiplications.

All clock waveforms are generated on chip from a two phase master clock, and the system timing is such that it is possible to cascade CZT's for the purpose of multi-

dimensional transforms, or for performing correlation by multiplication in the frequency domain.

A block diagram of the CZT chip is shown in Figure 3, and a photomicrograph of the IC is shown in Figure 4. The IC measures 6.04 x 5.69 mm^2 (238 x 224 mil^2). Details relating the performance of the 32 point CZT IC have been described elsewhere.[4]
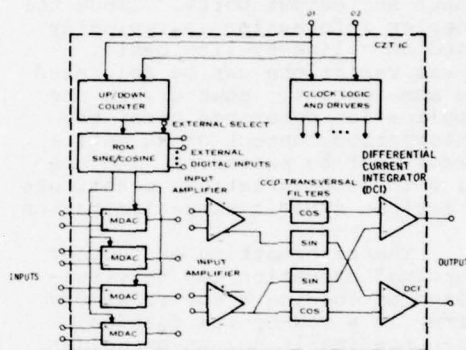
Figure 3. Block Diagram of 32 Point CCD CZT IC
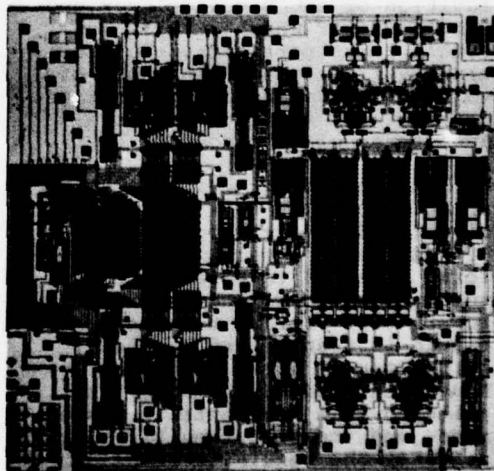
Figure 4. Photomicrograph of 32 Point CCD CZT IC.

IV. 32 X 32 CCD CTM

Analog CCD reformatting memories have been recently applied in high speed processors for pulse doppler radar in conjunction with surface acoustic wave device chirp transform units. [8-12] These memories are predominantly line-addressable CCD delay line structures which exhibit line-to-line offset and gain variations due to fluctuations in MOS transistor threshold voltages at the multiple input and output ports. Since the doppler information is typically used on a line-by-line basis, these variations can be tolerated to some extent. However, in the application described here, the information content of an entire frame must be preserved, and the line-to-line variations constitute a serious dynamic range limitation.

The reformatting or "corner turning" operation can be visualized as loading a square memory array in a row-by-row fashion, then reading it column-by-column. The most direct realization involves the use of a memory structure in which charge can be transferred either horizontally or vertically. [13] This realization is further enhanced with the addition of a CCD multiplexer and demultiplexer which results in a single input port and output port, thereby minimizing the number of voltage-charge and charge-voltage conversions, and their troublesome threshold dependence.

A block diagram illustrating the operation of this two dimensional CCD memory appears in Figure 5. The input demultiplexer performs a serial to parallel conversion and loads the memory array row-by-row. During the load cycle charge is transferred vertically in the memory array. When all rows have been loaded, the array is switched to a horizontal transfer mode, and the output multiplexer performs the requisite parallel to serial conversion of the data stored in each column.
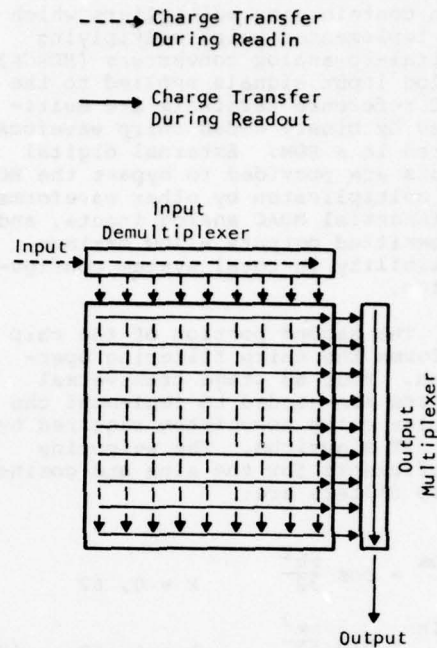
Figure 5. Block Diagram of the Corner Turning Memory (CTM)

A 32 x 32 element CCD memory based on this architecture has been designed and fabricated using the same process utilized for the 32 point CZT IC. A photomicrograph of the chip appears in Figure 6. In order to permit 100% duty cycle in other applications, an additional multiplexer and demultiplexer were included at the bottom and right of the memory array. The memory array is composed of 1024 three-phase two dimensional charge transfer cells placed on 2.0 mil centers. It operates as two interleaved two-phase structures with one common phase. The multiplexer and demultiplexer are four phase structures in order to match the pitch of the memory array and maintain short transfer lengths for good CTE. The structure is buried channel, with the exception of the demultiplexer input circuitry.
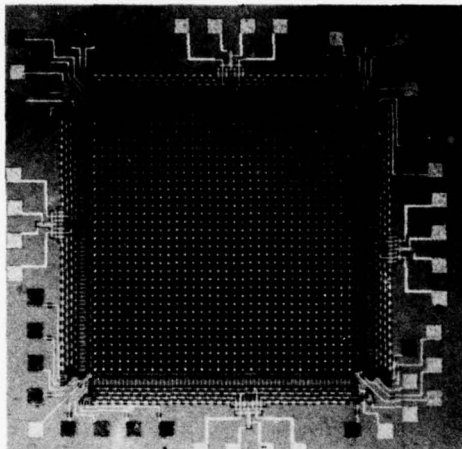
Figure 6. Photomicrograph of Corner Turning Memory (CTM)

The chip has been successfully operated at data rates in excess of 5 MHz. Dynamic range is still dictated by threshold variations in the multiplexer and demultiplexer channels which result in "fixed pattern" noise components. However, nearly 40 dB dynamic range (peak signal to peak noise) is achieved across the entire frame as compared to less than 20 dB observed in a previous line addressable design.[10]

V. **EVALUATION OF CCD TWO DIMENSIONAL TRANSFORM**

Implementation

A detailed block diagram of the CCD two dimensional transform is shown in Figure 7. A one dimensional DFT is performed on the rows of a real input signal, $f(m,n)$, using the 32 point CZT IC. The real and imaginary Fourier coefficients, $G_R(m,\ell)$ and $G_I(m,\ell)$ are reformatted in two CCD CTMs resulting in transposed matrices $G_R^T(m,\ell)$ and $G_I^T(m,\ell)$. A second one dimensional transform is performed on the transposed data from the CTMs. The final postmultiply operation has been replaced by a magnituding operation.

All timing pulses needed for the CTM operation are generated externally using standard TTL circuits and TTL-MOS drivers. This control circuitry also provides the two phase clocks and synchronization pulses needed for the CCD CZT ICs. Due to a photomask error, the tapweights of the CCD filters on the CZT IC were shifted one stage thereby shifting the output sequence of the Fourier coefficients by one position. This also precludes use of the on chip MDACs for postmultiplication operations.[4] Therefore the MDACs of another CZT IC using a delayed sync pulse were used to perform the postmultiplication needed in the first one dimensional transform.

In order to facilitate interfacing the analog circuitry and to simplify system timing and synchronization, evaluation of this demonstration unit was performed at a 100 kHz data rate.

Experimental Results

A simple two dimensional input test signal was generated by multiplying two analog signals together in a 4 quadrant analog multiplier. One signal provides variations along the horizontal axis and corresponds to the rows of $f(m,n)$. The second signal is sampled once per row and amplitude modulates the first signal to provide variations along the vertical axis and thus along the columns of $f(m,n)$. An example of the two dimensional input signal is shown in Figure 8 for sinusoidal signals. The signals are synchronized by the master timing to provide phase lock for the photographs. Figure 8a shows the input signal for a complete frame, i.e., 32 rows and 32 columns. Figure 8b is an expanded view of the input for one row. In addition, a DC offset was added to the two dimensional test signal in order to mark the origin $F(1,1)$ of the two dimensional transform. Figures 9 through 12 illustrate the operation of the two dimensional transform with the input signal of Figure 8.
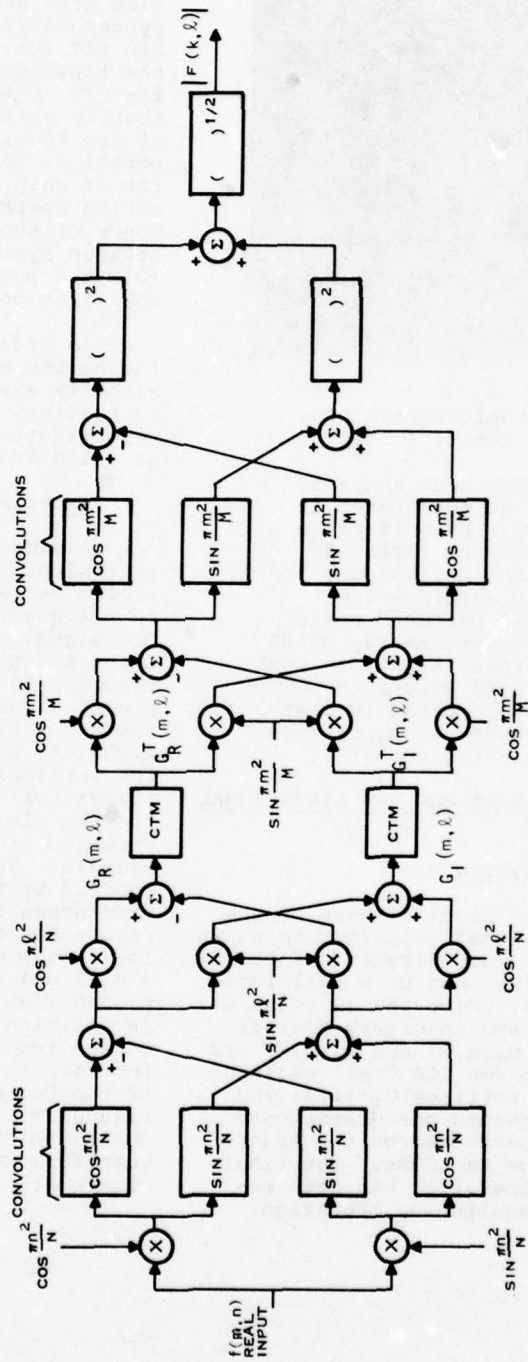
Figure 7 Implementation of the Two Dimensional Discrete Fourier Transform

f(m,n)

(a) 1 Frame (2ms/cm)   (b) 1 Row (50μs/cm)
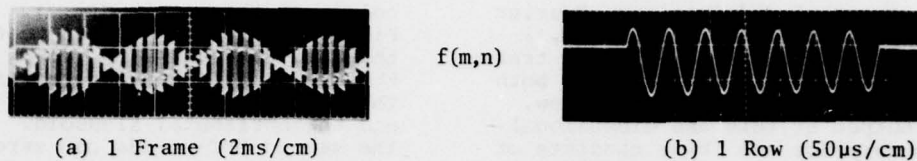
Figure 8.   Input to Two Dimensional DFT

$G_R(m, \ell)$

$G_I(m, \ell)$

(a) 1 Frame (2ms/cm)   (b) 1 Row (50μs/cm)
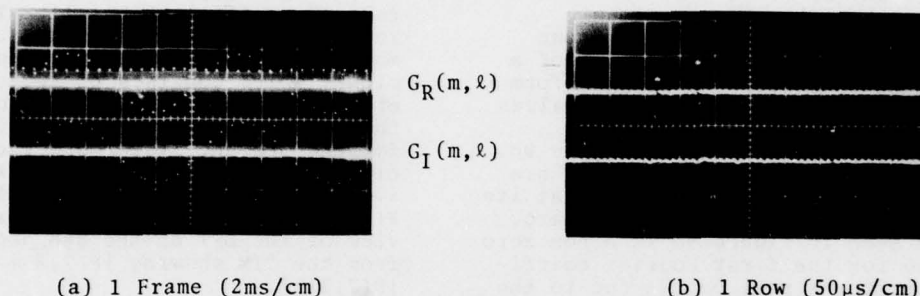
Figure 9.   Output of First One Dimensional Transform $G(m, \ell)$

$G_R^T(m, \ell)$

$G_I^T(m, \ell)$

(a) 1 Frame (2ms/cm)   (b) 1 Row (50μs/cm)
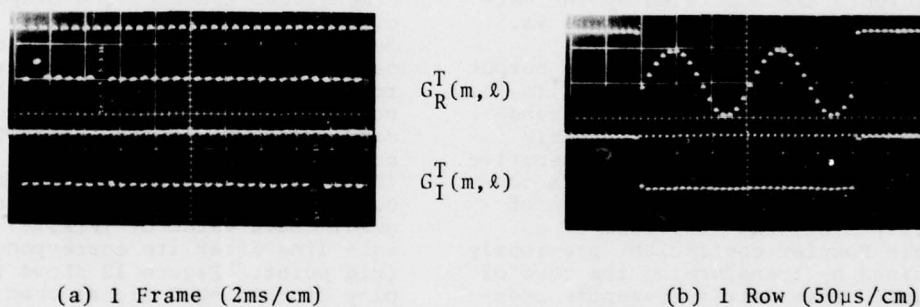
Figure 10.   Output of Corner Turning Memory $G^T(m, \ell)$

$|F(k, \ell)|$

(a) 1 Frame (2ms/cm)   (b) 1 Row (50μs/cm)
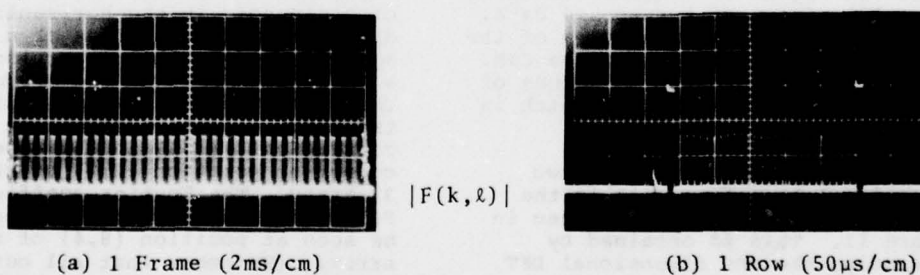
Figure 11.   Output of Second One Dimensional Transform

The real and imaginary Fourier coefficients, $G_R(m,\ell)$ and $G_I(m,\ell)$ from the first one dimensional transform are shown in Figure 9 for both the entire frame and for one row. The output of this one dimensional transform for one frame consists of 32 groups of 32 Fourier coefficients, one group for each row of the input signal $f(m,n)$. The Fourier coefficients in each group appear in the order 32, 1, 2, 3, ..., 31 due to the photomask error previously mentioned. The horizontal input signal consists of six cycles of a sinusoid. Therefore the transform of a row results in non zero values for the 7th and 27th Fourier coefficients as shown in Figure 9b. The real and imaginary outputs are 90° out of phase, thus one is at its peak value when the other is zero. Also seen in Figure 9b is a non zero value for the first Fourier coefficient of the real output due to the DC offset of the input signal. Note that with the exception of the DC coefficient the non zero Fourier coefficients are modulated by the vertical signal as seen in Figure 9a.

Figure 10 illustrates the output of the corner turning memory $G^T(m,\ell)$. The corner turning operation transposes the coefficients previously stored, $G(m,\ell)$, thus each consecutive group of 32 points from the CTM consists of the data in one column of $G(m,\ell)$, i.e., the 32 values of a single Fourier coefficient previously obtained by transforming the rows of $f(m,n)$. This matrix transpose operation is confirmed by comparing the CTM outputs in Figure 10 to the CTM inputs in Figure 9. Figure 10a shows a complete frame of transposed data. Figure 10b is an expanded view of the 8th group of 32 points from the CTM. This corresponds to the 32 values of the 7th Fourier coefficient which is the 8th column of $G(m,\ell)$.

The final output of the two dimensional transform unit is the magnitude $|F(k,\ell)|$ which is seen in Figure 11. This is obtained by generating the one dimensional DFT of each of the 32 groups of 32 points from the CTM. This corresponds to obtaining the transform of each column of the matrix $G(m,\ell)$. From Figure 10a it can be seen that only the 2nd, 8th, and 28th groups from the CTM contain non zero coefficient These are due to the input DC offset and the horizontal sinusoid. Thus the second DFT yields non zero coefficients only in the 1st, 7th, and 27th rows of $F(k,\ell)$. The second group from the CTM represents the unmodulated DC offset. The DFT of this group yields only a non zero DC coefficient $F(1,1)$. The The 8th and 28th groups have been modulated by the vertical input signal which consists of two cycles of a sinusoid. The DFT of each of these groups yields non zero values for the 3rd and 31st Fourier coefficients in rows 7 and 27 of $F(k,\ell)$, i.e., $F(7,3)$, $F(7,31)$, $F(27,3)$, and $F(27,31)$. Figure 11b is an expanded view of the DFT of the 8th group from the CTM showing $|F(7,3)|$ and $|F(7,31)|$.

In order to conveniently demonstrate the operation of the two dimensional transform, a display circuit was employed to apply the desired signal to the Z axis of an oscilloscope. The X axis sweep was triggered by a row synchronization pulse and a frame synchronized staircase waveform was applied to the Y axis. A short pulse added to $|F(k,\ell)|$ before each coefficient output displays a two dimensional grid. Each value of $|F(k,\ell)|$ appears as a line after its corresponding grid point. Figure 12 shows the display of the input signal used in Figures 8 through 11 and its two dimensional transform. The input signal is the product of six cycles of a sinusoid in the horizontal direction and two cycles of a sinusoid in the vertical direction with a DC offset added to the product. The display of the two dimensional transform magnitude shows the DC coefficient $F(1,1)$ in the upper left corner at position (2,2) of the 32 x 32 array. The Fourier coefficient $F(7,3)$ due to the input product can be seen at position (8,4) of the array. (Remember that all outputs are shifted by one bit in both directions due to the CZT photomask error.) The three aliased outputs

F(7,31), F(27,3), and F(27,31) can
also be seen.
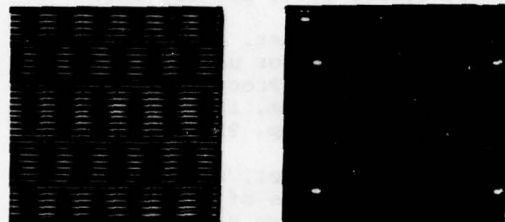
(a) Sinusoidal   (b) Output
    Inputs f(m,n) $|F(k,\ell)|$

Figure 12. Two Dimensional Display of
the DFT Output for Sinusoidal Inputs.

Figure 13 shows the operation of
the two dimensional DFT with a square
wave product input. The horizontal
input seen in Figure 13a is two cycles
of a square wave and the vertical
signal is one cycle. A DC offset has
been added. The DFT output seen in
Figure 13b clearly shows the funda-
mental and odd harmonic components
due to each input. The aliased funda-
mental from the vertical square wave
appears in the first column of the
display due to the CZT photomask error.
The DC components from the 2nd CZT
seen in column two of the display are
due to the -36 dB fixed pattern noise
in the CTM. Figure 14 shows $|F(k,\ell)|$
for k=3, i.e, the 4th row of the
display. An imbalance in the output
magnituding circuit used causes the
nonuniformity seen in the harmonics.
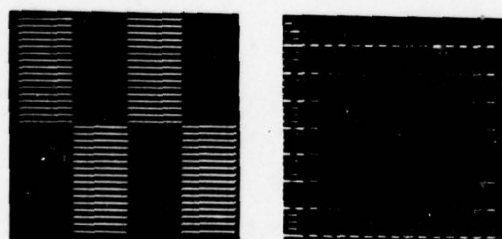
(a) Square Wave   (b) Output
    Inputs f(m,n) $|F(k,\ell)|$

Figure 13. Two Dimensional Display of
the DFT Output for Square Wave Inputs.
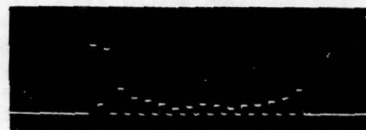
Figure 14. One Row of the DFT Output

The dynamic range of the two
dimensional transform is presently
limited by the corner turning memory
which exhibits 36 dB dynamic range
due to a fixed pattern noise component
discussed earlier. The dynamic range
of the CCD CZT IC has been demon-
strated to be 50 dB.[4] The power re-
quired for the complete two dimen-
sional transform breadboard was 10
watts. This includes all timing cir-
cuitry, external amplifiers, drivers,
MDACs, etc. Improvements to the CZT
and CTM IC and further integration
can be expected to reduce the power
requirements and increase dynamic
range.

CONCLUSIONS

Preliminary results from a two
dimensional DFT breadboard demon-
strated the potential in applying
analog CCD technology to the imple-
mentation of low power, high speed
complex two dimensional signal pro-
cessing algorithms. Although 100 kHz
is not an aggressive data rate for
CCD circuits, it results in computa-
tion of the 32 x 32 point two dimen-
sional DFT (1024 total points) in
40 msec. It is anticipated that
CCD two dimensional transforms can
be performed at clock rates of
several magahertz with a moderate
increase in system complexity.
This would result in computation
times on the order of one milli-
second.

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A COMPLEMENTARY CCD/SAW RADAR SIGNAL PROCESSOR

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ABSTRACT: In recent years the size, weight, power, and cost factors of radar equipment have escalated sharply as the result of a demand for a greatly expanded operational capability. Multimode operation, enhanced resolution, improved detection capability, etc., have increased signal processing equipments to the point that neither evolutionary improvements nor innovative circuit designs and packaging techniques may provide practical solutions for implementation. Instead, step improvements must be made by finding new technological approaches to supplement or replace the conventional means of implementing desired functions. The charge coupled device (CCD) and surface acoustic wave (SAW) device technologies offer the opportunity of making such a step improvement in the size, weight, power, and cost of a radar doppler processor.

INTRODUCTION

Based upon the realization that a radar processor concept such as that contemplated utilizing CCDs is at least five years away from field deployment, a rather aggressive set of performance parameters were postulated as summarized in Table 1. The anticipated processor application is a high resolution airborne radar system capable of both search and track modes of operation.

Modes	Search & Track
Range Resolution	15 m
Range Sampling Factor	1.25
Range Bins	1000 Search 500 Track
Doppler Resolution	64 Points
PRF	Staggered
Dynamic Range	50 dB

Table 1. Basic Radar Characteristics

ARCHITECTURAL TRADE-OFFS

In an attempt to capitalize on the attendant size, weight, and power advantages of CCD based analog signal processing for an advanced, high performance, multimode radar processor, two basic configurations were carefully evaluated as summarized in Table 2. The two approaches evaluated were the range gated CZT bank approach[1] of Figure 1 and the corner turning memory/CZT approach[2,3,4] of Figure 2. The retention of phase information necessary to perform tracking using conventional monopulse radar techniques[5] becomes a significant factor in the architectural trade-offs. This requirement is particularly significant with respect to the range gated CZT bank approach since the "sliding" CZT[6] is no longer applicable. Additionally, this approach, while performing signal storage and convolution simultaneously within the CCD, is redundant in its storage of the in-phase (I) and quadrature (Q) signal samples. Therefore, the performance of a mathematically rigorous N point CZT requires approximately 8N CCD storage locations and provides a 50% duty cycle.

The corner turning memory (CTM) configuration which is architecturally similar to the conventional digital approaches requires only 2N storage locations to perform an N point complex transform with a 50% duty cycle. Calculation of an N point transform over M range bins with 100% duty cycle using "ping-pong"

Characteristics	MAGNITUDE ONLY		MAGNITUDE AND PHASE	
	RANGE GATED CCD CZT	CCD CTM SAW CZT	RANGE GATED CCD CZT	CCD CTM SAW CZT
Range Resolution	$c/2f_R$	$c/2f_R$	$c/2f_R$	$c/2f_R$
Doppler Resolution	PRF/N	PRF/N	PRF/N	PRF/N
CCD Data Rate	PRF	f_R	PRF	f_R
Duty Cycle	100%	50%	50%	50%
CCD Storage/Range Bin	4 N	2 N	8 N	2 N
Range Bins/CCD Chips	5	32/2	5	32/2

Table 2. Comparison of the Range Gated CZT and CTM/CZT Radar Processor Architectures
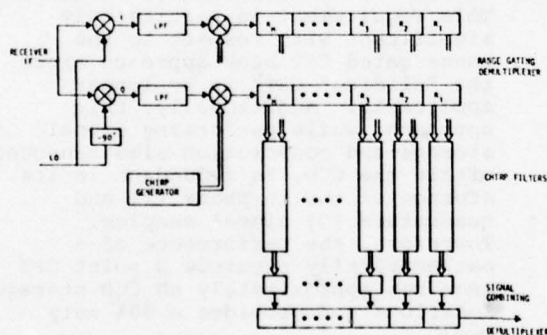
Figure 1. Range Gated Pulse Doppler Processor Utilizing the CZT.

Figure 2. Radar Processor Architecture Using CCD Memory and SAW CZT

techniques will require 16 MN storage locations for the range gated CZT approach and 4 MN locations for the CTM approach.

Either of the two approaches appears to provide adequate dynamic range. The range gated CZT processor's dynamic range is limited by the associated amplifier and/or multiplier circuitry. The wide bandwidths and attendant clock feedthrough difficulties will limit the achievable dynamic range of the CTM.

Operating speeds, power, and operational difficulties of the two approaches represent key issues which almost defy analysis. The range gated CZT architecture, which demultiplexes the signals into M parallel paths which are clocked at the PRF, provides the lowest CCD data rates. The CTM approach, in general, requires CCD data rates approximately equal to the range resolution (or sampling) rate, $f_R = c/2\delta_R$, where c is the speed of light and δ_R is the range resolution, which is normally commensurate with the radar's video bandwidth. However, the operating speed limitation in both cases is the multiplexer/demultiplexer circuitry which, due to system integration considerations, must be integrated on-chip with either processor configuration and must operate at the range sampling rate, f_R.

Power dissipation requirements based upon simple CV^2f considerations for the CCDs alone indicate the requirements for the CTM approach are 1/4 that of the range gated CZT approach if all unambiguous range bins are processed and equivalent if 1/4 of the unambiguous range bins are processed. This conclusion is based upon the clocking of 2N stages at f_R for the CTM and 8MN stages at the PRF for the range gated CZT. The power dissipation for both cases will be dominated by the clock requirements for the multiplexer/demultiplexer circuitry. Amplifier and other signal conditioning circuitry power requirements will, in all likelihood, exceed the theoretical CCD clock power requirements. Thus, based upon the system requirements outlined in Table 1, the two processor configurations are comparable in terms of power requirements.

The key considerations related to the choice of a system configuration are the cost and complexity of eventual system construction and integration. Cost is primarily influenced by the quantity and complexity of the ICs employed. Compared with the CTM, the range gated CZT IC is more complex and may be expected to exhibit a lower yield. Furthermore, due to the redundant data storage and additional circuitry components, a larger number

of range gated CCD chips will be required (a factor of 3 to 6 is anticipated), thereby increasing system complexity. Although the CTM approach requires the additional investment in the surface acoustic wave chirp transform unit,[7,8] this technology is quite mature and the cost trade-off appears reasonably favorable.

The combined CCD CTM/SAW CZT approach was, therefore, appraised as exhibiting the most promising overall cost/performance potential for the proposed high resolution, multi-mode processor, and a program to develop the required components was initiated. It should be pointed out that, for processors not requiring phase information, the range gated "sliding" CZT still represents a viable option due to its 100% duty cycle with its storage requirements of 4N samples. The remainder of this paper describes the component development and compares observed performance with design goals. In addition, preliminary results on a new CCD CTM configuration are presented.

CTM TRADE-OFFS

The CTM can be configured into N delay lines of length M or into M delay lines of length N as shown in Figures 3 and 4 respectively. In the former case, returns for sequential PRIs are loaded into sequential delay lines at the range resolution rate until all N delay lines are filled. Thus each delay line corresponds to range swath returns for a particular PRI. Locations within the delay lines correspond to range bins. The N samples from a given range bin are then sequentially read from the outputs of the delay lines at a rate commensurate with the CZT analysis bandwidth (i.e., B/N). The latter configuration loads a sample into each delay line once each PRI. Thus the contents each delay line correspond to returns from sequential PRIs for a particular range bin. The contents of each delay line must be sequentially read at a rate equal to the spectral analysis bandwidth, B, while the contents of the remaining delay lines are statically maintained.
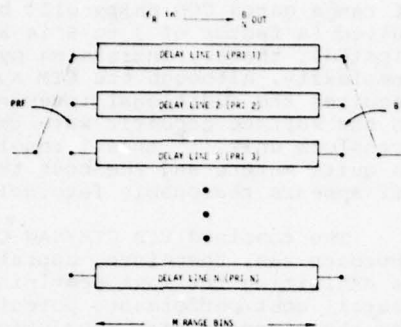
Figure 3. Serial In/Parallel Out CTM Configuration.
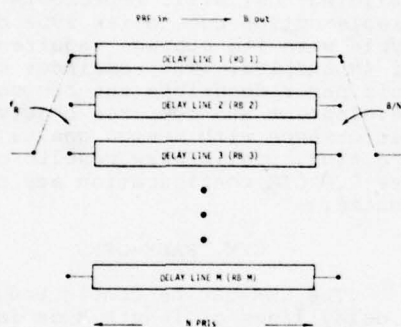
Figure 4. Parallel In/Serial Out CTM Configuration.

Therefore, the former configuration requires high speed CCD transfers for read-in while the latter requires high speed read-out transfers. Also since N is usually much less than M, CTE effects are less pronounced with the latter configuration.

Further consideration of the partitioning of the CTM indicates some potential advantages with respect to memory utilization may be accrued by partitioning the memory into square arrays. Proper design of the memory timing will permit each square array to be switched between the two configurations discussed above permitting simultaneous loading and unloading of

the array which results in 100% memory utilization. Simultaneous data loading and unloading implies equal input and output data rates which further implies that the CZT spectral analysis bandwidth, B, must be equal to the range resoluton rate, f_R. This constraint may be avoided at the cost of additional input/output buffers and/or more complicated memory timing considerations.

An attractive alternative to the line addressable memory concept for implementation of the CTM is the two dimensional charge transfer structure[9] to be discussed in detail in a later section. The complexity of the design was considered to be a significant risk factor for this development and has been pursued under a separate program.[10]

CCD CTM IMPLEMENTATION

Based on the previously discussed architectural considerations, a processor brassboard has been developed based on the configuration illustrated in Figure 2. The I and Q components of the radar video are to be derived from a synchronous detector in the radar receiver and stored in separate memory (range store) modules. Each module consists of a number of 66x66 cell CCD memory blocks required to accommodate the range swath of interest. For the brassboard, two blocks per module were employed, although this is expandable to allow the desired coverage of the radar pulse interval. Thus the range stores in the brassboard can accommodate 132 range bins (I and Q) collected over 66 PRIs in the search mode and 66 range bins (I and Q for both Σ and Δ channels) over 66 PRIs in the track mode.

The range stores are emptied at a 12.5 MHz rate into I and Q up converters to generate single sideband doppler information at a 318 MHz IF for subsequent spectral analysis by the 64 point SAW CZT module. (The use of 66 cells in the range stores allows 2 "burn-pulses" for settling of transients before spectral analysis is initiated). The SAW CZT module

consists of two complex CZT channels which are commutated by processor timing to allow continuous system operation. The use of the complex CZT realization is required to maintain the desired phase information.

The organization of the CCD memory chip is illustrated by the block diagram in Figure 5. The configuration shown consists of sixty-six 66-stage CCD delay lines and the circuitry required to address individual input and output terminals on a line-by-line basis. The corner turning operation is performed by sequentially switching between a parallel mode in which consecutive samples are read into and out of consecutive delay lines, and a serial mode in which consecutive samples are read into or out of one particular delay line.
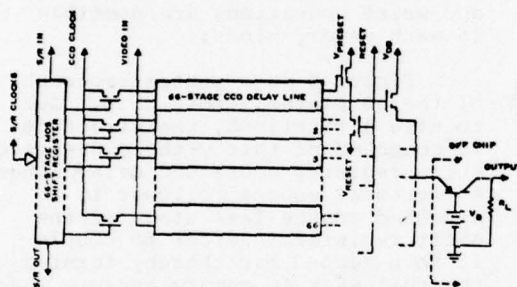
Figure 5. Block Diagram of Sequentially Line Addressable Memory Chip.

The design approach used in the range stores is based on the two phase CCD structure which can be realized with the double level polysilicon gate process developed at TI. These delay lines are operated in the so-called "phase and one-half" mode in which one set of gate electrodes is clocked while the other is maintained at an intermediate DC level. By properly designing the output circuit, the charge transfer and sensing operations can be controlled with a single clock pulse. When the CCD clock is off, the signal charge is stored in ion implanted potential wells beneath the non-clocked electrodes.

The efficacy of this structure is that it makes it possible to manipulate the data samples in the memory by enabling a single clock signal to the desired CCD delay line. All the delay line input terminals and output terminals can respectively be connected in parallel since charge is transferred into or out of a particular delay line only if its clock is enabled. Since the addressing required for the corner turning operation is always sequential (i.e., line m + 1 is always addressed after line m, unless a reset to m = 1 is required) the addressing function is implemented using a digital shift register operating synchronously with the CCD clock rather than the address decoder circuits typical in random access designs.[11] Thus, the memory is not randomly line addressable, but rather is referred to as "sequentially line addressable."

In the parallel mode the shift register clock operates at the same rate as the CCD clock with a logic "1" entered at the shift register input at the start of each radar pulse interval. In the serial mode, the shift register clocks operate at 1/66 the CCD clock rate with a single "1" entered at the start of the serial cycle. Thus the digital shift register must be capable of operating at the maximum data rate required of the memory and must also be able to retain a logic "1" in each cell for a large number of clock periods in the serial mode. Further, it is necessary to interface some type of switch to the shift register structure in order to enable the CCD clock line. All of these requirements are met with a dynamic MOS digital shift register which is implemented on chip with the CCD delay lines.

Referring to Figure 5, a logic "1" is entered at the input of the 66 stage MOS shift register and propagates through the structure sequentially addressing MOS switch transistors which couple individual CCD clock lines to the CCD clock busses. Serial or parallel oper-

ation is determined by the shift register clock rate. Signal charge is transferred down the CCD delay lines and detected at individual output circuits which include an additional reset switch whose operation will be described later. The commutating shift register is a standard dynamic MOS ratio-less configuration with an additional transfer switch connected to the CCD clock switch transistor which operates in a bootstrap mode.

The CCD delay lines are each 66 stage buried channel devices having 6 mil (152.4 µm) channel widths and 0.6 mil (15.24 µm) gate lengths. The input circuits are dual gate surface channel configurations and can be operated in either the "diode cutoff" or "potential equilibration" mode. The buried channel is coincident with the edge of the implanted well under the first clocked electrode.

In order to preserve dynamic range at the clock rates required, it was determined that each delay line should have an individual source follower output transistor. Furthermore, power dissipation requirements dictated that each output transistor should be turned off when not in use. This was accomplished with an additional reset transistor at the output of each delay line and the use of external current summing in the output circuit. As indicated in Figure 5, all output nodes are tied in parallel and connected to the emitter of a PNP common base current summing amplifier. The value of V_B sets the voltage at the emitter and hence the common output node voltage. This is adjusted such that the preset level at the output diode of the currently addressed delay line is sufficient to turn on its respective source follower.

The collector current of the summing amplifier then follows the drain current of the output follower and is sensed by R_L. Coincident with the operation of the shift register, a reset pulse is applied to the gate of the additional reset transistor. This pulls the output diode voltage at all delay lines down to V_{reset} which is adjusted to

a level below the emitter voltage of the summing amplifier ($V_{reset} = V_B$ is sufficient) thereby turning off all output source followers. The next preset operation turns on the output circuit of the next delay line, and the output voltage follows the source follower drain current until the next reset pulse occurs.

This output scheme results in an excessive fixed pattern noise component observed during the parallel mode due to threshold voltage variations among the individual output circuits. In the serial mode, however, it results in DC level shifts between consecutive output data sequences which may be removed by subsequent filtering. Consequently, only the serial mode output can be utilized, and two units are multiplexed such that simultaneous read and write operations are possible in each memory block.

Figure 6 is a photomicrograph of the completed memory chip. Due to size limitations, the structure is composed of thirty-three 66-stage shift register addressed delay lines. An integral source follower is attached to the last stage of the shift register in order to couple it to a second bar thereby forming the full 66 x 66 memory array. The dimensions of the chip are 156 mils by 293 mils (3.96 mm x 7.44 mm).
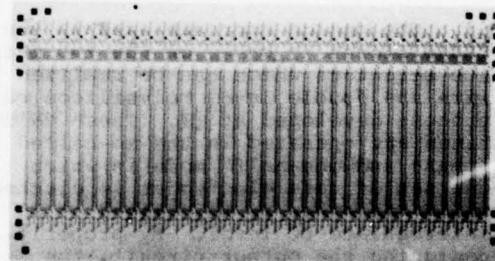
Figure 6. Sequentially Line Addressable Memory Chip.

Figure 7 illustrates the operation of two interconnected memory chips performing time compression of an analog test signal at a 12.5 MHz clock rate. The top two traces are, respectively, the test signal and memory output (before sample and hold) on the same time scale. The test signal is sampled during the parallel mode which can be differentiated from the serial mode by level variations in the latter due to threshold voltage variations.
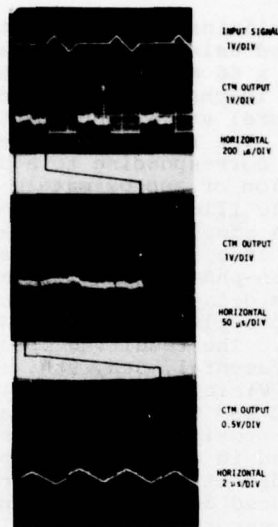
Figure 7. Sequentially Line Addressable CTM Operation at 12.5 MHz

Due to the organization of the memory it is not possible to make direct measurements of charge transfer efficiency (CTE) and dynamic range of the CCD delay lines. Instead, a separate CCD test structure was included on the chip in order to make meaningful measurements. Using this test structure the CTE was found to be 0.999 with the dynamic range in excess of 50 dB.

Clock waveforms for the commutating shift register and CCD delay

lines were generated with standard Schottky TTL logic elements. The required clock drive levels were obtained with discrete clock drivers using medium power VHF transistors. Each 66 x 66 memory block (4 chips) dissipates approximately 15 watts, of which 12 watts are dissipated in the clock drivers with the remainder in various amplifier, switching, and control circuits.

SAW CHIRP Z TRANSFORM

The SAW CZT module utilizes a dual channel 64 point chirp Z transform to process the doppler information. A block diagram of the SAW CZT module is shown in Figure 8. In operation the in-phase and quadrature baseband doppler signals from the range stores are mixed with appropriately phased 318.75 MHz carriers to produce an IF signal that can be accommodated by the transform processor. The two channels of the processor are multiplexed in such a manner as to provide continuous processing, in 5.12 s time segments, of the time compressed and up converted video.
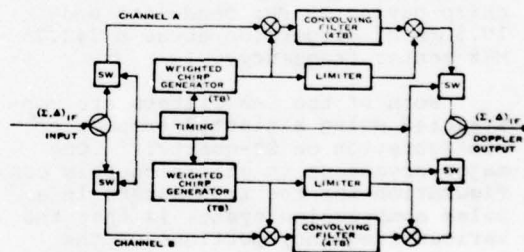
Figure 8. SAW CZT Module Block Diagram.

Operation of the SAW CZT is conveniently described by the frequency-time diagram shown in Figure 9. As a 5.12 μs data burst is switched into one channel, it is mixed with a synchronized linear FM down chirp having a 12.5 MHz bandwidth and 5.12 μs of dispersion about a center frequency of 175 MHz and weighted with a Dolph-Chebyshev function.
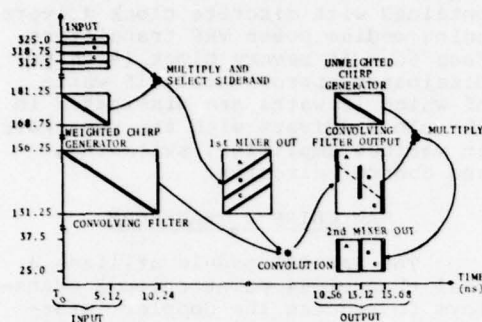
Figure 9. Frequency Versus Time Operation of CZT.

Note that the mixer output must be linear with respect to either input over a dynamic range which is the sum (in dB) of the dynamic range of the input signal and that of the weighting function. The lower sideband mixer product has a chirp sense opposite that of the premultiply chirp and is applied to the input of the compression filter which is a down chirp having 25 MHz bandwidth and 10.5 μs of dispersion about a 143.75 MHz center frequency.

Both of the SAW filters are constructed using a slanted transducer configuration on ST-quartz.[12] One major advantage in utilizing this configuration for the transducers in a pulse compression system is that the various frequency portions of the transducer are spatially separated and can be amplitude and phase compensated to minimize time sidelobes.

The compressed pulse output from the compression filter is then post multiplied with the chirp from the premultiply filter that has had the weighting removed by limiting. This process is facilitated by including a proper amount of flat delay in the compresson filter so that the filter output aligns with the synchronous post multiply chirp to produce a fixed output frequency of 31.25 MHz from the post multiplier.

The SAW CZT module exhibits in excess of 60 dB dynamic range (peak signal to noise floor) with a power dissipation of 16 watts. It appears possible to achieve 80 dB dynamic range with an optimized design. Sidelobe levels fall below 40 dB at frequencies two to three doppler bins removed from an analyzed signal. The nearer sidelobes were only suppressed 26-30 dB due to pattern generator difficulties.

SYSTEM TEST RESULTS

Preliminary system tests were performed using a partial range store (one 66 x 66 memory block, half used for the in-phase channel and half for quadrature) and a complete SAW CZT module. The repetition interval was 5.28 μs corresponding to a doppler resolution of approximately 3 kHz. Figure 10 illustrates the response due to a complex input signal consisting of a 6 kHz square wave applied to the in-phase channel with a similar waveform delayed by + one quarter of a period applied to the quadrature channel. The resulting spectra with the fundamental, 5th, 9th, and 13th (barely visible) harmonics in one sideband and the 3rd, 7th, and 11th in the opposite sideband are clearly indicated in the oscillographs. The amplitudes of the higher harmonics are reduced due to the low pass filter response of the sample and hold circuit following the range stores.

Figure 11 illustrates 40 dB dynamic range achieved in the initial tests. The top trace is the response to an 18 kHz sine wave (single sideband) with an amplitude of approximately 1 volt peak to peak, while the bottom trace is the response on a more sensitive scale after 40 dB of attenuation was added in each channel. The signal is still visible (vis. detectable) above the noise floor.

System tests using a more complete range store (132 I, 132 Q, fully buffered) have proven moderately successful. The primary operational problems were the expected system related difficulties associated with circuit board layout and shielding.

(a)

(b)

Figure 10. Response of CTM Chip and SAW CZT to complex Square Wave Input (f = 6 kHz) with Fundamental in (a) Lower Sideband and (b) Upper Sideband.

S_{MAX}

$S_{MAX}-40$ dB
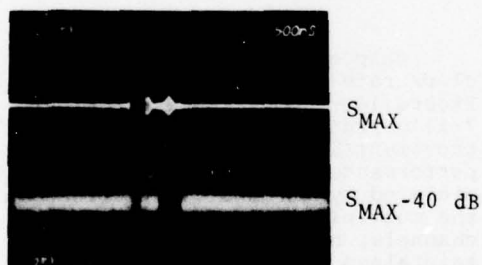
Figure 11. Response of CTM Chip and SAW CZT to a 40 dB Change in Input Level.

Additional problem areas were related to distribution and buffering of critical waveforms to minimize both noise and waveform variations due to changes in buss loading. Solutions to these problems have been identified and will be incorporated in future designs.

The primary problem area related to the chip design resulted from gain variations between I and Q channels which are related, through the trans-conductance (g_m) of the individual output transistors, to MOS device threshold voltage variations mentioned earlier. In order to suppress the unwanted sideband in the SSB up conversion process by greater than 50 dB (the system dynamic range), the gains through the I and Q channels must be nearly identical. The unwanted sideband is suppressed by $20 \log [(G_I+G_Q)/(G_I-G_Q)]$ where G_I and G_Q are gains through the I and Q channels, respectively. To achieve 50 dB suppression of the unwanted sideband, G_I and G_Q must be within ± 0.63 percent of their nominal value (± 0.06 dB variation). The achievement of the desired unwanted sideband suppression will require a redesign of the line addressable memory input/output circuitry. The two dimensional CTM discussed in the following section exhibits inherently better performance in this area.

TWO DIMENSIONAL CHARGE TRANSFER CTM

Since the "corner turning" operation can be visualized as loading a square memory array in a row-by-row fashion, then reading it column-by-column, the most direct realization involves a memory structure in which charge can be transferred either vertically (row-by-row) or horizontally (column-by-column).[8] Cell structures controlling the two dimensional charge transfer operation are complicated, and the potential advantage of a direct realization is lost in the higher risks associated with such a sophisticated design. The potential advantage of the two dimensional transfer memory is substantially improved with the addition of CCD multiplexers and demultiplexers to perform serial/parallel conversions

at the input/output ports. The resulting CCD structure has a single voltage-charge conversion at the input and a single charge-voltage conversion at the output thereby eliminating path dependent threshold voltage variations which proved troublesome in the line addressable approach.

A block diagram illustrating the operation of this two dimensional CCD memory appears in Figure 12. The input demultiplexer performs a serial/parallel conversion and loads the memory array row-by-row. During the load cycle charge is transferred vertically in the memory array. When all rows have been loaded, the array is switched to a horizontal transfer mode and the output multiplexer performs the required parallel/serial conversion of data stored in each column.
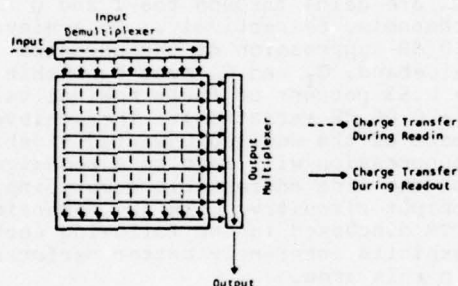
Figure 12. Operation of Two Dimensional Charge Transfer Corner Turning Memory.

Of course, as discussed previously, an additional demultiplexer can be added at the left of the memory array, and an additional multiplexer added at the bottom to permit 100% memory utilization (i.e., simultaneous load and unload).

A 32 x 32 element CCD memory based on this architecture has been designed and fabricated using the same process utilized for the line addressable CTM IC. The memory array is composed of 1024 three-phase two dimensional charge transfer cells placed on 2 mil centers.

It operates as two interleaved two-phase structures with one common phase. The multiplexers and demultiplexers are four phase structures in order to match the pitch of the memory array and maintain short transfer lengths for good CTE. The structure is buried channel, with the exception of the demultiplexer input circuitry. A photomicrograph of the completed chip appears in Figure 13.
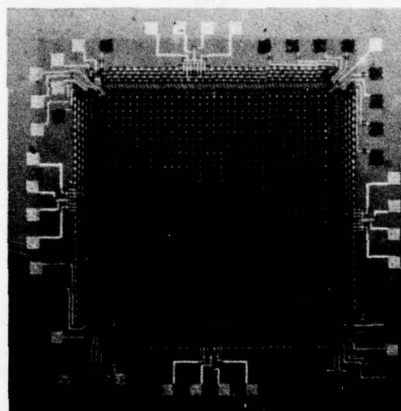
Figure 13. 32 x 32 Two Dimensional Charge Transfer Corner Turning Memory Chip.

Chip operation at a 600 kHz clock rate is demonstrated in Figure 14. Comparison with Figure 7 illustrates the dramatic improvement in fixed pattern noise performance. Dynamic range is still dictated by threshold variations in the multiplexer and demultiplexer channels, however, nearly 40 dB is maintained across an entire frame as compared to less than 20 dB observed in the best case for the line addressable CTM.

The two dimensional charge transfer CTM has been operated with data rates in excess of 5 MHz, although dynamic range is degraded due to capacitive coupling of the memory array clock pulses into the output circuit. The data rate employed in
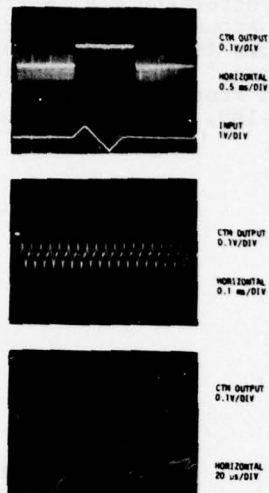
Figure 14. Two Dimensional CTM Operation at 600 kHz.

Figure 14 is due to the frequency limitation in an external circuit used to suppress this noise component. It is anticipated that the clock feed-through problem can be remedied in future designs. The two dimensional structure has the potential for higher data rates than the line-addressable approach since the input demultiplexer function is realized with a high speed CCD structure, rather than with an MOS shift register.

Since each cell in the memory array is bounded in two dimensions, maximum charge capacity is limited to less than 1/3 that available in the line addressable design. As a result the two dimensional structure offers higher density at the possible expense of dynamic range due to comparable thermodynamic noise sources in both designs.

Although the two dimensional CTM requires a substantially larger number of clock waveforms as compared to the line addressable CTM, only the transfer gates which interface

the multiplexer and demultiplexer to the memory array require precise control by system timing. The memory array clocks operate at 1/N times the data rate and are conveniently driven by standard TTL-MOS drivers at even the most ambitious data rates. The multiplexer and demultiplexer clocks run continuously and are eminently suited to resonant driver techniques at high data rates.

CONCLUSIONS

The CCD CTM/SAW CZT approach to radar signal processing provides an attractive option for improving resolution capabilities over the next few years without tremendous size, weight, and power disadvantages. SAW technology can readily provide increased throughput rates. Technological development in high speed CCD design and applications areas currently underway at many device research laboratories are expected to be key to resolution capabilities of this approach.

ACKNOWLEDGEMENT

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DEVELOPMENTS IN RADAR DOPPLER PROCESSING

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The capability of performing wideband spectrum analysis in real time using surface acoustic wave (SAW) chirp filters presents an opportunity to apply a single spectrum analyser to multiple channels of low bandwidth data using time-compression. This technique is particularly appropriate to pulse doppler radar in which each range gate presents a separate sampled data time series for analysis. Given the SAW spectrum analyser, the radar signal processing problem centres on the store used to acquire the sampled video, re-order it into time sequences from each range gate and output it in a highly compressed time scale. This "corner turning" store has been realized in both digital and CCD forms. The digital store has been built in two versions, one, for low bandwidth, is inexpensive but relatively slow, the second, for high bandwidth radars, is both expensive and power consuming. A new integrated CCD store has been designed to solve these problems, incorporating a new mode of clocking, using novel clock drivers and minimizing external pin connections. Results from all these configurations, in which both real and simulated radar data are analysed, are given. Conclusions on their relative merits in terms of real world constraints such as power consumption, size, complexity and clutter levels are drawn.

1 Introduction

We have previously[1,2] discussed approaches to the problem of processing pulse doppler radar signals. The basis of these has been to accumulate samples of radar video, either in a CCD analogue store or in digital RAM, to re-order the samples into time sequences from individual range bins, and to serially output these sequences into a spectrum analyser serving all range bins. The commercial availability of fast spectrum analysers using surface acoustic wave (SAW) filters now readily allows this type of multiple channel, compressed-time spectrum analysis. The problem is thus reduced to the implementation of a flexible store capable of accepting samples at rates dictated by the radar parameters [pulse repetition frequency (prf) and range bin spacing] and outputting them in bursts matched to the time scale of the SAW analyser. This paper compares digital and analogue CCD implementations of the storage function aimed towards providing modules adaptable to a variety of radar requirements using a standard SAW analyser and describes in some detail a new CCD under development for this.

2 The SAW Spectrum Analyser

The number of resolvable doppler frequencies or time-bandwidth product of the coherent processing, is limited to the number of pulse echoes available from the radar targets. This is a function of prf, beamwidth and scan rate for a scanning radar, and the number of pulses per beamwidth rarely exceeds 100. Because of this we have used an analyser of nominal time-bandwidth product (TB) 100, it being a simple matter to under-use its capability for radars with a smaller number of hits on target. TB products exceeding 100 are obtainable by relaxing the $\pm$ 0.5dB flat response requirement. The actual SAW time and bandwidth parameters are of only secondary importance because T and B scale inversely under time compression, the product being invariant. For our analyser, T = 25 μs and B = 4 MHz. The SAW filters used of course operate at IF frequencies in the 20 to 30 MHz range but by internal single-sideband mixing the

analyser covers the band ± 2 MHz when presented with a dual channel, I and Q (in-phase and quadrature) baseband input. Time weighting is included to suppress spectral sidelobes to approximately -35dB whilst the overall dynamic range is about 40dB. This is sufficient for some radar situations but in cases where the clutter signal ratio exceeds these parameters, some pre-filtering will be necessary to reduce the dynamic range of the radar video.

3 Digital Storage

The digital store has 3 dimensions: the number of range cells x the number of pulses coherently processed x the data word length. For the 40dB dynamic range analyser, 8 bit words are sufficient and the re-ordering, or "corner turning" function is accomplished by appropriate input and output addressing of RAM under the control of range cell and pulse counters. The use of digital storage implies the use of A/D and D/A converters at the input and output (the SAW analyser being analogue) and when approaching and receding velocities are to be distinguished both I and Q channels must be stored.

Two versions of the digital store have been constructed to match differing system requirements. The first is appropriate to a relatively high resolution in range and doppler utilising the full TB capability of the SAW spectrum analyser. The range cell spacing of 22m specifies a range counter running at 7.5 MHz on 'write' while during 'read', 128 samples are output at 5.12 MHz. TTL control logic and fast NMOS RAM is therefore used together with bulky and power consuming A/D converters. For a 16-range cell system, 40W is consumed excluding the SAW analyser. The time compression factor of ~10³ would allow several hundred range cells to be added before a second spectrum analyser became necessary. Figures 1 and 2 illustrate some on-line range-doppler displays photographed with this processor used with a meteorological research radar.

A second store has been built for a radar of lower range resolution and fewer hits on target. This used 16 ranges x 32 pulses x 8 bits, I channel only, with a range counter running at only 200 kHz. This allowed CMOS control circuits and RAM to be used together with compact low-power A/D converters consuming only 3W in total.
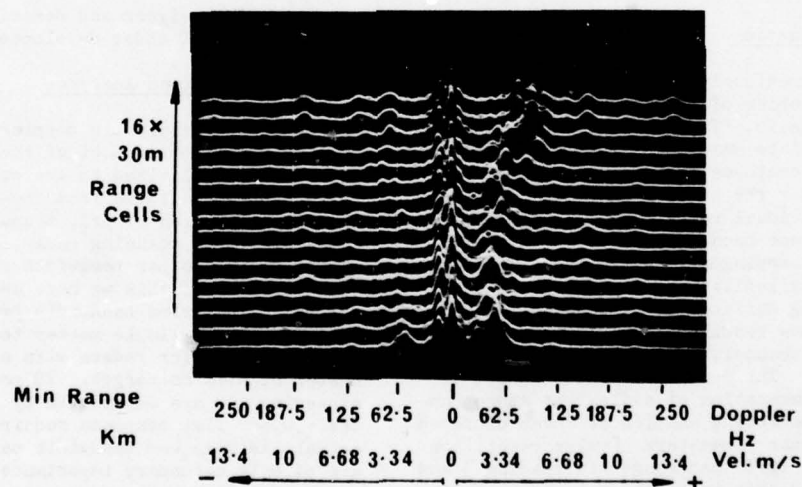
Figure 1 Range Doppler Display from metrological radar showing wind shear versus height/range.

16 × 30m Range Cells

Min Range Km

| 250 | 187·5 | 125 | 62·5 | 0 | 62·5 | 125 | 187·5 | 250 | Doppler Hz |

| 13·4 | 10 | 6·68 | 3·34 | 0 | 3·34 | 6·68 | 10 | 13·4 | Vel. m/s |
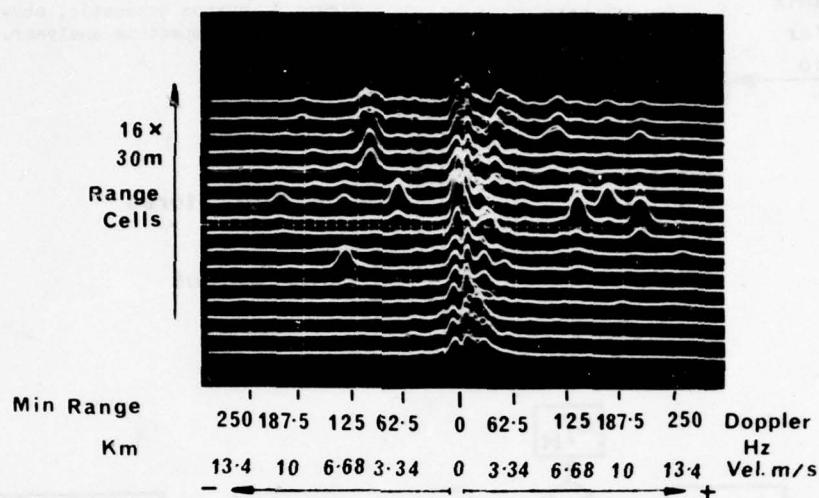
Figure 2 Similar display showing birds/insects.

4 CCD Storage

The object in designing a CCD store is to produce a module structured to meet the radar problem but capable of adaptation to a wide range of radar parameters. A/D interconversions are avoided, an increasingly valuable feature for higher bandwidth radars. The number of range cells handled by the store module is a convenience factor only, dictating the number of modules needed in particular applications, whereas the pulse storage capacity should, like the spectrum analyser, match the highest TB product likely to be needed, eg 100, and the dynamic range should also at least equal that of the analyser.

Our first experimental CCD store was configured from discrete, already available devices: a 32-sample tapped delay line sampling the radar video in 32 range bins of 4 MHz following each pulse. 16 of the tap outputs were connected to each feed an orthogonal 100-sample linear CCD register clocked once per radar pulse to form I-channel time sequences from each selected range. These range bin stores were filled at a clock rate of 4 kHz (the simulated prf) and, when full, individually emptied at a 4 MHz rate to feed the SAW analyser. The layout of this system is sketched in

Fig 3 and Fig 4 shows time-compressed ($\times 10^3$) waveforms and spectral outputs. This exploratory system of 16 range bins occupied a 30 x 35cm board and confirmed the expected difficulties in matching CCD gains and levels which would be multiplied for systems processing many range cells. However it allowed flexible control of the clock waveforms, for instance, to interleave the input and output functions to minimise the hold time when the signal is most liable to corruption by dark current, and established the feasibility of the CCD approach.

To implement these functions onto one chip requires (1) a register which takes in the radar data at a rate of 4 MHz (2) a sideways transfer structure which operates at $\leqslant 1/R$ of this rate where R is the number of range cells (3) a storage section implemented in the same fashion as the slow transfer part of an SPS structure and (4) a means of reading out each of the parallel channels individually and independently at a rate of 4 MHz, with a minimum of external peripheral circuitry.

The serial to parallel structure of an SPS array achieves (1) to (3) of these requirements, but in these structures the data cannot be read out of the parallel channels independently. We have adapted this type of structure into a new type of storage module. In our structure the phases 1 and 3 clocks in the parallel section of the

Figure 3 System Schematic, showing store and spectrum analyser.

0-2MHz Bipolar Video

4MHz

4kHz Input

Range Cell Stores

4MHz Output

S/H

Chirp 1
25µs, 2MHz
Generator

Chirp 2
50µs, 4MHz
Convolver

Det & Threshold
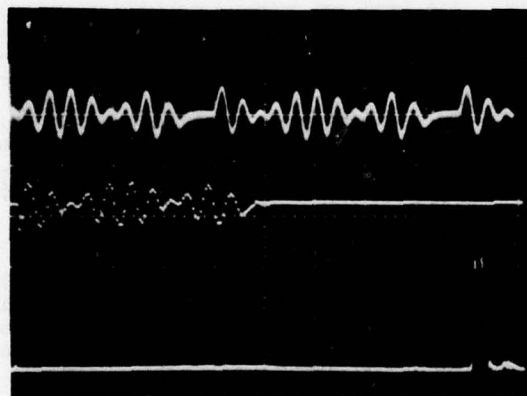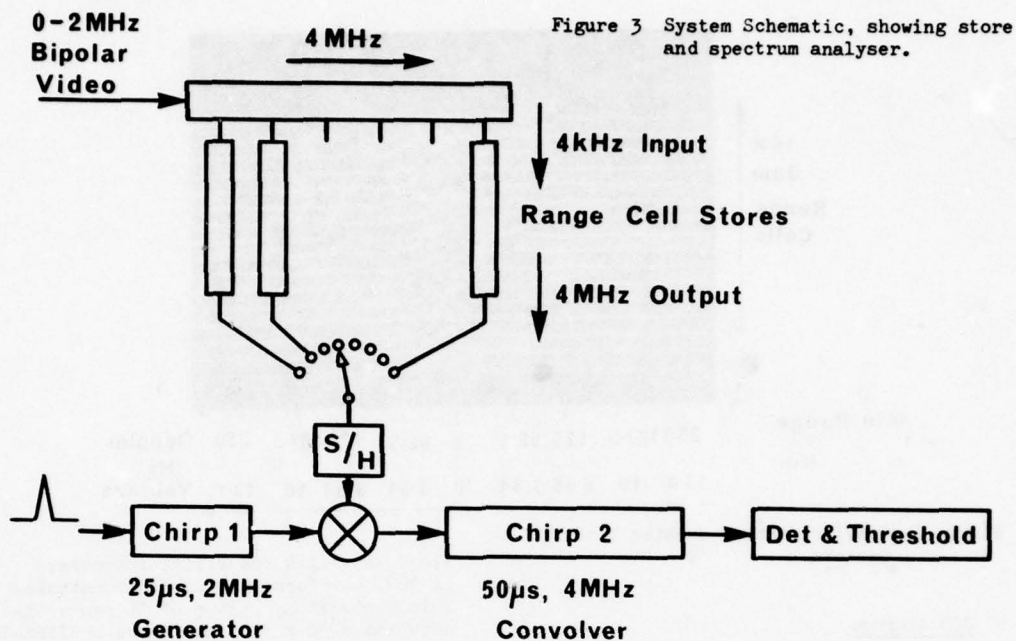
Top trace: video, 5ms/div containing 400 Hz and
             500 Hz components

Middle trace: time compressed video, 5µs/div

Lower trace: spectrum output 5µs/div or 800Hz/div

Figure 4

array (ϕ_{1p}, ϕ_{2p}) Fig 5 are common to all the parallel sections. The phase 2 clocks (ϕ_{2np}) are brought out individually to pads around the chip periphery. In contrast to an SPS structure, an output transfer gate common to all parallel channels feeds all channels into a common output amplifier. Fig 6 is a chip photograph, of a 16 x 128 bit version.

The input to this device operates in a conventional way, whereby the parallel clocks ϕ_{np} are clocked with the input register clocks ϕ_{nS} to fill the array with data, the parallel clocks operating once each time the serial register is filled by R input clock cycles, corresponding to R range gates.
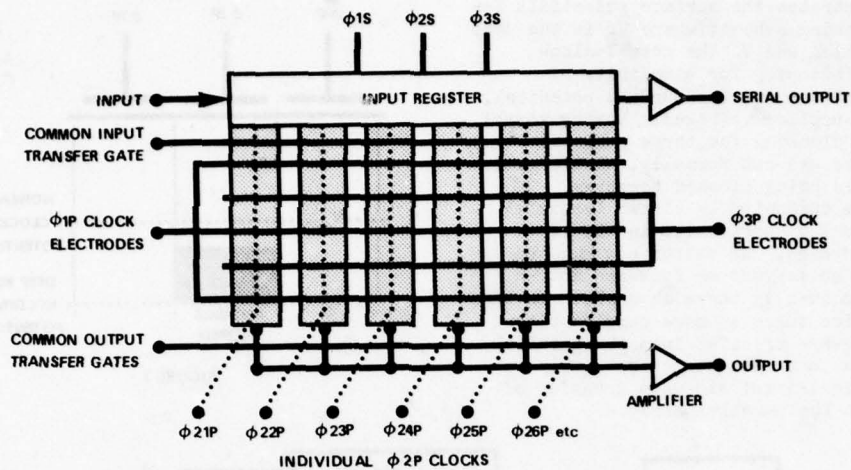
FIGURE 5

After P clock cycles, where P is the number of pulses to be analysed, the array is full of data. At this point the logic system associated with the parallel clocks switches the clocks to a new mode of operation. All parallel clock electrodes, save one, are driven to a high potential, up to twice the parallel clock swing. In the deep wells so formed, the charge held under every phase 2 electrode remains under these electrodes independent of the state of the phase 1 and 3 clocks. The desired range channel is clocked normally, together with the ϕ_{1p} and ϕ_{3p} clocks to read that channel out independently to the common output circuit, at 4 MHz, and so to the SAW analyser. The phase 2 clocks are then switched one by one in sequence to normal clocking, while all the others are held high. Thus the individual range cells are read at high speed in sequence to the SAW analyser.
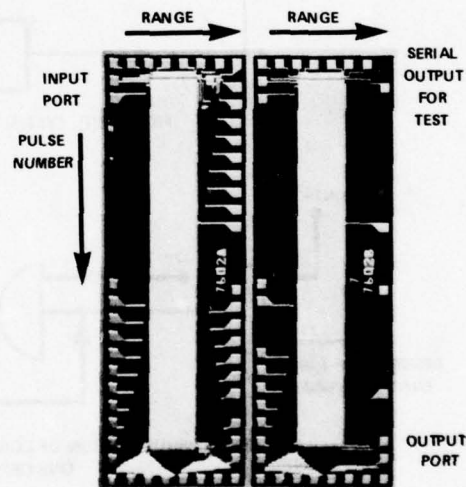
ACTUAL CHIP PHOTOGRAPH OF
16 RANGE x 128 PULSE CHIP IN
TWO VERSIONS
  (a) WITH AMPLIFIERS
  (b) WITHOUT AMPLIFIERS

FIGURE 6

Fig 7 illustrates the surface potentials for such a clocking scheme, where V_D is the deep well potential and V_C the normal clock potential (assuming for simplicity of explanation that ϕ_S, the surface potential, equals the applied voltage). During normal slow input clocking the three parallel phase clocks are run normally, all individual channels being clocked together. On readout one channel only clocks (rapidly) in the normal manner, while in the rest ϕ_{2p} is held high. No matter how ϕ_{1p} and ϕ_{3p} behave no forward or backward motion of charge occurs in these channels. In the actual device there is more complex timing of the sideways transfer into the parallel channel than has been suggested simply to ensure rapid initial sideways transfer of charge into the parallel array.
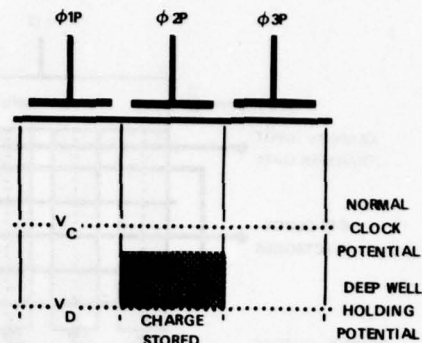
FIGURE 7
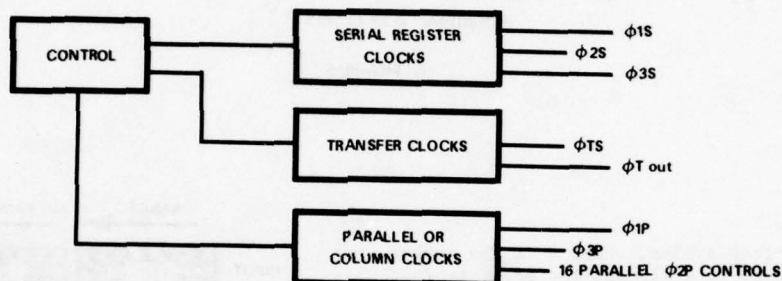
FIGURE 8(i) SYSTEM CONTROL
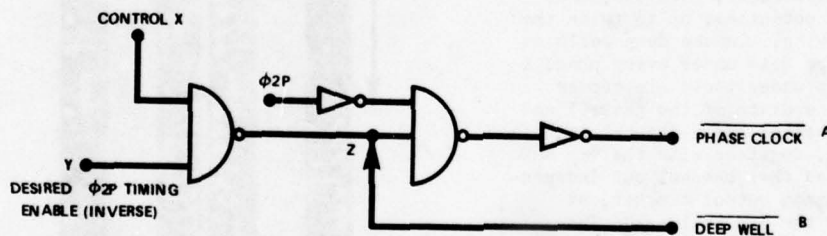
FIGURE 8(ii) SECTION OF LOGIC CONTROLLING
ONE DRIVER

In order to drive and time the store in this way, appropriate novel three level clocks had to be designed and these are described in the next section.

5 System Control Logic

The control logic for the system is presently implemented in TTL using approx-imately 20 chips. It could currently be implemented in a ULA package or, indeed, designed directly onto the same chip as the drivers; packaging the whole with the CCD in a hybrid. Ultimately it could all be implemented on a single chip.
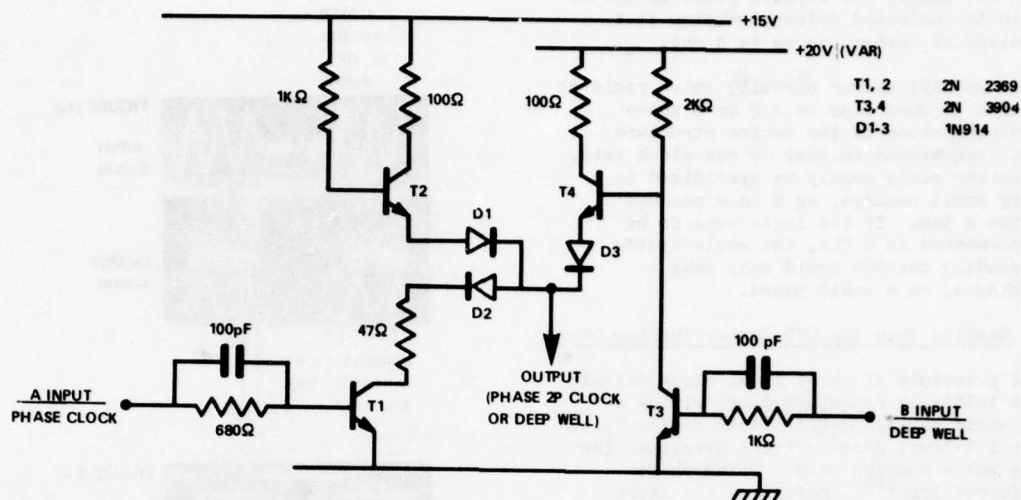
FIGURE 8(iii)   DRIVER CIRCUIT

The basic control system is shown in Fig 8 wherein the serial register clocks, the transfer clocks and the parallel or column clocks are timed to read in data at a rate matched to the radar output, and to read out the data from each channel in sequence, at high speed, to the SAW spectrum analyser. The basic system timing can be arranged to either (i) read in data into the store until it is full, then read out each channel sequentially to the analyser or (ii) with a minor reconfiguration read out one or more channels between each radar return. This obviates a duplicate store operating in 'ping-pong' and minimises dark current effects. In addition (iii) since the read-in and read-out of data are separately controllable, and the chip configuration so arranged, having a transfer gate between the serial input register and the storage/read-out section, both the acquisition of data and the read-out from any channel or channels, can take place simultaneously without interference. Thus the chip itself and the control logic and driver system form a versatile module which can be used with various timing configurations to suit the radar system in use.

6   The Special 3-Level Clock Driver Circuit and its Operation

The driver circuit (Fig 8 (iii)) is controlled by TTL level signals. The circuit gives out 15 volt clock waveforms or variable (typically 20 volt) deep well pulses according to the control signals from the control circuit 8(ii). The choice of deep level pulse amplitude is a compromise between signal handling and low dark current. These circuits have to drive the CCD store in one of two modes, (a) slow accumulation of data or (b) rapid read-out of one channel at a time. During (a) the control line X is asserted low, giving high output at Z. This causes the final output A to be asserted, which in turn gives a normally clocked output from the driver circuit (iii). This occurs simultaneously on all 16 driver circuits so that the store accumulates data. When the store is full condition (b) is invoked. On 15 channels at any given time output Z, which goes directly to input B of the driver circuit, gives a deep holding well on all 15 channels. On the sixteenth channel, selected by the logic pulse applied to input y, provided the input X is also

enabled by the general read-out system control pulse, the circuit gives an output A to the selected driver, causing that individual channel to be read out.

This special driver circuit, which could of course be used also in a 2 or 4 phase implementation of the device structure, has been tested to over 10 MHz clock rate. A number could easily be hybridized in a very small package, eg 8 in a package 2.5cm x 5cm. If the logic were to be implemented in a ULA, the whole system including the CCD would only take 4 packages, on a small board.

7 Results From the CCD Corner Turning Store

The principle of three level clock driving was initially established by driving a separate normal 32-bit linear device by the novel 3-level clock drivers developed for the pulse doppler chip. Using phase referred input[4] (referring the input diode to ϕ_1) requiring no extra 'fill and spill' pulses and automatically sampling at the correct time periods, together with the clocking scheme described above, the output shown in Fig 9 was obtained, the ϕ_2 clock being held high at $DC \approx 30\%$ above V_C for several milliseconds in this case. The phase 1 and 3 clocks were clocked at 1 MHz continuously, and the phase 2 clocks at 1 MHz when not at the deep well holding value.

In each output burst the first section of the data has been held in the device by the high ϕ_2 clock, held high during the 2 mSec period between outputs, with ϕ_1 and ϕ_3 running continuously. The second output portion of each burst was the normal output from the device, appearing 32 bits after the re-starting of the normal ϕ_2 running period. In a large store of course, the high clock storage period needs to be much greater, typically

16 BURSTS OF OUTPUT SIGNAL AT 1.0 MHz CLOCK RATE

INPUT SIGNAL 1 KHz REPETITIVE

FIGURE 10

STORED PORTION OF INPUT

FIGURE 9(i)

INPUT SIGNAL

OUTPUT SIGNAL

DIRECTLY CLOCKED SIGNAL

STORAGE TIME

STORED SIGNAL

FIGURE 9(ii)

ϕ_2

ϕ_1
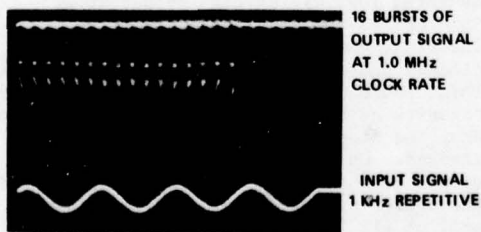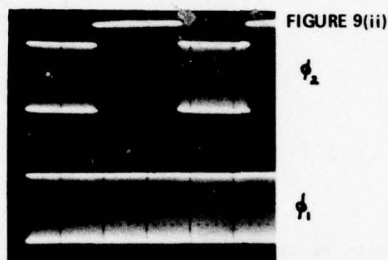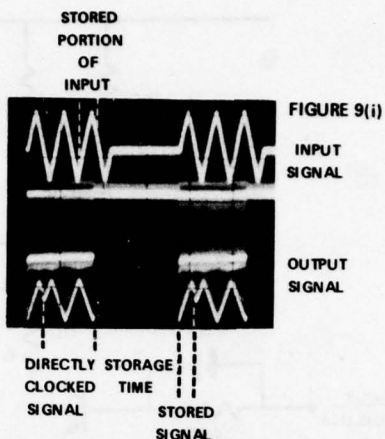
25-50 mSec, but still well within the dark current capabilities of this device.

Operation of a 16 range-cell by 32 pulse corner-turning processor of the type described earlier and shown in Figs 5 and 6 may most easily be illustrated by the input of repeated bursts of 1 kHz sine-wave data simulating a radar doppler signal at 1 kHz in every range cell, as shown in Fig 10. In this mode of operation read-in and read-out of data take place simultaneously. Read-in is at approximately 1 MHz. Fig 10 also illustrates how a dark current problem may show up - the 16th output channel of this particular device suffers from excessive dark current accumulation during the 20 mSec high-clock storage period before read-out, showing up as an excessively high output signal. In this figure the input and output signals are illustrated to the same timescale. Parallel transfer is at 4 kHz and read out at 1 MHz.

CHANNEL 1
OUTPUT

CHANNEL 6
OUTPUT

CHANNEL 9
OUTPUT
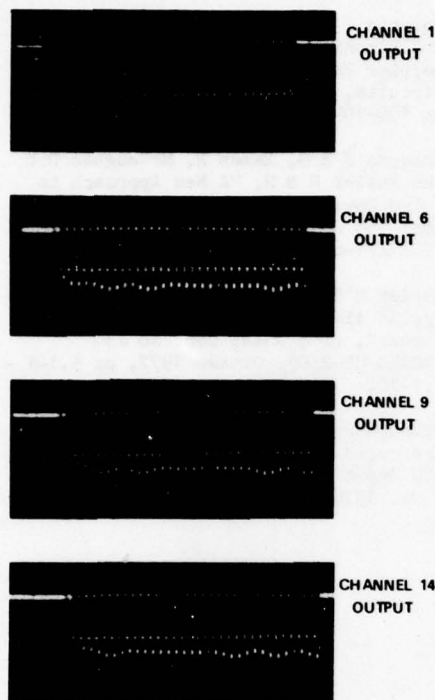
CHANNEL 14
OUTPUT

FIGURE 11 TYPICAL OUTPUTS

channel 6, samples from both dead and
active time are shown, as is the case in
channels 9 and 14 (iii) and (iv), compar-
ison between these pictures illustrating
the slippage of sampling points from
channel to channel in this mode of opera-
tion. On real radar data of course, there
would be vastly different doppler signals
from channel to channel unlike this simple
illustrative simulated data. Finally
Fig 12 shows the effect of overly large
high-clock voltage; (i) shows normal
operation using a high-clock DC value of
40% above normal clock voltage; in (ii) the
DC high clock is increased to 2 x the normal
clock voltage, which this particular channel
cannot handle without dark current problems.

In summary then the pulse doppler corner
turning store problem has been solved in a
new way, using the 3-level clock principle
for the first time to enable read-in and
read-out from the store simultaneously at
different rates in a complex manner with a
minimum of external connections to the
chip. The high-clock storage principle is
as equally applicable to 2 phase or 4 phase
structures. The new three level clock and
logic design makes implementation easy and
meagre in power consumption. Implemented
in CMOS the whole system, operating at
4 MHz output for the SAW analyser will
consume less than 2 watts in total.

The data in each parallel channel is
accumulated from 32 separate bursts of
input. Each input is slipped slightly in
time with respect to its predecessor so
that in each parallel channel successive
data points along the input waveform are
taken just as would be the case with real
radar data. Thus over 32 input bursts each
storage channel (range bin) accumulates a
history incorporating (in this case) a
1 kHz doppler signal. Due to this method
of input each channel is slightly displaced
in time with respect to its neighbours,
leading to the outputs from channels 1,
6, 9 and 14 chosen by way of example, and
shown in Fig 11 (i) to (iv). In (i),
channel 1, the samples start from the
beginning of the burst and include a lot of
the dead time between the input bursts, at
the right side of the picture. In (ii),

CHANNEL 3
DEEP WELL
40% OVER
CLOCK

CHANNEL 3
DEEP WELL
2X CLOCK

**FIGURE 12 OUTPUT SHOWING STORAGE
TIME EFFECTS**

8 Conclusion

The applicability of a single wideband spectrum analyser to the multichannel narrowband radar doppler processing problem has been shown. In many cases the interface is conveniently made using a digital store. However for wideband radars, and when power consumption and size are controlling factors it appears that CCD storage will be increasingly attractive, partly through its avoidance of multi-bit storage per sample and partly through dispensing with A/D interconversions. This promise will only be realised through the development of a specially configured CCD storage module requiring a minimum of control connections and adaptable to differing radar bandwidths and prfs.

The new clock and device configurations we have described represent an advance towards this module. The logic and drivers for the CCD clocks are capable of integration to minimise power and size. The storage modules may be chained together (by staggered clocking which avoids signal degradation through inter-CCD transfers) to meet the range-bin requirement of particular radars.

The principle limitation of the all-analogue approach is probably the dynamic range of ~40dB. This prevents its use in strongly clutter dominated situations unless the processor is preceded by a clutter filter. However a digital or analogue 3 or 4 pulse canceller will often be sufficient to allow very high speed analogue spectral processing to replace digital FFT methods. The advantage of course increases with the number of resolved doppler frequencies and ranges. A feature of this processor is its ready applicability to jittered-prf radar. By reproducing the jittered timing of samples in the compressed-time output of the store, the required ambiguity function is preserved. The SAW spectrum analyser operating in continuous time handles this naturally whereas the discrete, equally spaced sampling necessary to FFT processing cannot.

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3 Butler M B N, "Development and Application of an SAW Chirp-Z Transformer", Proc AGARD Conf No 230 (AGARD-CP-230), Ottawa 1977, pp 5.1-1 - 5.1-10.

4 McCaughan D V and Harp J G, "Phase-Preferred Input: A Simple New Linear CCD Input Method", Elec Lett $\underline{12}$ No 25, 9 Dec 1976, pp 682-683.

CCD SONAR BEAMFORMING

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ABSTRACT

CCD's provide a flexible approach to sonar beamforming. Wide bandwidth, small size, frequency agility, and low power dissipation are characteristics of CCD beamformers which make them attractive for many applications. This paper discusses the design of a special beamformer chip set and the systems which can be implemented with these and other CCD devices in a complete sonar system. The advanced CCD sonar chip, which has an "organ pipe" geometry, uses buried channel technology, double polysilicon electrodes, and an on chip MOS/bipolar analog reconstruction circuit. Experimental results are presented for a torpedo type beamformer with these advanced chips.

1.0 Introduction

In any sonar system one of the most important criteria for judging performance is its S/N enhancement. This processing gain is accomplished by frequency domain filtering which restricts the passage of signals to the target's probable frequency range (passive) or doppler range (active) and by spatial domain filtering or beamforming which limits the response of the array to a particular direction.

To steer a transducer array in a particular direction, a sonar designer must supply electrical delays to the appropriate hydrophone output in such a way as to cancel propagation delay of a wave incident on the array from that direction. Signals from other directions will be out of phase and will not add coherently. Figure 1 shows how a line array would be steered in a direction $\widehat{\theta}$ degrees from perpendicular.

The electrical delays required are found by multiplying element spacing (d) by the sine of the angle desired, and dividing the result by the sound velocity of water (v = 60,000 in./sec).

$$\tau = (d/v) \sin \widehat{\theta} \qquad (1)$$

The directivity response of the line array beamformer shown with a single frequency acoustic wave of wavelength λ incident upon it at an angle θ can be written as:

$$A(\theta) = \sum_{n=0}^{M-1} EXP\left[(j2\pi nd/\lambda)(\sin \theta - \sin \widehat{\theta})\right] \qquad (2)$$

where M = number of transducer elements. Because of the symmetry of the line array this can be further simplified to:

$$A(\theta) = \frac{\sin\left[(Md\pi/\lambda)(\sin \theta - \sin \widehat{\theta})\right]}{\sin\left[(d\pi/\lambda)(\sin \theta - \sin \widehat{\theta})\right]} \qquad (3)$$
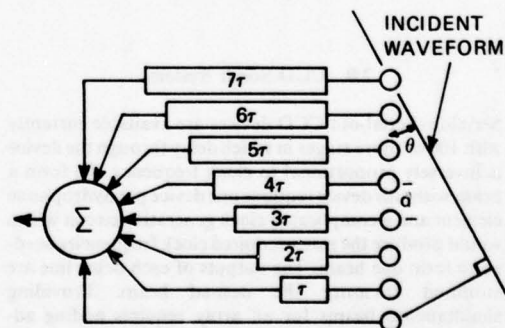
Figure 1. Basic Beamformer Structure

The above equations (2 and 3) describe systems which are made up of omni-directional transducer elements whose amplitudes are uniformly weighted or shaded. This is almost never the case. Each hydrophone element has its own directivity response which must be multiplied by the array beam pattern to obtain the system response. To reduce spatial sidelobes the outputs of the transducer elements are often weighted in a manner similar to time weighting an FM chirp in radar to reduce time sidelobes, or weighting a sample window for FFT processing to reduce frequency sidelobes.

For the general case of an array of hydrophones in space, the directivity response in polar coordinates is:

$$A(\theta,\phi) = \sum_{n=1}^{M} W_n \, G_n \, (\theta, \phi) \;\; EXP \, [(j \, 2\pi fs$$

$$\left(\frac{(X_n \cos \theta \sin \phi + Y_n \sin \theta \sin \phi + Z_n \cos \phi)}{v} - dn \right)]$$

(4)

where X_n, Y_n and Z_n are coordinates of the nth hydrophone,

d_n is the delay applied to the nth hydrophone.
v is speed of sound
M is total number of hydrophone elements.
W_n is shading coefficient of nth hydrophone
$G_n (\theta,\phi)$ is the directivity response of the nth
            hydrophone element

Current beamforming techniques include the use of phase shifting networks[3] in place of time delay for single frequency or narrow band systems, and the use of passive delay lines[1]. The advent of CCD technology has added a flexible and very small volume candidate for electrical delay for use by the sonar engineer.

2.0   CCD Sonar Systems

Serial-in/Serial-out CCD devices are available currently with 100 or more stages in which delay through the device is inversely proportional to clock frequency. To form a beam with this device requires one device per hydrophone element and a complicated clock generating circuit which would produce the many required clock frequencies needed to form one beam. The outputs of each delay line are summed forming the desired beam. Providing simultaneous beams for an array requires adding additional delay lines per element in proportion to the number of simultaneous beams required. The clock generating circuit for this scheme may become prohibitively large. A block diagram of a beamformer using this technique is shown in Figure 2a.

A second beamforming technique utilizes a serial-input/parallel-output tapped delay line charged coupled device for every transducer element. In this configuration, all the delay lines are clocked at the same frequency and are the same length; however, since the delay line is tapped along its length, the appropriate delay for each element can be obtained by selecting the delay tap that is closest to the exact delay required. A summing amplifier is used to sum the data from the selected tap on each line to form a particular beam. To provide simultaneous beams requires additional summing amplifiers to add the data that is available along each line. As the number of beams required is increased, the number of interconnects greatly increase making this approach less and less attractive. Many floating gate output structures and the associated reconstruction circuitry that must be implemented on a single chip make long tapped delay lines difficult to produce. Figure 2b shows a system implemented in this manner.

A third type of system architecture makes use of a parallel-in/serial-out, also known as delay and add, CCD device. This device is either a corner turning memory with modified clocks or many parallel CCD's of different lengths summed together. The outputs from the array elements are connected to the parallel inputs of the CCD. As the device is clocked, the element signals are each delayed the amount required for a particular beam and are added together by summing the injected charge packets within the monolithic device. This configuration requires only one CCD device per formed beam and the total number of devices is equal to the number of beams required. The packaging volume required for a beamformer system in which the number of beams is less than the number of array elements is considerably less than the other two configurations discussed. The architecture of this system is shown in Figure 2c.

Since any CCD beamformer system is a sampled data system special attention must be paid to delay or phase quantization, which is the measure of how accurately an electrical delay can be approximated with a delay equal to a multiple of the CCD clock period. Course quantization will tend to broaden the main beam and will raise sidelobe levels, especially if the transducer array is shaded for very low sidelobes. Computer simulations of various test arrays have shown that 10 x oversample ($\pm 18°$ phase quantization) will produce sidelobe levels no better than -28 dB regardless of shading function used. Each system should be simulated to choose the phase quantization required to meet system requirements.
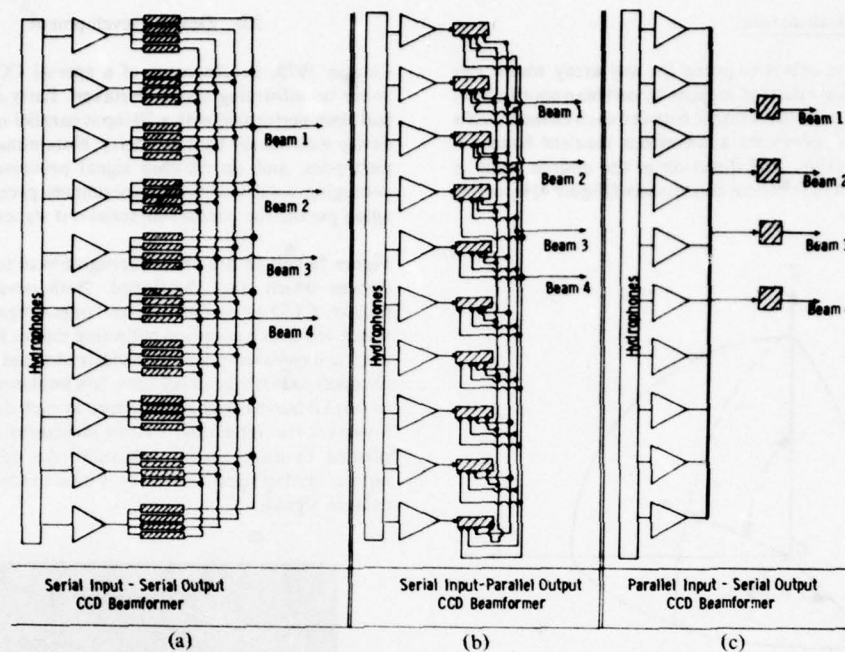
Figure 2. System Architectures

Frequency aliasing which is of great concern in most sampled data systems is not normally a problem when designing a CCD beamformer. The resonant response and high frequency roll off of the hydrophone element plus attenuation characteristics of the water medium provide the anti-alias filtering required.

Gain differences from tap to tap on a CCD device resulting from pattern variation is another source of error contributing to slight degradation of steered beam response. Similar degradation occurs in the beam pattern if the response of each hydrophone does not track with angle. Statistical analysis of these problems have resulted in the graph of Figure 3. This shows the average sidelobe level attainable given average amplitude mismatch.

The effect of CCD transfer inefficiency is negligible for most beamformer applications. Z transform analysis[6] of a CCD taking transfer inefficiency into account yields the following transfer functions:

$$(V_{out}/V_{in}) = \overbrace{(C_{in}/C_{out})\, e^{-\epsilon N(1-\cos 2\pi(fs/fc))}}^{\text{Amplitude}}$$

$$\underbrace{e^{j2\pi N\,(fs/fc)}}_{\substack{\text{Desired}\\\text{Delay}}} \quad \underbrace{e^{jN\epsilon \sin 2\pi\,(fs/fc)}}_{\text{Phase Error}} \qquad (5)$$

where N is the number of stages, ϵ is transfer inefficiency per stage, fs is signal frequency, and fc is sample frequency. For a 10 x oversampled system using a CCD with an ϵ of 10^{-4}, 500 stages are needed to obtain a 0.1 dB amplitude error and 1.6 degree phase error.
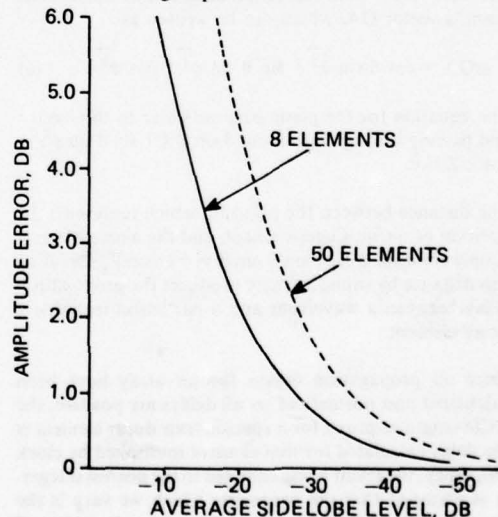
Figure 3. Average Sidelobe Vs. Amplitude Mismatch

2.1 Delay Calculation

To determine delays required for any array whose element centers are defined in space by cartisian coordinates, we must examine the distance between each element and a plane which represents a wavefront incident from the desired direction. The direction of the desired beam is usually given in spherical coordinates (Figure 4) by defining θ and ϕ.
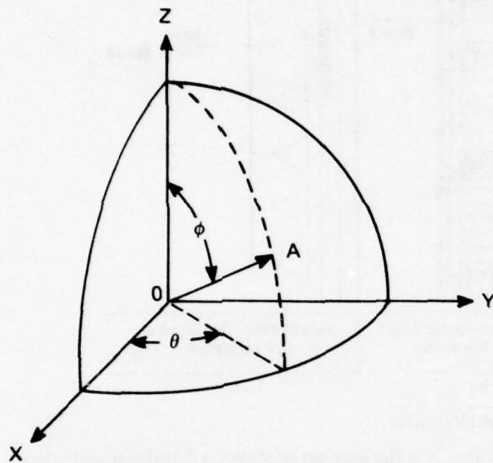
Figure 4. Coordinate Definition

The unit vector pointing in the direction of the desired beam is vector OA, which can be written as:

$$OA = \cos \theta \sin \phi \vec{i} + \sin \theta \sin \phi \vec{j} + \cos \phi \vec{k} \qquad (6)$$

The equation for the plane perpendicular to this vector and passing through zero is $\cos \theta \sin \phi X + \sin \theta \sin \phi Y + \cos \phi Z = 0$.

The distance between the point P_i, which represents the position of a transducer element, and the above plane is simply $\cos \theta \sin \phi X_i + \sin \theta \sin \phi y_i + \cos \phi Z_i$. Dividing this distance by sound velocity produces the propagation delay between a wavefront and a particular transducer array element.

Once all propagation delays for an array have been calculated and normalized so all delays are positive, the CCD length required for a specific transducer element is the delay calculated for that element multiplied by clock frequency, the result being rounded to the nearest integer. It is assumed that the parameter which we vary is the length of the CCD delay line. The delay lines for all elements will be clocked in parallel.

3.0 Device Development

Late in 1975, development of a special CCD chip for sonar beamforming was undertaken. Early experiments had been performed with a 20 input parallel-in/serial-out device with corner turn geometry, aluminum-polysilicon electrodes, and an off-chip signal processor. The encouraging results of these experiments prompted us to again pursue the parallel-in/serial-out structure.

Figure 5a and 5b are photomicrographs of the two CCD devices which were developed. Both devices contain parallel CCD delay lines in an "organ pipe" geometry which fed into a common collecting diode. Both devices use $7\ \mu$m coplanar polysilicon electrodes and $50\ \mu$m wide channels to form the delay lines. Ion implantation is used to form a buried channel structure in each delay section; however, the input and output structures are not implanted to insure linear operation. An on-chip MOS bipolar analog signal processor is used to reconstruct the delayed signals.

a. 7011/64

b. 7011/16

Figure 5. Photomicrographs Of CCD Sonar Devices

The larger device (200 mil x 165 mil) contains 64 parallel delay lines, each line different in length from the next by one delay. Signals are injected at structures along the top and bottom and are clocked toward the center diagonal connection point. If a particular transducer array and steering angle required more than one hydrophone element signal to be delayed the same amount, these signals would be added prior to injection into the CCD. The elimination of pre-summing circuitry could be accomplished with special chip designs which duplicate delay lines of the same length where needed. The smaller device (85 mil x 70 mil) is similar to the 64 input device but contains 16 delay lines. This device was designed to steer smaller line arrays.

The delay line structure and output circuitry used in both devices is shown in Figure 6. A four phase structure clocks the charge samples obtained by stabilized charge injection through the delay line. Charge packets which are collected at the output are added in the diagonal connecting structure of each chip and applied to a source follower MOS amplifier. A sample gate is then pulsed which stores the signal on a 1 pf capacitor. The signal on the sample and bold amplifier is buffered by a bipolar transistor which must be connected to an external load. Both devices use 15V clocks which are generated by CMOS logic circuits. The signal applied to each input sits on an 8 volt pedestal.
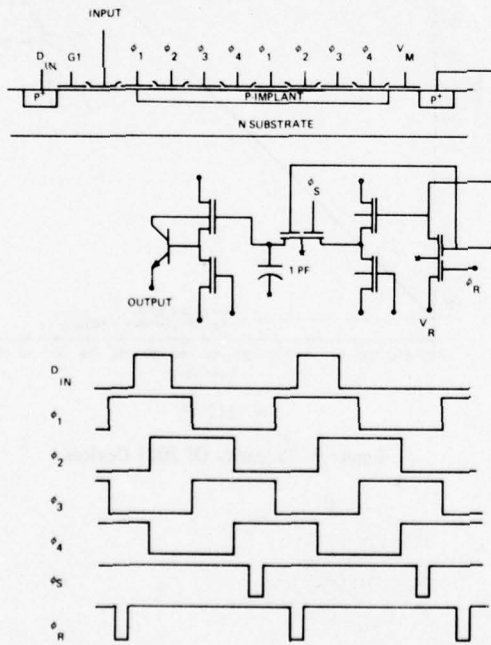
Figure 6. CCD Structure And Operating Waveforms

The output of this device is shown under two test conditions in Figure 7a and b. In Figure 7a, 28 successive inputs of the large device were connected together forming a transversal filter whose impulse response is a unit step 28 clock periods long. A pulse was applied to the common input, resulting in an output which is the convolution of the impulse response and the input waveform. Figure 7b is the output with a sine wave applied to the inputs.
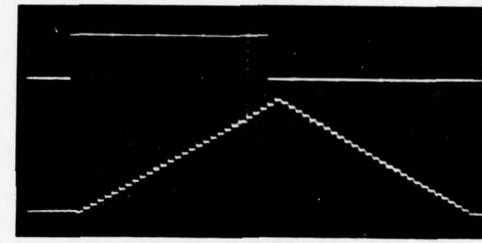
a. Input 5 v/Div
   Output 0.5 v/Div
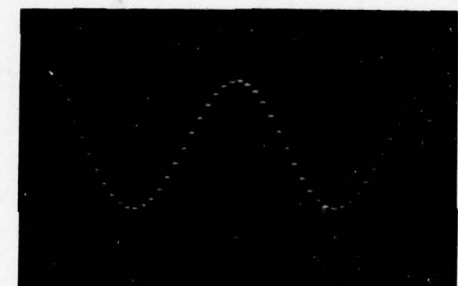
b. Vert 0.5 v/Div
   Horiz 10 μsec/Div

Figure 7. Output Waveforms

Linearity and dynamic range are the device parameters which most concern the system designer. Extensive measurement of these and other parameters were made over a wide temperature range. Shown in Figure 8a and b are plots of output noise spectral density for different temperatures and for different clock frequencies. Noise bandwidth of the spectrum analyzer was 160 Hz, which makes the plot 22 dB above noise in a one Hertz band. The spike present at approximately 6 kHz is a pilot tone used to monitor linear operation. Other signals are spurious response caused by nearby machinery. For all cases measured, output noise was less than -125 dBv/Hv at 25 kHz. Because there is a loss through the CCD device ($C_{in}/C_{out} \cong 1/$ Number of Inputs), noise reflected to the inputs, assuming all inputs are considered, is $-125 + 10 \text{ Log } N$. For the 16 input device this level is -113 dBv$\sqrt{\text{Hz}}$.
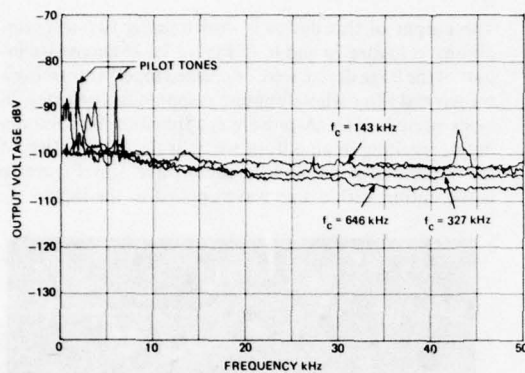
a. Various Clocks
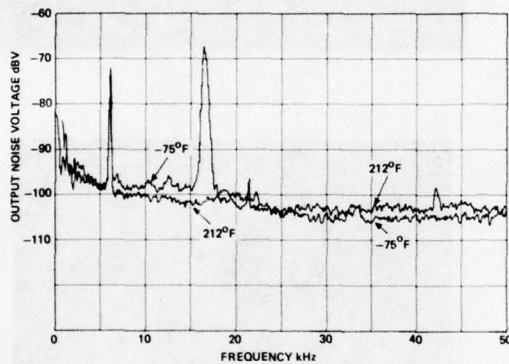
b. Temperature

Figure 8. Output Noise Spectra

Linearity and harmonic distortion were measured at both room temperature and 212°F. Input signal levels were varied from -100 dBv to +10 dBv while the output was observed on a spectrum analyzer. Plots of the resulting data are shown in Figure 9a and b. Maximum clocking speed of these devices was measured to be approximately 3.5 MHz, although for applications under consideration they would not be operated higher than 1 MHz. Transfer inefficiency, ϵ, is less than 10^{-4} per stage.
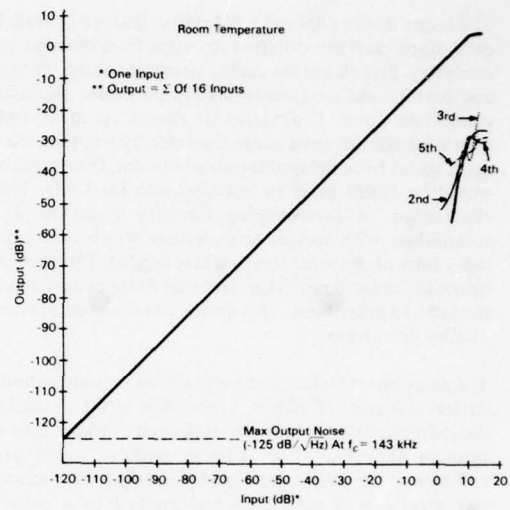
a. Room Temperature
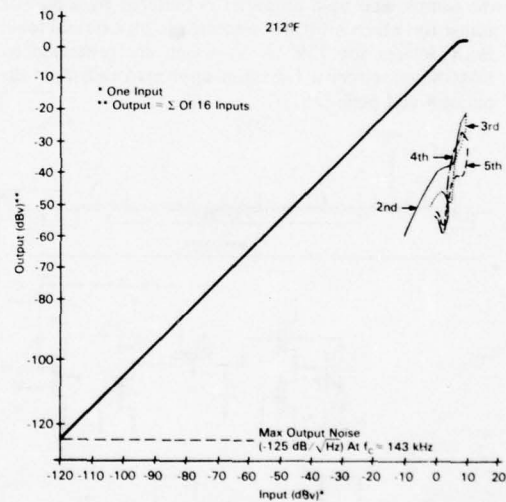
b. 212°F

Figure 9. Linearity Of 7011 Devices

4.0 Test Results

Using one of the 7011/64 devices with 28 inputs available (pin limited), a breadboard beamformer was built to steer a 7 x 7 torpedo transducer array. The array configuration used is shown in Figure 10. Delays were calculated to steer the response pattern 9° in elevation and 26° in azimuth. The delay tap on the CCD required for each transducer element is shown on that element in the figure. The clock frequency required in the CCD is 307 kHz, but by varying the clock the direction of the beam could be positioned along the dotted line in Figure 10b.
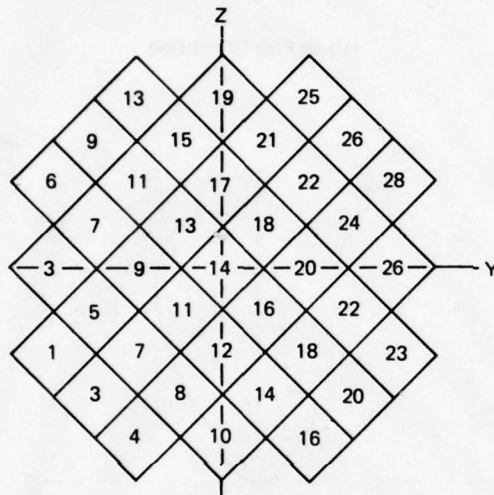
a. Numbers Indicate Delay Stages Required
Per Transducer Element
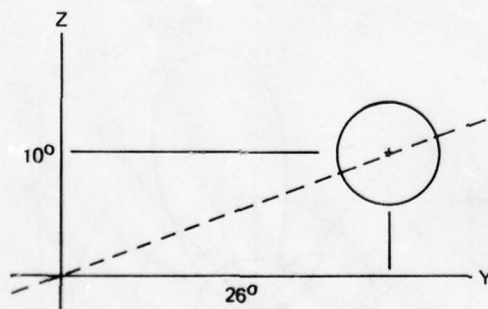
b. Beam Formed With 307 kHz Clock

Figure 10. Beamformer Delay Assignments

The block diagram of the breadboard beamformer in Figure 11 shows the single chip per beam architecture discussed previously. A preamplifier provides gain and amplitude shading for each transducer element. Some transducer elements required the same delay, so resistor summing was implemented as shown. The preamp outputs were DC coupled to the CCD device utilizing the preamp output bias as the DC level necessary for signal injection.

Beam patterns were taken by rotating the transducer about its perpendicular until the main lobe of the beam lay in the horizontal plane. Azimuth patterns were taken in this orientation with various input frequencies and clock frequencies. Results of these tests are shown in Figure 12a through e.
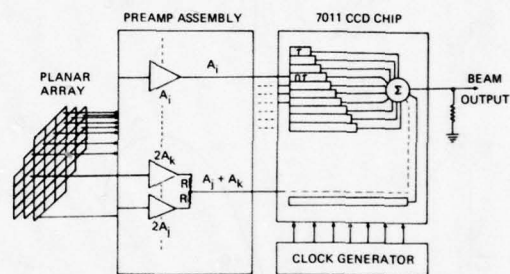
Figure 11. Block Diagram Of Breadboard Beamformer

5.0 Two Stage Beamforming

The orthogonal symmetry of many planar transducer arrays can be utilized in a system architecture offering many advantages over a simple chip per beam system. The vertical column of transducer elements is connected through preamps and shading networks to a small parallel input CCD device such as the 7011/16. Each of these first stage devices is clocked in parallel with a clock frequency f_v which is inversely proportional to the desired verticle steering angle. Each of the vertical steered columns is in turn connected to a second CCD clocked at a frequency f_h which is proportional to the desired horizontal steering angle. The basic structure for this system is shown in Figure 13, which represents components needed to position a beam anywhere in one quadrant.

Independent steering of horizontal and vertical axes offers potential system flexibility and may eliminate the need for a bank of many beams. The problem of phase quantization is eliminated since we take advantage of transducer array symmetry and uniform transducer element spacing in this implementation.
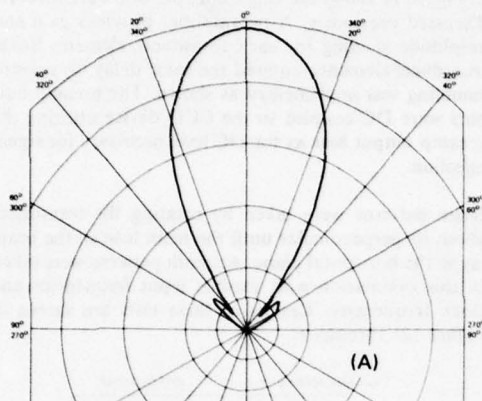
A. SUM PATTERN (UNSTEERED)
B. f_{CLOCK} = 307.2 KHZ f_{SIGNAL} = 20.5 KHZ
C. f_{CLOCK} = 625 KHZ f_{SIGNAL} = 20.5 KHZ
D. f_{CLOCK} = 307.2 KHZ f_{SIGNAL} = 19.2 KHZ
E. f_{CLOCK} = 625 KHZ f_{SIGNAL} = 19.2 KHZ

(10 dB PER DIVISION)
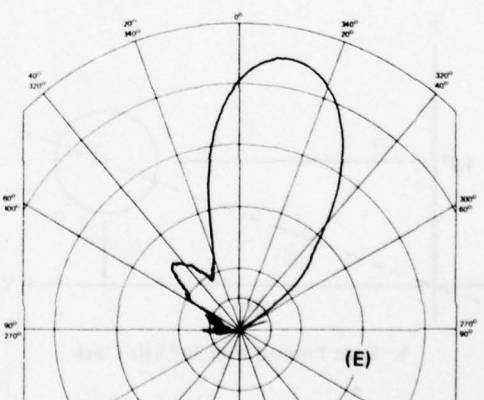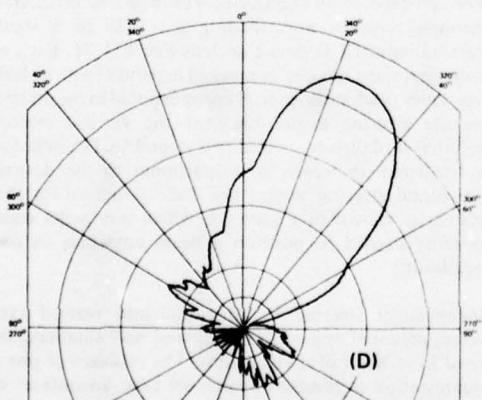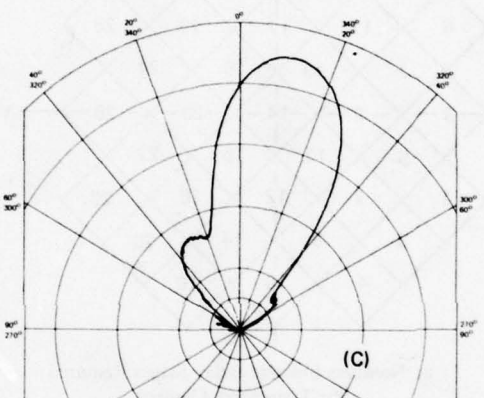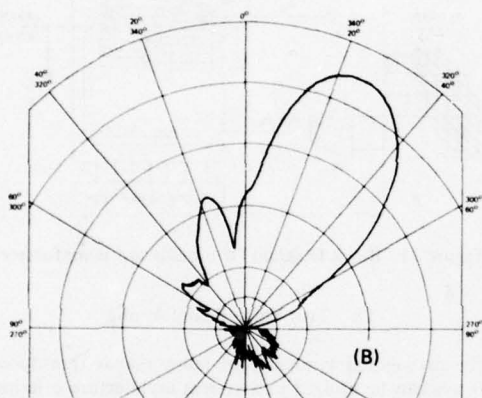
Figure 12. Beam Patterns From Steered Torpedo Array (40 dB Shading)
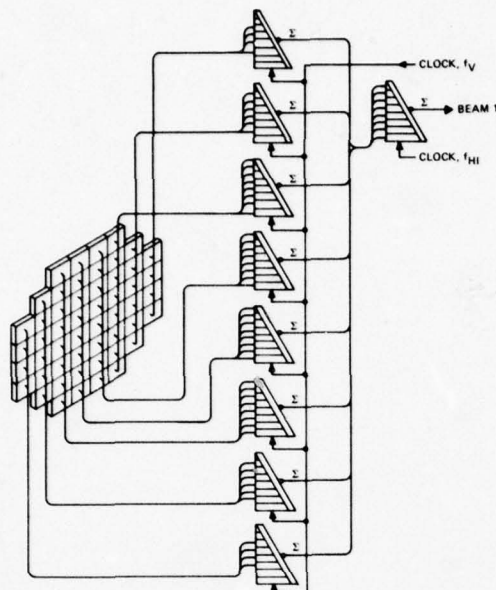
Figure 13. Two Stage Beamformer

CLOCK, f_V

Σ BEAM 1

CLOCK, f_{HI}

6.0   Summary and Concluding Remarks

CCD devices are an ideal building block to provide time delays required for sonar beamforming. The parallel-in/serial-out structure of current CCD devices permits implementation of beamformer systems which occupy a very small volume — a necessity for torpedo or small underwater search vehicles. The power requirements of a CCD beamformer system are also very small and average approximately 15 mw per CCD device which includes the capacitive loading of electrodes at a 1 MHz clock rate. Since a CCD is a time delay beamformer it will operate over a wide range of input frequencies and opens the door to implementation of multi-frequency or FM chirp systems. Unlike passive delay lines, the delays through a CCD and therefore the steered beam angle are alterable by changing clock frequencies. This allows for further system flexibility which may reduce the number of beams required by a system.

Bench testing of a CCD beamformer is a very easy task to accomplish. Replacing a line of transducer elements by an oscillator common to each input changes the beamformer into a transversal filter whose frequency response is identical to the spacial response of the beamformer assuming omnidirectional transducer elements.

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4.   M.H. White, "Charge-Coupled Device (CCD) Analog Signal Processing", 1975 Int'l Conference on the Application of CCD's, Oct. 1975

5.   D.R. Lampe, et. al., "CCD's for Discrete Analog Signal Processing (OASP)", Intercon 74, March 1974, New York.

6.   M.H. White and W.R. Webb, "Study of Charge Coupled Devices for Use in Analog Signal Processing", Final Report NRL Contract N00014-74-C-0069, May 1974

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8.   G.A. Gilmour, *High Resolution Sonar*, Westinghouse Electric Corp. OER 76-21, June 1976.

A CHARGE-COUPLED DEVICE FOR SONAR BEAM FORMING

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FRANCE

ABSTRACT   This paper describes a charge-coupled device (CCD) that has been specially developed for sonar beam forming.

The principle of operation that is employed here for beam forming reduces the number of interconnections to a minimum. It consists of sampling and multiplexing the signals from a large number of hydrophones, the samples then being fed into a delay line. The signal is non-destructively read out at different points along the delay line so that, at a given time, the delays required to form a particular beam are available. An instant later, the signals available at the same points permit forming another beam, and so on. The device that has been developed consists of a transversal filter having 512 stages, of which only 39 coefficients are non-null. It permits forming 32 beams from a circular array of 32 hydrophones, each beam using 12 hydrophones.

I. INTRODUCTION

In sonar systems, as a general rule, the signals from the hydrophones of the antenna are spatially processed. The operations involve the weighted sums of delay signals.

Systems primarily based on cabled circuits use a very large number of circuits and interconnections. Systems primarily based on software need a large computing capacity because of *the number and high frequency of the signals that must be processed.*

However, the delays and weightings required for beam forming can be performed by CCD delay lines [1]. Several techniques can be used. The first (Figure 1) is to use one delay line per hydrophone, the signals thus being processed in parallel. The operation is repeated as many times as there are beams. This method requires many interconnections because the processing system cannot be integrated into a single unit. Another way (Figure 2), only suitable for circular arrays, is to multiplex the signals from the hydrophones and to process them in a single CCD that is analogous to a transversal filter. The beams are formed successively by the same circuit, and are supplied multiplexed.

The interconnections are reduced to a minimum, but the length of the delay line and the clock frequency may exceed the technological possibilities. By interpolating the samples of signals in the same circuit, the last two parameters can be minimized without increasing the difficulties of realization.

The CCD described in this paper uses the second technique.

II. PRINCIPLE OF OPERATION OF CCD BEAM FORMING

The beam-forming method described is applicable to a large bandwidth sonar having a circular array of N hydrophones, M hydrophones being used for each beam.

To form a beam, the signals x_i (t) from the M hydrophones are added after having been delayed τ_i and weighted A_i so as to compensate for the delays due to the geometry of the array, *and to ensure the required beam pattern response as a function of the angle of incidence of a plane wave* :

$$y\ (t) = \sum_{i=1}^{M} A_i x_i\ (t)\ \delta\ (t-\tau_i).$$

The signals from the N hydrophones are sampled at a frequency F_e, and then sent multiplexed in series into a CCD delay line of L stages that has M taps corresponding to the delays τ_i. The taps are connected to an adder. At a time t, the output signal of the adder is a sample of a beam, and a time $t + \Delta t$ it is a sample of the next beam. After a time $N\Delta t$, all N beams have been formed. The CCD must have a number of stages L, and a sampling frequency $F = NF_e$, such that :

$$L = \tau_{max} \cdot FeN,$$

where τ_{max} is the maximum geometrical delay that is to be compensated.

The delays τ_i are composed of a whole number of sampling periods. If this quantification is not to alter the beam pattern, the following condition must be satisfied :

$$Fe >> 2F_{max} .$$

where F_{max} is the upper limit of the frequency band. Because of this requirement, L can reach very high values, which are technologically difficult to realize, and where the transfer inefficiency, ϵ, would be prohibitive at the frequencies concerned.

To reduce L, Fe must be reduced, the signals then being delayed by fractions of sampling periods to obtain a suitable beam pattern.

This can be done by interpolating the signal samples in an FIR (Finite-duration Impulse Response) filter. This type of filter is easily realized on CCD registers by adding 2p taps around the theoretical delay τ_i (Figure 3). From the 2p samples of signal x_i (nT), one calculates (Figure 4) :

$$X\left[(n+a)\ Te\right] = \sum_{j=0}^{j=2p-1} I_{aj} \times \left[(n+p-j)Te\right]$$

where : $a < 1$

and $\quad Te = \dfrac{1}{F_e}$.

The interpolation coefficients, I_{aj}, can be calculated in several different ways (Spline function, Lagrande polynomials, etc.).

The value of p depends on Fe/F_{max} and on constraints due to the beam pattern.

In this way, F_e/F_{max} and the number of stages, L, can be greatly reduced. The influence of ϵ is thus minimized

Because the sampled signals from the hydrophones are multiplexed in the delay line, the transfer inefficiency, ϵ, creates *intermodulation* between them, which results in a deviation of the beam axis and a change in the secondary lobes of the beam pattern.

Figure 5 shows the effect of interpolation at 5 kHz on the beam pattern of an array of 32 hydrophones, 12 hydrophones being used per beam, for F_e/F_{max} equal to 6 and 2.5.

Figure 6 shows the influence of ϵ on the beam pattern of the same array at 5 kHz.

This beam-forming circuit is thus similar to a transversal filter with Np taps. In addition, by modifying the tap weighting of the circuit, specific changes can be made to the basic beam pattern as a function of the frequency. This possibility is very interesting for large-bandwidth sonars.

III. DESCRIPTION

The device described below was designed for a circular antenna of 32 hydrophones, and was to give 32 beams, each beam using 12 hydrophones. The frequency F_e was chosen to be 6 F_{max} = 30 kHz. The CCD's clock frequency was thus to be 32 F_e = 960 kHz.

Interpolation of each delay was assured by 2p = 4 taps.

Because a maximum delay, τ_{max}, of 396 μs was required, the total number of stages was given by L = τ_{max}F + 3 elements per interpolation = 380 + (3 x 32) = 476.

In actual fact, the CCD was realized with a total of 512 stages so that it could be used for other applications.

The beam-forming circuit is thus, practically speaking, a delay line with a large number of delay elements, which has several intermediate taps where the signal can be read non-destructively. To read and weight the signal with interpolation at the taps, a split-electrode design was used, so that the device has the structure of a CCD transversal filter.

The schematic diagram of this device is shown in Figure 7. An input stage permits biasing the signal samples so that they can be injected into the CCD. The samples are then delayed 512 times, and meet 39 taps where they are read out non-destructively because of the split electrode structure. Due to the large numbers of stages, a folded design was used, the arms of 128 stages being interconnected by diffusion zones [2]. A serial output permits checking the correct operation of the delay line. The split electrodes are connected to two charge-sensing circuits, which work by integrating the charge currents in low-value capacitors C− and C+.

After biasing, the voltages available at these capacitors control the injection into the two channels of a differential CCD stage [3]. The potential of floating electrode FG, which is proportional to the difference between the charges injected into the two channels, supplies the output signal after a sample-and-hold stage.

This device was made using N-channel technology with two levels of polycrystalline silicon, and TMOS depletion. Figure 8 is a photomicrograph of the circuit. The chip dimensions are 4.4 mm x 2.6 mm.

IV. EXPERIMENTAL RESULTS

Here we present the results of the first series of tests on the circuit. Three supply voltages and seven phase signals were required.

The impulse response (Figure 9) is a means of assessing its performance. The operating frequency is 1 MHz, and the output signal is available on the 500 ns-wide peaks of a square wave. Unit tap weightings are available at several points along the delay line, so the transfer efficiency is easily assessed.

For example, the 1st and 381st stages have unit tap weighting. So, the ratio of the signal amplitudes measured at these two points gives directly the transfer inefficiency (these are two transfers per stage) :

$$\epsilon = \frac{1}{2(N-P)}\ \ln \frac{An}{AP}\ ,$$

where $P = 1$ and $N = 381$.

The first batches of these devices were made using surface transfer technology, which gave measured values of ϵ that varied from 2.5×10^{-4} to 4×10^{-4}. These values are too high for beam-focusing applications, as they correspond to excessive deflection of the beam axis (Figure 6). For this reason, buried-channel technology was used to reduce ϵ to 10^{-4} or less.

To evaluate the performance of the whole device, it was operated as a matched filter. A PROM was then programmed to generate the time-inverted impulse response, in three levels $(0, +1, -1)$, of the CCD.

When fed into the CCD, this signal should give an output signal with a correlation peak whose amplitude with respect to the secondary lobes can be used to characterize the overall performance of the device. In addition, the amplitude of this peak is close to the maximum level for normal beam-focusing operation, so it can be used to estimate dynamic range.

Figure 20 shows this operating mode. The correlation peak amplitude is 7 dB above the first lateral lobe, instead of the theoretical value of 7.4 dB.

The dynamic range is estimated from the ratio between the maximum signal and the noise measured in an 8-kHz bandwidth. First results give a figure of better than 60 dB.

V. CONCLUSION

These first results prove the feasibility of forming sonar beams by using CCD's and applying the principle of multiplexed hydrophones with interpolation.

More complete results will be obtained when the device is used with a simulated sonar antenna.

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FIG.1   PARALLEL   BEAMFORMING

FIG. 2   MULTIPLEXED   BEAMFORMING
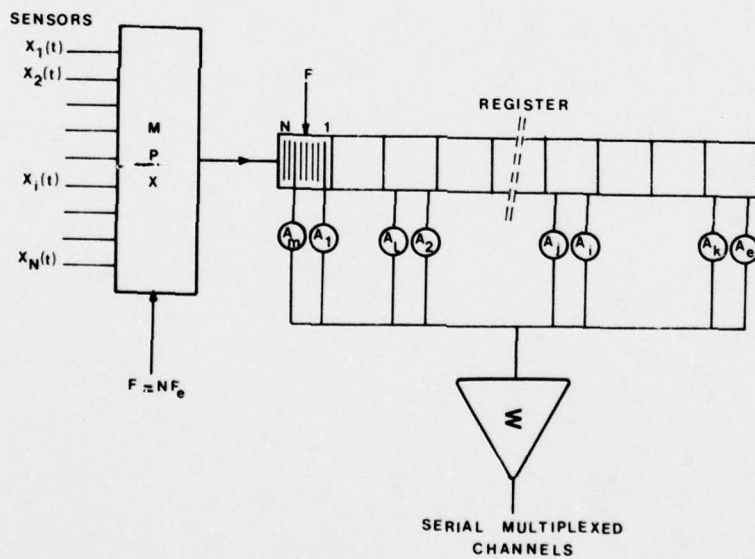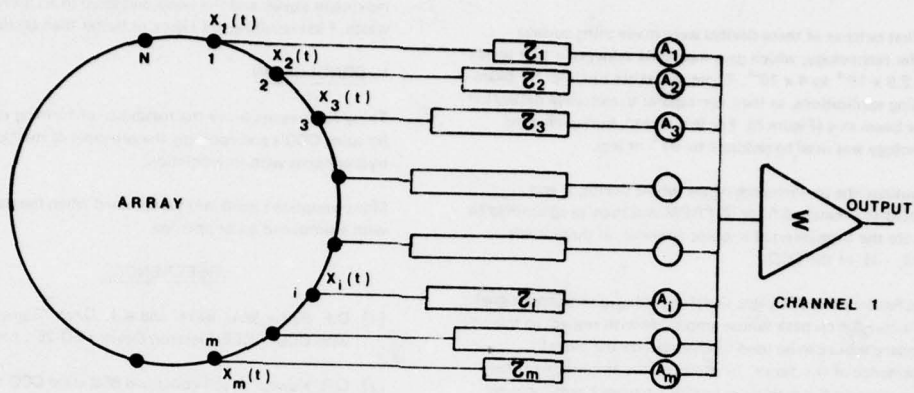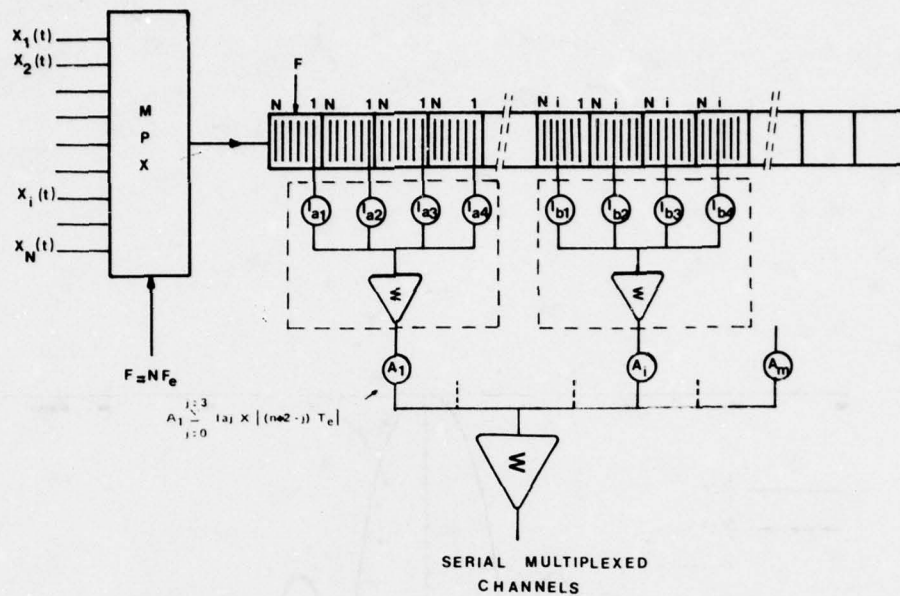
FIG.3 MULTIPLEXED BEAMFORMING WITH INTERPOLATION
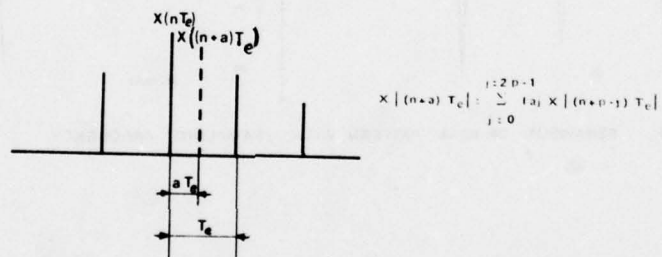
FIG. 4 INTERPOLATION METHOD
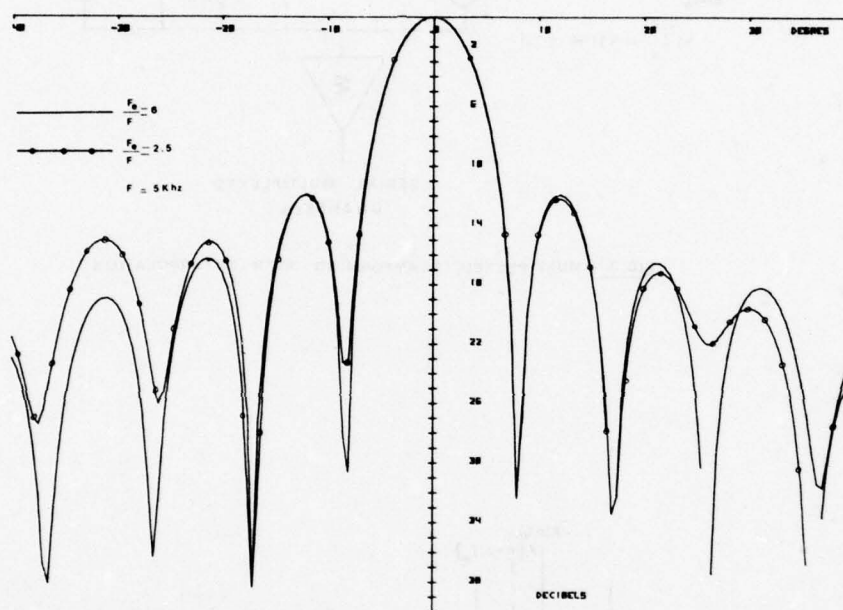
FIG.5   BEHAVIOUR OF BEAM PATTERN WITH   SAMPLING FREQUENCY
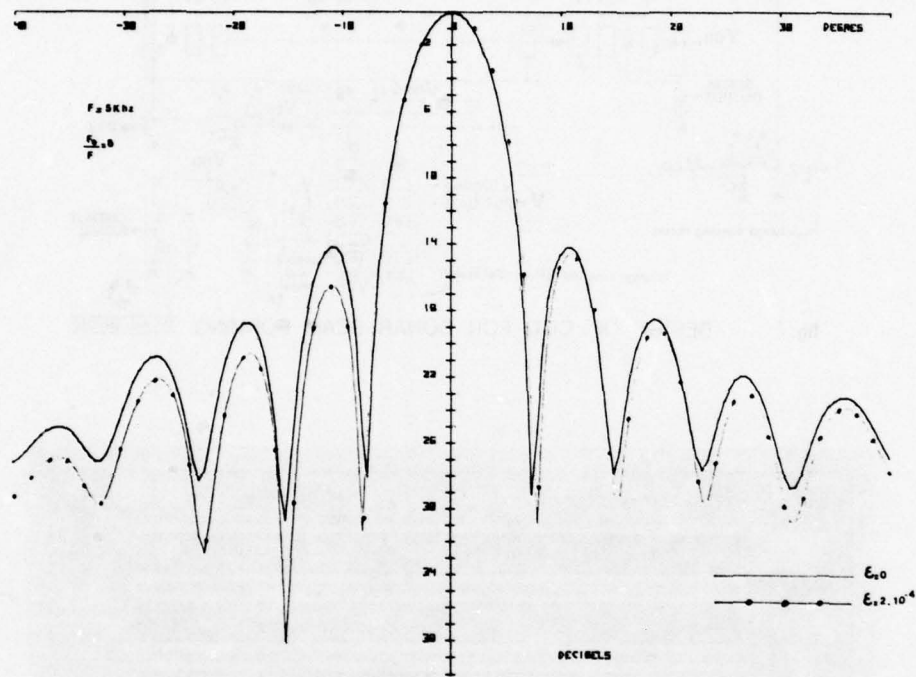
FIG 6   BEHAVIOUR OF BEAM PATTERN WITH TRANSFER EFFIENCY ε
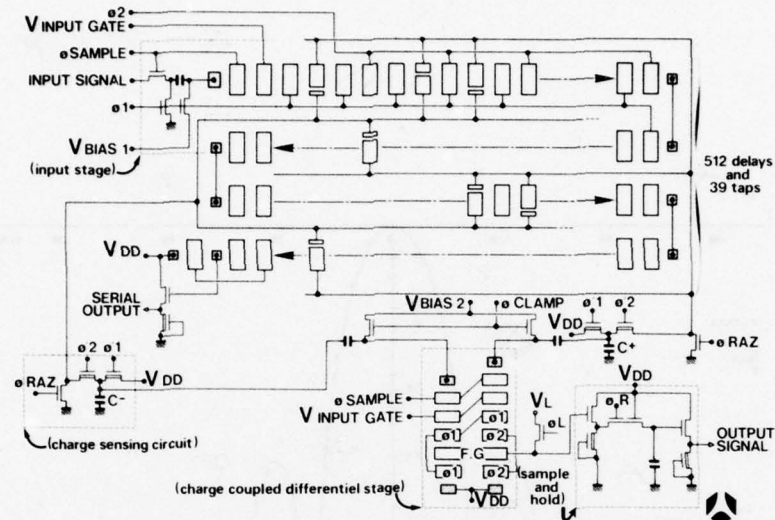
fig. 7   DESIGN OF CCD FOR SONAR BEAM FORMING   THOMSON-CSF
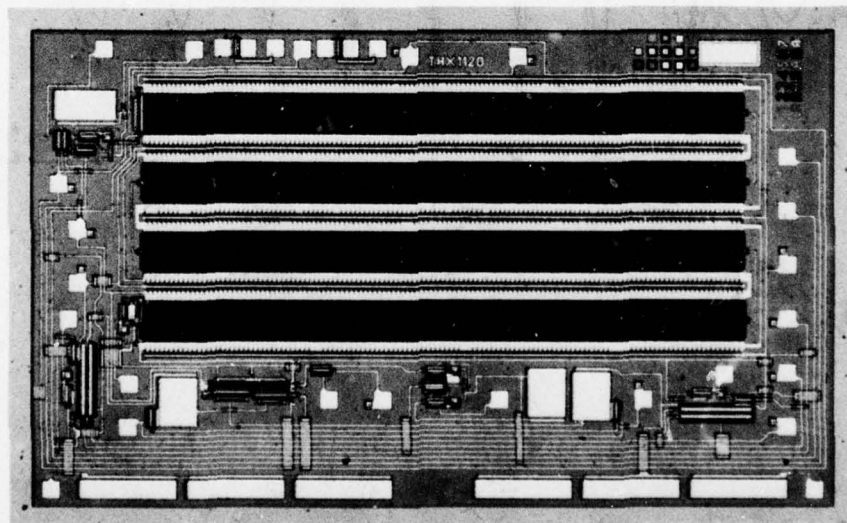
fig. 8 : PHOTOMICROGRAPH OF CCD FOR SONAR BEAM FORMING

INPUT

OUTPUT
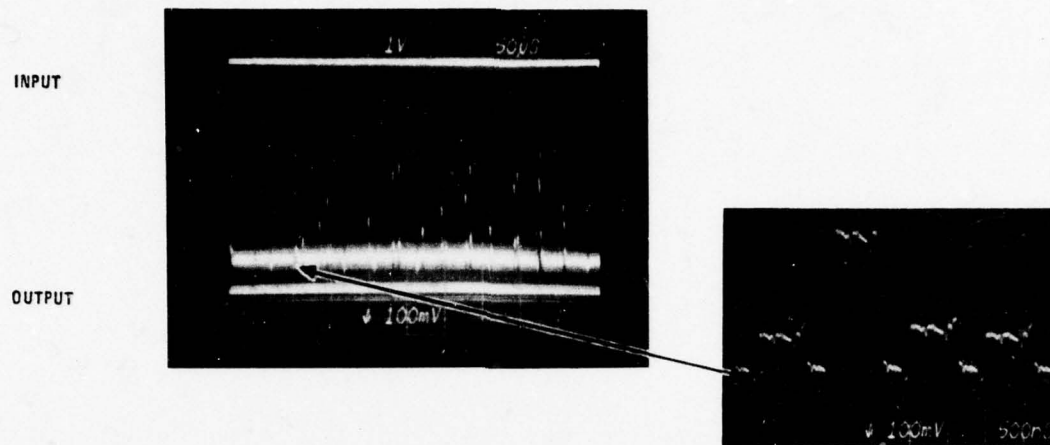
fig. 9 : IMPULSE RESPONSE OF CCD FOR SONAR BEAM FORMING

INPUT

OUTPUT
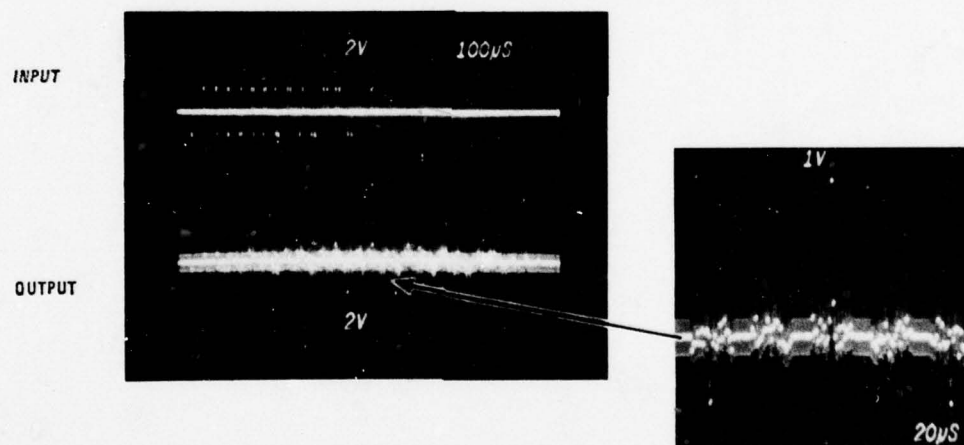
fig. 10 : AUTOCORRELATED RESPONSE TO A THREE LEVELS
ADAPTATED INPUT

Radiation Tolerance Constraints on CCD Application

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Abstract

Charge-coupled devices have been
shown to be sensitive to both neutron and
ionizing radiation effects. They are also
very susceptible to transient radiation
induced loss of stored information. Un-
hardened devices are usually severely de-
graded for doses greater than 5×10^4 rads
(Si). A total ionizing dose radiation
hard technology has been developed which
enables the devices to tolerate 10^6 rads
(Si). CCD use in 77°K radiation environ-
ments, in common with all MOS devices, is
presently severely restricted due to accel-
erated oxide charge buildup during irradia-
tion. The neutron induced degradation of
transfer efficiency in surface channel
CCD's is typically more than an order of
magnitude smaller than that observed in
buried channel structures.

Introduction

Charge-Coupled Devices (CCD's) have
potentially extensive applications in
optical imaging, signal processing, and
serial memories. They have small size,
low power consumption, and high relia-
bility. Such characteristics make CCD's
attractive for certain space and military
missions provided the devices can satisfy
the radiation hardness requirements. The
CCD radiation tolerance required will of
course be dependent on the radiation en-
vironment and the amount of shielding
available. An unshielded device in certain
earth orbits can receive a dose in excess
of 10^6 rads (Si) per year from electrons
and protons trapped in the Van Allen Belts.
Nuclear weapons environments may subject a
device to neutron fluences in the 10^{11} to
10^{13}n/cm^2 (1 MeV equivalent) range and

gamma ray doses from 10^4 to 10^6 rads (Si).

The purpose of this paper is to aid
the systems design engineer by providing
information concerning the nature and
magnitude of radiation induced degrada-
tion of CCD parameters. In addition,
techniques for obtaining the maximum dose
tolerance from a given device structure
are presented along with the optimized
CCD structural design for radiation en-
vironments. The increased total ionizing
dose tolerance of CCD's fabricated with
a radiation hard oxide is described and
the more rapid positive charge build-up
in silicon dioxide during 77°K irradia-
tion is discussed.

Radiation Effects in Semiconductor Devices

The basic effects of radiation on
semiconductor devices have been described
by Gregory.[1] The salient features of
that review will be briefly outlined here
as a background for the discussion of
expected radiation effects in CCD's.

High energy radiation deposits energy
in semiconductor materials via two mech-
anisms, atomic collisions and electronic
ionization. The relative importance of
these two mechanisms depends both on the
type of radiation and the nature of the
device. Electrons, protons, and gamma
rays deposit most of their energy via the
ionization process, while fast neutrons
deposit up to 50% of their energy in
atomic displacement damage. MOS devices
are more sensitive to ionizing radiation
(surface damage), while the characteris-
tics of bulk-effect devices such as bi-
polar transistors, are usually degraded
by displacement damage. However, CCD's

are sensitive to both surface and bulk displacement damage effects. They are also very susceptible to transient-radiation induced loss of stored information.

Numerous studies have shown that ionizing radiation causes failure of MOSFET devices due to two mechanisms: 1) trapped charge buildup in the silicon dioxide layer and 2) an increase in the density of trapping states at the silicon-silicon dioxide interface. Ionizing radiation generates electron-hole pairs in the silicon dioxide. The electrons are swept out of the oxide but some of the holes are trapped permanently producing a negative threshold voltage shift. The size of the threshold voltage shift varies with the magnitude and polarity of the applied gate bias during irradiation. Positive gate-substrate bias results in a greater threshold voltage shift since the holes are trapped near the silicon surface where they will exert maximum influence on the semiconductor. The absolute magnitude of the oxide charge and interface state buildup is also greatly dependent on the details of the fabrication process.

In addition to these permanent degradation mechanisms, ionizing radiation produces electron-hole pairs in the silicon substrate during irradiation. Carriers produced in device depletion regions, or within a diffusion length of these regions, can produce photocurrent at the device terminals. These photocurrents can cause large transients in linear circuits, and can cause error in the information stored by logic circuits.

Fast neutron irradiation produces displacement damage in the silicon which leads to significant decreases in carrier concentration, carrier mobility, and minority carrier lifetime. Decrease in carrier concentration and minority carrier lifetime reduction are the dominant failure mechanisms in most neutron irradiated bulk semiconductor devices. Mobility degradation does not become severe in silicon until neutron fluence exceeds 10^{15} neutrons/cm^2.

Surface Damage Effects

Since CCD's are MOS devices, ionizing radiation causes a buildup of positive space charge in the gate oxide and an increase in trapping states at the silicon-silicon dioxide interface. The resulting negative flat-band voltage shift changes the CCD operating bias while the interface state density increase reduces the charge transfer inefficiency in surface channel devices and increases the dark current density in both surface and buried channel structures. Consequently, non-hardened devices are unsuitable for most room temperature applications requiring a dose tolerance greater than 5×10^4 rads (Si). The details of these radiation induced failure mechanisms are presented in the following paragraphs.

Charge Buildup in the Oxide

For a given oxide technology, the smallest flatband voltage shifts are observed in n-buried channel and p-surface devices since the gate voltage in these structures is negative with respect to the channel potential. The effects of positive space charge buildup in the oxide on CCD operation will be discussed separately for the CCD input, charge transfer section and the output of the CCD shift register shown in Figure 1.
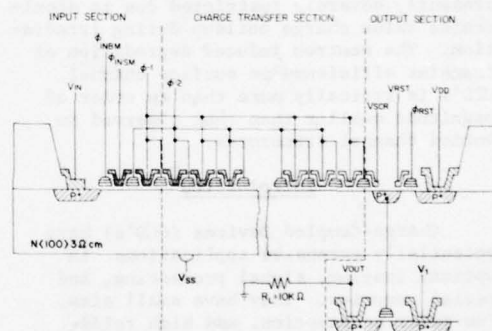
Fig. 1 Cross-section of a two phase p-surface channel CCD shift register. The device is shown separated into three sections: input, charge transfer section, and output.

The CCD input structure is the most radiation sensitive section of the device unless a threshold insensitive input is employed. MOSFET input techniques such as dynamic injection[2] which operate by leaking charge into a CCD potential well over the barrier formed by the input
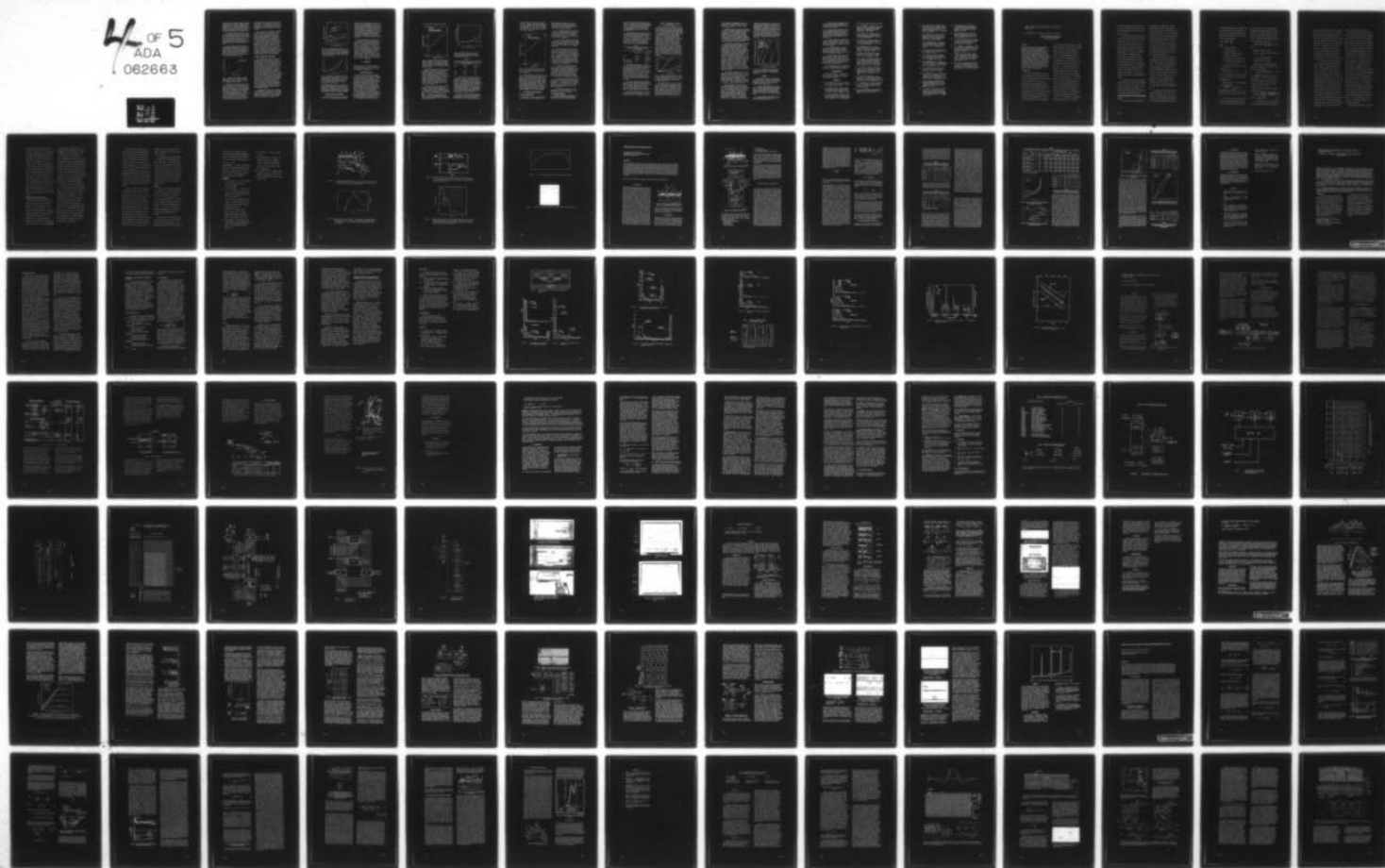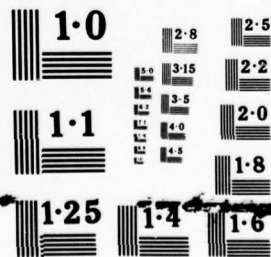
transfer gates, ϕ_{INBM} and ϕ_{INSM}, typically tolerate only 10^3 rads (Si) before requiring adjustment. However, threshold voltage shifts up to -5 volts have been accomodated by the input structure when the potential equilibration input, a threshold insensitive technique, was employed.[3]

The charge transfer process in a properly designed charge-coupled shift register is fairly insensitive to uniform transfer gate flatband voltage shifts.[4] However, gate to gate nonuniformities of the space charge buildup may distort the potential profile in the CCD channel with increased signal charge trapping as a result.

Unequal flatband voltage shifts on adjacent gates has also lead to severe loss in CCD signal handling capacity.[5] The difference in flatband voltage shifts between the aluminum and polysilicon CCD gates, shown in Figure 2, reduced the full well capacity to 20% of the irradiation value after 3×10^5 rad (Si).
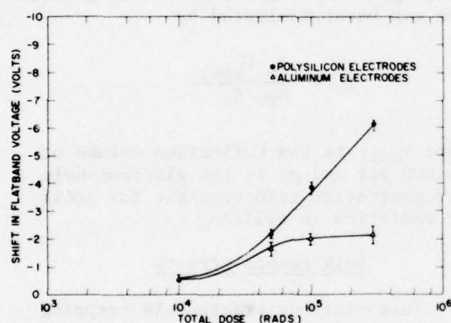
Fig. 2 Difference in flatband voltage shift for polysilicon (1,000 A° oxide) and aluminum (2,400 A° oxide) CCD gates as a function of total dose.

The radiation induced negative flatband voltage shift will cause the potential energy profile in the CCD channel to change in both surface and buried channel structures. Eventually the channel will be driven out of depletion in p-surface and n-buried channel devices. A few volts of flatband voltage shift accomodation can be obtained in an n-buried channel structure simply by applying a reverse bias to the reset drain voltage, V_{DD}, several volts in excess of the

pre-irradiation value required to deplete the channel. The flatband voltage shift tolerance of a p-surface channel device can be increased by either applying a positive substrate bias or a negative clock offset voltage.

The CCD output is the least radiation sensitive section of the device. The input and charge transfer sections will usually be severely degraded before the output becomes inoperable. The reduced radiation sensitivity of the CCD output can be attributed to the following: (1) The output MOSFET threshold voltage shift is smaller than the shift on the other CCD gates due to the reduced electric field strength in that oxide. (2) The output signal is AC coupled. Hence, small shifts in the DC operating point of the output transistor are of little consequence. (3) The output MOSFET is operated as a source follower. Therefore, the output gain will be relatively insensitive to radiation induced change of the transconductance.

Interface State Density Increase

The irradiation produced increase of trapping states at the silicon-silicon dioxide interface reduces the charge transfer efficiency in surface channel devices and increases the surface component of the dark current density in both surface and buried channel CCD structures. The increase in charge transfer inefficiency due to interface state trapping in surface channel devices renders them unsuitable for most applications after 10^5 rads (Si). Surface state trapping effects do not occur in a buried channel since the charge packet is transferred in the bulk of the silicon rather than at the silicon-silicon dioxide interface. A comparison of the transfer inefficiency as a function of dose for surface and buried channel devices is shown in Figure 3.[6] The small degradation of the transfer efficiency observed in the buried channel device after large doses is probably due to gamma induced bulk trapping effects.

Interface states also act as generation recombination centers for the surface component of the dark current. The linear relation between the dark current and the interface state density for an irradiated device is illustrated in Figure 4.[4]
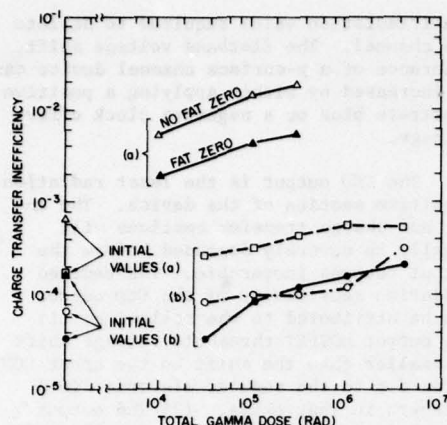
Fig. 3 Charge transfer inefficiency as a function of total gamma dose (a) for surface channel CCD's, (b) for buried-channel CCD's, illustrating the larger degradation observed in surface channel devices after ionizing radiation.
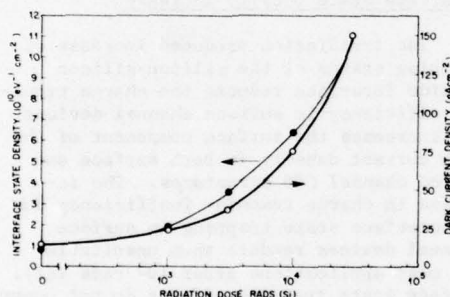
Fig. 4 Increase in interface state density and dark current density in a surface channel CCD as a function of dose. The data illustrate the linear relation between interface state density increase and dark current increase.

Dark current densities of $1,000 nA/cm^2$ have been measured after 10^6 rads in devices having a pre-irradiation value of $2 nA/cm^2$. Increases of this magnitude usually prohibit room temperature applications of unhardened devices after doses of 10^5 rads (Si).[6]

Transient Ionization Effects

Charge-coupled devices are extremely sensitive to transient-radiation induced

loss of stored information since they are very sensitive photosensors. The CCD potential wells are observed to fill with charge after a radiation pulse which deposits a dose on the order of one rad (Si) in a period which is smaller than the time a given potential well exists in the silicon.[7] The well saturation dose can be increased approximately an order of magnitude by reducing the thickness of the collection volume associated with each CCD bit.

In some applications the amount of time required to recover normal device operation after a radiation pulse is important. It has been observed that the excess charge generated in a CCD is removed at a rate which is a function of the CCD clock frequency, f_c, for a given dose.[8] Additional analysis indicates a recovery time dependence on CCD well capacity, N_{FW}, since the quantity of charge carriers transported out of a CCD during a clock period is limited by the well capacity. Hence, the CCD recovery time, T_R, after a pulse of ionizing radiation can be approximated by

$$T_R \simeq \frac{g_\gamma V_{coll}}{N_{FW} f_c}$$

where V_{coll} is the collection volume of one CCD bit and g_γ is the electron-hole pair generation rate constant for ionizing radiation in silicon.

Bulk Damage Effects

Fast neutrons create bulk trapping centers in silicon which cause a decrease in transfer efficiency primarily in buried channel devices and an increase in bulk component of the dark current density in both surface and buried channel structures. Increased trapping effects in neutron irradiated n-buried channel CCD's are usually insignificant for fluences less than $10^{11} n/cm^2$ ($\sim$ 15 MeV average).[9] The linear transfer inefficiency increase in the 10^{11} to $10^{13} n/cm^2$ fluence range is shown in Figure 5. After $10^{13} n/cm^2$ ($\sim$ 15 MeV average) the transfer efficiency at $295°K$ was reduced to 0.992, making the devices unsuitable for most applications. The degradation observed after 15 MeV neutron bombardment is expected to be 2.5 to 3 times greater than the value for a

1 MeV equivalent neutron fluence.[10]
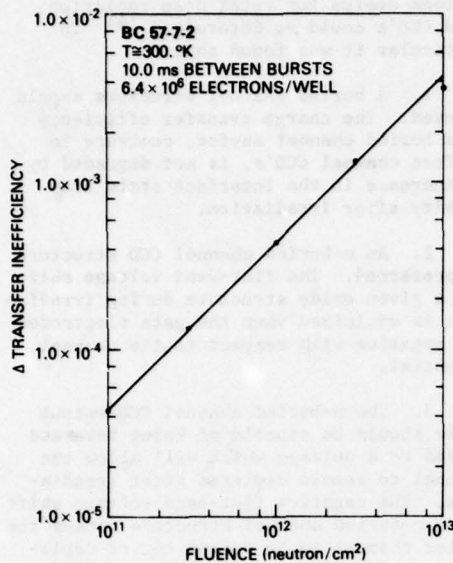
Fig. 5 Change in transfer inefficiency at 300°K as a function of 15 MeV (average) neutron fluence, illustrating the linear relation between the increase in transfer inefficiency due to bulk trapping and the neutron fluence.

Bulk traps are created during neutron bombardment in both surface and buried channel CCD structures. However, the volume occupied by a charge packet in a surface channel device is more than an order of magnitude smaller than the volume in a buried channel structure. Consequently, the transfer efficiency in a surface channel is less sensitive to increases in bulk trap density since the charge packets interact with fewer bulk traps. See Figure 6.[6]

Neutron irradiation produces several trapping levels of unequal density in silicon. Three distinct trap levels have been observed from 77°K to 300°K by use of the double pulse technique.[11] The energy level, (E_c-E_t), and the creation rate, $\left(\dfrac{\Delta N_t}{\Delta \phi}\right)$, of the bulk traps are given in Table I. Similar trapping levels have been observed in other types of irradiated silicon devices.[12]
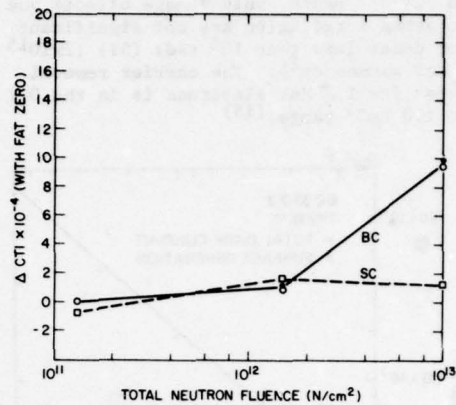
Fig. 6 Change in charge transfer inefficiency (CTI) with neutron fluence (1 MeV equivalent) for typical surface and buried-channel CCD's.

TABLE I

Bulk Trap Energy Levels and Creation Rates (15 MeV Neutron)		
Level	(E_c-E_t) eV	$\Delta N_t/\Delta\phi$ cm^{-1}
N-1	0.14	1.1
N-2	0.23	~ 0.8
N-3	0.41	7.0

The bulk trap level located near mid gap, $E_c-E_t = 0.41$ eV, acts as a bulk recombination generation center for dark current in both surface and buried channel devices. An approximate linear increase in dark current density in the 10^{11} to 10^{13} n/cm^2 range is shown in Figure 7 for an n-buried channel device.[9] The surface component of the dark current density did not increase since the total dose equivalence of the 10^{13}n/cm^2 fluence was only approximately 10^4 rads (Si).[13]

While 50% of the fast neutron energy is deposited in silicon via displacement damage, the fraction for gamma rays is much smaller. The bulk trap creation rate

for 1 MeV photon per cm^2 is only 1×10^{-3} cm^{-1}.[14] Hence, bulk damage effects due to gamma irradiation are not significant for doses less than 10^6 rads (Si) (2×10^{15} 1 MeV gammas/cm^2). The carrier removal rates for 1.7 MeV electrons is in the 0.2 to 1.0 cm^{-1} range.[15]
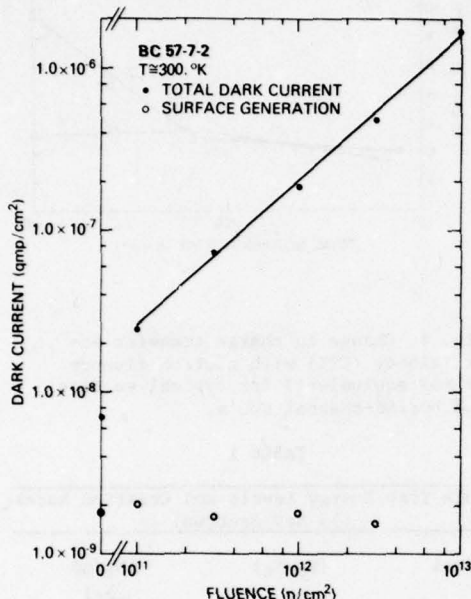
Fig. 7 Dark current density at 300°K as a function of neutron fluence, illustrating the linear relation between J_D and neutron fluence.

Little progress has been made in the area of neutron hardening of buried channel CCD's. An obvious technique would be to fabricate a thinner but more heavily doped buried channel so that the signal charge packet would interact with a small number of bulk traps, thereby reducing the transfer efficiency degradation. Another approach would be to fabricate the devices on Czochralski wafers since the neutron damage in oxygen rich silicon is smaller than the damage in float zone material.

CCD Surface Damage Hardening

Structural Optimization

The earliest work on total dose irradiation effects in CCD's identified the major failure mechanisms peculiar to several device structures so that the optimum design for total dose radiation hard CCD's could be determined.[4] In particular it was found that:

1. A buried channel structure should be used. The charge transfer efficiency in a buried channel device, contrary to surface channel CCD's, is not degraded by an increase in the interface state trap density after irradiation.

2. An n-buried channel CCD structure is preferred. The flat-band voltage shift for a given oxide structure during irradiation is minimized when the gate electrodes are negative with respect to the channel potential.

3. The n-buried channel CCD output diode should be capable of being reversed biased to a voltage which will allow the channel to remain depleted after irradiation. The negative flat-band voltage shift in an n-buried channel structure causes the buried channel to be driven out of depletion. A few volts of flat-band shift can be automatically accommodated by biasing the output diode to a value several volts in excess of pre-irradiation bias required to deplete the buried channel.

4. The design should use a planar channel insulator (no stepped oxide) and only one type of electrode material. This is necessary to eliminate differences in the flatband voltage shift under adjacent electrodes, since such differences can reduce or eliminate potential barriers which can result in reduced well capacity and increased charge transfer inefficiency.

5. The use of undoped polysilicon for interelectrode isolation should be avoided. Experience on two different types of device has shown that total doses of 1 to 3×10^4 rads (Si) cause channeling in the isolation regions with resulting deterioration in device performance.

6. The input structure should be compatible with the operation of a threshold insensitive input technique.

Hard Oxide Technology

Structural optimization alone is not sufficient to enable CCD's fabricated using standard gate oxide techniques to

satisfy the total dose radiation requirements for most space and strategic applications. The approach taken in the development of a radiation hard insulator for CCD's was to modify the process used in the fabrication of radiation hard CMOS devices.[16,17]

Both p-surface and n-buried channel shift registers have been fabricated using the CCD hard oxide process.[18] These devices can be operated after 10^6 rads (Si) with the pre-irradiation clock and bias voltages. The post-irradiation values for the n-buried channel device parameters, listed in Table II, are acceptable for most radiation environment applications.

TABLE II

Radiation Hard n-Buried Channel
CCD Parameters

	Pre-Irradiation	1×10^6 rads (Si)
CTE	0.99999	0.9999
J_D	$5 nA/cm^2$	$140 nA/cm^2$
Well capacity	$3 \times 10^6 e^-$	$2.25 \times 10^6 e^-$
Threshold shift	-	-1.8V

The transfer efficiency in surface channel devices fabricated with this radiation hard oxide was seriously degraded for doses greater than 10^5 rad (Si).[17] A severe increase in interface state trapping required the use of a 50% bias charge to obtain a transfer efficiency of 0.992 after 10^6 rads (Si). The dark current density and threshold voltage shift after 10^6 rads (Si) were approximately equal to the values observed in the buried channel structure.

It should be noted that the pyrogenic CCD hard oxide process described above is insensitive to total dose radiation effects only for negative gate to channel bias (i.e., p-surface channel and n-buried channel). The flatband shift for positive gate to channel bias can be quite large.

Bulk silicon damage effects in neutron irradiated radiation hard devices do not differ from those in unhardened structures.

Irradiation Effects at Cryogenic Temperatures

CCD's are being considered for use in space and infrared imaging systems both as infrared detectors and as signal processors for IR focal plane arrays at low-temperatures. However, several studies have shown that charge build-up in SiO_2 is more rapid in devices irradiated at low-temperatures.[19,20] Large flatband voltage shifts, are also observed during 77°K irradiation, in oxides which are radiation hard at room temperature.[21] The increased charge trapping effects at low-temperatures in the CCD radiation hard oxide, shown in Figure 8, make these devices unsuitable for most 77°K applications after a dose of 5×10^4 rads (Si).[22] Several techniques (alternate insulators, metal nitride oxide structures, and aluminum implanted oxides)[23] have been suggested for improving the low-temperature radiation behavior of MIS structures, but their use in CCD fabrication has not been reported.
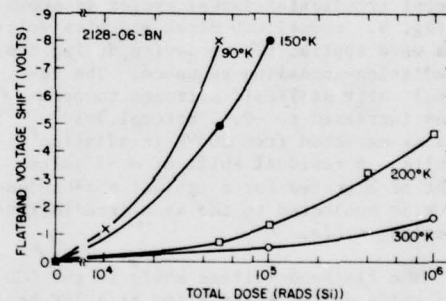
Fig. 8 Flatband voltage shift for the CCD radiation hard oxide as a function of dose at several temperatures, illustrating the increased oxide charge trapping effects at low-temperatures.

The holes generated in the oxide during a liquid nitrogen temperature irradiation are trapped almost immediately producing a nearly uniform density of positive charge in the oxide. The resultant flatband voltage shift is proportional to the oxide thickness squared and has a value of -2.0V per 10^4 rad (Si) for a 1,000 A° oxide if all the generated holes are trapped uniformly.[24] The fraction of the

holes trapped is independent of gate voltage polarity for small doses but is a function of the electric field strength in the oxide.[25]

Several techniques have been employed to anneal the excess flatband voltage shift observed in devices irradiated at low-temperatures. These include: photo-depopulation of the traps, field-aided emission of holes from traps and thermal annealing.[26] Room temperature radiation hard oxides show some recovery even at 85°K but the annealing process is accelerated at temperatures greater than 125°K.[27]

The excess low-temperature irradiation threshold voltage shift observed in the room temperature radiation hard CCD was annealed by warming the device to room temperature. After recooling to 85°K the CCD threshold voltage shift was approximately equal to the shift which would have been observed if the devices had been irradiated at 300°K and then cooled. The input gate threshold voltage shift for several irradiation-anneal cycles is shown in Fig. 9. Normal CCD clock and bias voltages were applied to the device during the irradiation-annealing sequence. The residual shift at liquid nitrogen temperatures increased to -0.5V after 1.3×10^5 rads as expected from 300°K irradiation results. A residual shift of ~ -5 volts might be expected for a typical non-hardened oxide subjected to the same irradiation-annealing cycle.

The flatband voltage shift in the CCD hard oxide during irradiation at 4.2°K has recently been found to be identical to the shift for 77°K irradiation.[28] Also, it has been shown that the MNOS approach offers considerable improvement in the radiation hardness of capacitors irradiated at 77°K.[29] This technique may be useful for radiation hard devices at 4.2°K.

The limited amount of experimental data available suggest that the permanent bulk silicon damage caused by fast neutrons in CCD's irradiated at 80°K and 294°K is similar.[9] The density and the energy of the N-1 bulk trap level created by the neutron bombardment was independent of irradiation temperature (80°K or 294°K) and irradiation bias for the particular devices tested. However, the transfer inefficiency in a buried channel device will change as the temperature is varied since the particular bulk levels responsible for signal charge trapping is a function of temperature. At 80°K the bulk level (N-1) dominating the transfer loss has an order of magnitude lower density than the level important for trapping at 300°K (N-3). Hence, the charge transfer inefficiency at 80°K after neutron irradiation is approximately an order of magnitude smaller than the values for 300°K that are shown in Fig. 5.
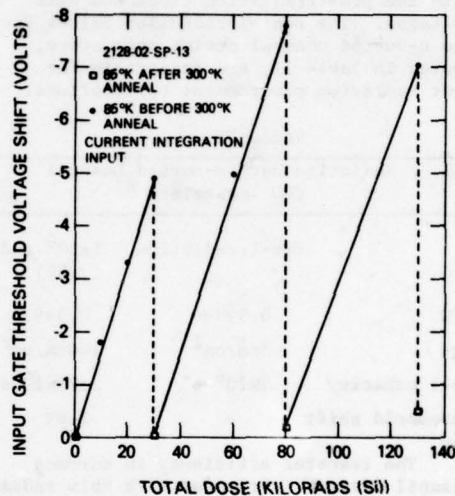
Fig. 9 Room temperature radiation hard CCD input gate threshold voltage shift at 85°K as a function of dose and 300°K annealing.

Summary

The previous sections of this paper have presented an overview of the current state-of-the-art of radiation effects and hardening techniques. The key points presented are listed below.

1. CCD's are sensitive to both surface and bulk damage effects due to radiation. Devices fabricated using standard commercial gate oxide technologies are unable to satisfy the total dose requirements for most space and strategic requirements.

2. An n-buried channel device is the least radiation sensitive structure for total ionizing dose effects.

3. The neutron induced degradation of the charge transfer efficiency is greater in buried channel devices than in surface channel devices.

4. Only a limited increase in the total dose radiation tolerance of CCD's can be achieved by means of structural and operational considerations alone. A radiation hard oxide technology is required to satisfy system radiation requirements.

5. CCD's are extremely sensitive to transient upset effects. Increased tolerance can be achieved by thinning. Device burnout is prevented by current limiting the power supplies.

6. An megarad-hardened n-buried channel hard CCD technology has been developed and simple linear radiation hard shift registers have been fabricated with the optimized structure.

7. Total ionizing dose effects are more severe for irradiation at 77°K. Ordinary room temperature radiation hardening techniques do not apply for irradiation at liquid nitrogen temperatures. However, several techniques have been proposed to solve this problem.

8. The degradation of CCD parameters in neutron irradiated buried channel CCD's are less severe at 77°K than at 300°K.

Acknowledgements

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A Bipolar Current Amplifier/Buffer Output for Very Small Geometry CCDs

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ABSTRACT

A reliable and sensitive charge detection scheme for very small charge packets is described. This scheme integrates a bipolar pnp device into the output gate of a CCD using one extra mask and two ion implants. The charge packet flows into the base causing a large emitter current flow in the bipolar device. This emitter current flows into the substrate. A simple analysis of the operation is presented. Trade offs of high β and low current β fall off are presented. Bipolar devices with β as high as 800 and base width of ~1500A have been fabricated. It is shown that good low current β fall off is more essential than high β. Finally various clocking schemes for this output are discussed.

INTRODUCTION

CCD's have now been established as a viable technology for memory applications. The trend towards higher density has resulted in very small geometry sizes and correspondingly small charge packets which must be transferred and detected reliably to meet the desired performance goals. The reliable detection of extremely small charge packets over a wide range of temperature and noise requires elaborate circuitry to provide the desired gain (viz regenerator circuits for 64k bit CCD memories). Charge detection schemes used with CCD's at present employ a capacitive voltage change of a floating node due to the signal charge packet. For small geometry CCDs (cell sizes of $\leq 50\mu m^2$) the charge packet size is decreased ($\leq 5 \times 10^{-15}$ coulombs) with a corresponding decrease of the output voltage swing. In this paper we describe a CCD output structure which utilizes a bipolar current amplification to achieve reliable detection of very small charge packets. The bipolar device is integrated at the end of the CCD channel. This structure is realized by adding one mask and two extra ion implantation steps at the end of the CCD process to fabricate a p^+ injector (emitter) and a non-depleted n-base region under it, at the output end of the CCD. The combination forms a vertical PNP structure with the substrate serving as the collector. The emitter

is biased through a depletion load, and its voltage is sensed through a source follower. The schematic diagram of this structure is shown in Figure 1.

When a charge packet flows into the base region of the PNP transistor, it turns on and draws emitter current which is β times the base current equivalent of the signal charge. This current gain allows a much larger drive capability. When the charge packet is annihilated by recombination in the base, the PNP transistor switches off and is automatically reset for the next charge packet. Contrary to floating node schemes, there is no precharging necessary and no clock feedthrough at the output when no charge packets are sensed in this mode of operation of the bipolar output detector. This feature is expected to result in reduced fixed pattern noise.

The capability of integrating bipolar buffer devices on the same chip as MOS/CCDs provides the current drive capability that allows this technology to compete with bipolar technologies for VLSI logic, memory and signal processing applications.

BIPOLAR OUTPUT CONCEPT AND DESIGN CONSIDERATIONS.

Figure 1 shows the cross-section of a

CCD channel which incorporates a bipolar charge detection element at the output. This detection element is shown for a buried channel CCD structure. It can in principle be used with both surface and buried channel CCD's. The two phase coplanar electrode [1,2] CCD shown in Figure 1 is representative of the CCD structure which was used to demonstrate the concept. The concept is by no means limited to this CCD structure and may be used with other two, three or four phase versions as well.

The bipolar element is fabricated at the end of the CCD process by opening a window in the polysilicon output gate electrode. The n-type base region implant is performed through the same opening. In principle, the lateral straggle of the implants [3] should be adequate to ensure that no emitter collector shorts occur at the edge of the window. To guarantee this, however, a low temperature heat step ($\leq 200°C$) may be used to flow the resist into the window to provide additional margin.

The detection scheme presented here is designed to operate at very low current levels. The effective base current into this device may be computed from the dynamics of a charge packet being transfered

into the base region through the output gate. It has been shown, [4] that the charge transfer in a CCD is approximately exponential and electrode has a time constant τ_f which may be described by

$$\frac{1}{\tau_f} = C_1^2 \frac{\pi^2 D}{4L^2} + \frac{\mu^2 E_y^2}{4D} \tag{1}$$

where

D = electron diffusivity

μ = electron mobility

L = length of the gate electrode

E_y = lateral fringing field

C_1 = a parameter that varies from 1 to 2 as the normalized fringing field varies from 0 to ∞.

The charge $Q_B(t)$ flowing into the base is represented as

$$Q_B(t) = Q_o A_{well} (1 - e^{-t/\tau_f}). \tag{2}$$

In this expression Q_o is the charge capacity per unit area and A_{well} is the area of the CCD storage well.

The base current in the bipolar device will then be given by

$$i_B = \frac{dQ_B(t)}{dt} = A_{well} \frac{Q_o}{\tau} e^{-t/\tau} \tag{3}$$

This exponentially decaying pulse of i_B is fed into the bipolar device which is normally off.

The transient response due to this current may be estimated from the charge control analysis of the bipolar transistor.

The charge packet will supply the base recombination, and charge the emitter and collector junction capacitance as well as the output gate capacitance connected to the base. The differential equation describing this process may be written as

$$\frac{d}{dt}(Q_B + Q_{Te} + Q_{Tc}) + \frac{Q_B}{\tau_B} + \frac{d}{dt} C_g v_{be} = -i_B \tag{4}$$

where

Q_B = base minority charge

Q_{Te}, Q_{Tc} = junction transition capacitance

C_g = output gate capacitance

v_{be} = base emitter voltage

Following the standard charge control treatment [5] equation (4) may be written for our configuration as

$$i_B = \left(\frac{1}{w_T} + \frac{1}{w_g} + \frac{C_L R_L}{\beta}\right) \frac{di_c}{dt} + \frac{i_c}{\beta} \tag{5}$$

where $w_g = \frac{g_m}{C_g}$ for the output gate and $w_T = 2\pi f_T$ where f_T is the short-circuit current gain bandwidth product. The collector resistance is assumed to be zero, and $C_L R_L$ represents the emitter load.

We may now solve (5) and (3) to obtain the emitter current as

$$i_e(t) = \beta Q_o A_{well} \left[\frac{e^{-t/\ell.c.}}{\tau_f + k\beta} - \frac{\{(\beta-1)\tau_f + k\beta\}}{\beta \tau_f (\tau_f + k\beta)} e^{-t/\tau_f} \right]$$

where $k = \left(\frac{1}{w_T} + \frac{1}{w_g} + \frac{C_L R_L}{\beta}\right)$. \hfill (6)

It is obvious from (6) that the emitter current provides a factor of β increase in

the charge available to drive the next stage. Alternatively, the load capacitance is now reflected to the base node as $\frac{1}{\beta}$ times what it would be in a simple precharge circuit. Base widths of ~1500Å, as fabricated in our structure, would lead to an w_T of much greater than 1GHZ. So, in typical layouts, the total effective node capacitance of this output device is dominated by the enlarged output gate needed to enclose the base structure. Hence frequency response of this output structure would be limited by the output gate.

In Figure 2(a) we show a theoretical evaluation of the emitter current waveform based on (6) for a charge packet size of ~1.6 fc. The assumed parameter values are shown in the figure. The simple theory presented here is compared also to a numerical simulation using SPICE circuit simulator and typical MOS parameters (Figure 2b). For the SPICE simulation we have used a simplified current pulse as the input and plotted the emitter voltage as the output. The emitter voltage follows the emitter current prediction of Figure 2(a) based on the charge controlled model. It has been assumed in this calculation that minimum geometry output gate node can be built. In practice the output gate capacitance is larger since it surrounds the bipolar. This will limit the turn off

characteristics of the bipolar device.

This application of the bipolar transistor as the output of the CCD shift register requires that the β fall off at low currents be minimized. It has been very well known that the low current β fall off is dominated primarily by injection efficiency considerations. The generation component of current in the emitter base depletion region and the surface recombination component play a very important role in the determination of the low current fall off characteristics of the bipolar transistor. The incorporation of a bipolar device in a CCD process has some very significant advantages. CCD's are built on (100) silicon to obtain low surface state density. Gettering sequences designed into the process allow very high bulk lifetimes to be achieved in processed devices [6,7]. Bulk lifetimes of ~1msec and surface recombination velocity of ≤ 1cm/sec have been measured in our devices. In addition Hansell and Fonstad [8] have shown that the β linearity at low currents is affected most significantly by decreasing emitter doping to take advantage of the increased mobility. They show that β at very low currents is obtained at the expense of the absolute β value.

We have fabricated bipolar structures

with a β of ~800 as well as those with ~100-150. The variations in β were achieved by varying the base implant dose. The typical implant distribution calculated for bipolar devices with β ~100-150 is shown in Figure 3. The estimated f_T of this pnp transistor from theoretical consideration is > 1GHZ. However, frequency response of the bipolar device by itself cannot be measured since it si integrated with a FET device at the base. The β vs. I_c characteristics of these devices is shown in Figure 4. For a typical charge packet size of ~4×10^{-15} coul. and a gate length of ~4μm the effective base current pulse is about 26nA. Thus for β ~ 100 the typical operating region is at I_c ~26μA. It is obvious from Figure 4 that our design for β ~100 has adequate low current β linearity.

OPERATION AS CCD OUTPUT AMPLIFIER.

The bipolar device concept and design discussed in the previous section may be operated in three distinct modes at the output of a CCD shift register. In the simplest mode the bipolar device is operated with a fixed emitter bias obtained through the depletion device which acts as an emitter load. In this mode, the charge packet turns on the bipolar as was described in the previous section, and a large current

gain is obtained. However there is no voltage gain available because the emitter voltage follows the base voltage. The effective charge to voltage ratio, of course, depends on the ratio of the net output node capacitance to the capacitance of a storage well. The use of the bipolar device provides an impedance transformation so that the load capacitance on the emitter node is reflected as a β times smaller capacitance at the base. Thus for a given load an effective increase in the net voltage swing may be obtained for a given charge packet size. This increase is partly offset, however, by the increased capacitance components due to base emitter capacitance of the bipolar device. The operation in this mode has the advantage of very low coupling of clocks and precharge pulses compared to a normal precharged output. A large current drive capability is obtained but the voltage swing is not significantly increased. We have found an effective current gain at the output of ~ β in CCD operation in this mode. Figure 5 shows the output of a CCD register and the input pulse. The input and output occur simultaneously by choosing the number of bits between input pulses to be equal to the length of the register.

The second mode of operation uses a dynamic emitter biasing or precharging of the emitter node before the charge packet flows into the base. In this mode the emitter is floating when the charge flows into the base and the transient emitter current proportional to $(\beta + 1)I_B$, produces a transient emitter voltage spike which may be much larger than ΔV_{be}. Thus a large transient voltage swing is available on the base which may be used as a latching signal. We have measured ~400mV signals on 4×10^{-15} coulomb of charge using this clocking scheme compared to 55mV output swing using the dc scheme.

The bipolar output may be operated in a non-destructive mode also. To achieve this, the device is built into one of the electrodes of the shift register. The charge packet flows into the base and remains there for the clock period. During this time the bipolar is turned on. The next phase clocks the charge out of the base into the next storage location. Thus the signal charge may be propagated after the read operation using the bipolar device. The signal charge used to provide the output signal corresponds to the fraction of the charge packet which recombines in the base during the read cycle. Since all base

charge does not have to recombine, this mode of clocking may provide an extremely high speed output.

The bipolar output scheme described in this paper has an added advantage for memory applications. The change in base voltage ΔV_{be} is proportional to the charge packet, and the collector current is proportional to $\exp(q \Delta V_{be}/kT)$. Thus for the second clocking scheme where the emitter is floating, the transient spike is exponentially proportional to the charge packet, so that a '0' and '1' can be very easily differentiated.

SUMMARY

A bipolar charge detection concept has been presented. It is shown that the concept may be implemented in a CCD process at the cost of one mask and two ion implants. Design considerations for this concept are presented. CCD shift registers have been fabricated to demonstrate the concept. It is observed that output voltage signals ~x8 greater than the conventional precharge techniques may be obtained.

The integration of the bipolar output provides the capability of driving large loads with a small charge packet. This buffer capability may also be utilized for

high off-chip drive capability, which coupled with the advantages nMOS/CCD provides a very high performance technology for logic, memory and signal processing.

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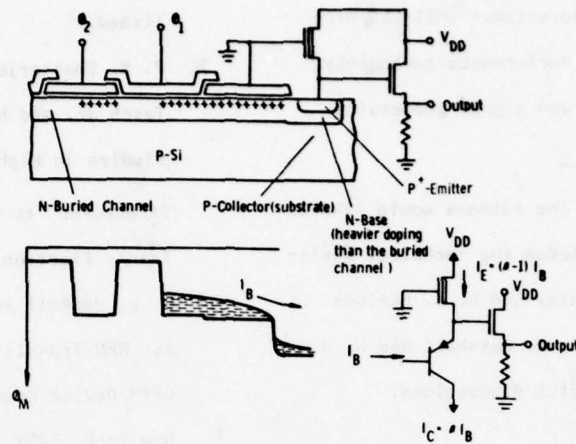
Figure 1   The structure and concept of the bipolar output for CCDs. The top figure shows the crossection of the output and the bottom shows the operation of this output scheme.
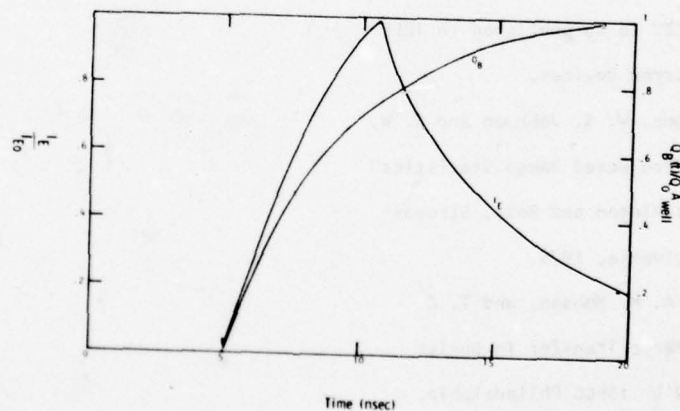
Figure 2(a) The emitter current response of the bipolar for a charge packet. The charge packet size ($Q_{well} A = 1.6$ fc) and the maximum emitter current is $i_{Eo} = 2.3\mu A$. The calculations are based on $\beta=100$ and $k=0.9$ nsec.
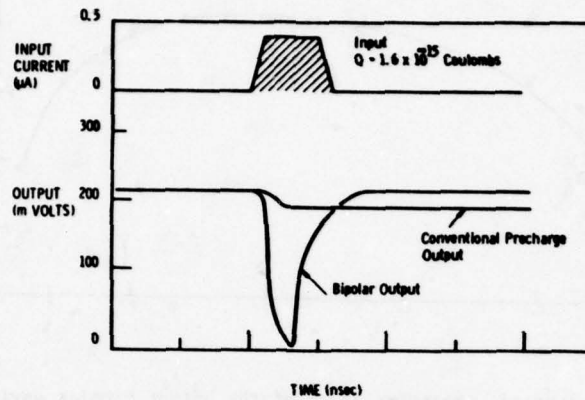
Figure 2(b) SPICE simulation of the bipolar output. The response to a
current pulse I$_B$ is shown. This simulation is more optimistic
than the charge control theory because default parameters for
the bipolar are used.
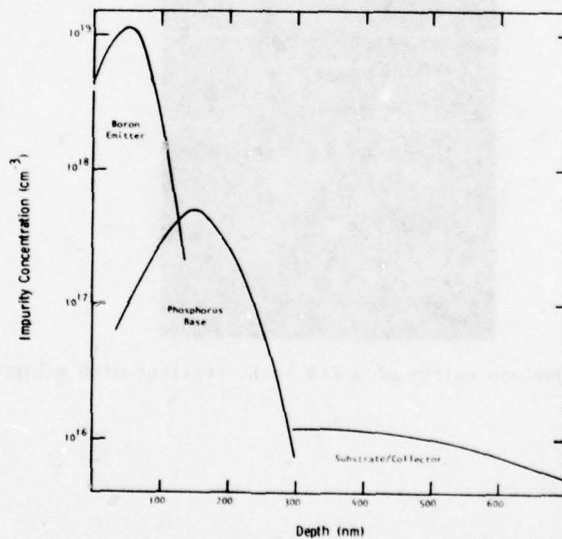
Figure 3   Doping distribution is due to the base and emitter ion implants
forming the pnp bipolar. The collector distribution is non-
uniform becuase of the channel implants required to avoid short
channel effects and punch through.

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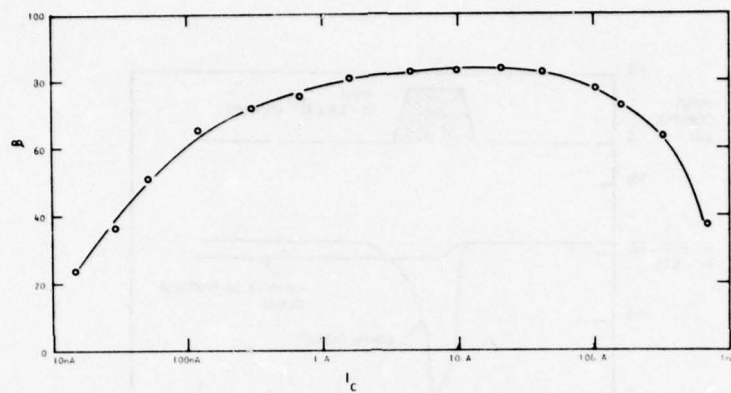
Figure 4   β vs. I_c characteristics of the output bipolar device.

Figure 5   Input and output of a CCD shift register with a bipolar output.

DEGRADATION ANALYSIS OF CCD'S*

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ABSTRACT

The effort reported in this paper concerns an experimental study of factors which influence the degradation of parameters and performance of analog charge-coupled devices. Measured parameters include charge transfer efficiency, dark current density, analog dynamic range, and full well capacity. Test cells of a p-surface channel device and an n-buried channel device were temperature-bias stressed for 1,000 hours with parametric measurements taken at time 0, 168, 500, and 1,000 hours. A total of 40 surface channel devices and 21 buried channel devices were tested. Dynamic and dc stresses were applied to separate test cells at temperatures of 125°C and 200°C. Results show an increase in dark current density for all SCCD's test categories and a decrease of transfer efficiency for both SCCD's and BCCD's under 200°C stress for 1,000 hours.

1.0 Introduction

The growing use of charge-coupled devices (CCD's) in systems for analog signal processing has generated a need to develop information on failure mechanisms that affect CCD structures. This paper reports the results of a temperature bias stress accelerated life testing experimental study aimed at revealing these failure mechanisms. Groups of 44-stage surface p-channel analog shift register CCD's (SCCD) and 455/910-stage bulk n-channel analog shift register CCD's (BCCD) were subjected to dc and dynamic electrical stress at 125°C and 200°C. The 44-stage devices were unscreened Westinghouse 7004 serial in-/serial out four-phase shift registers while the 455/910-stage devices were commercially available Fairchild CCD-321 serial in/serial out shift registers. Cross sections of these two devices detailing their structure are shown in figures 1 and 2.[1] The sample group sizes consisted of 10 devices each for the SCCD's and 7 devices each for the BCCD's. However, each BCCD had two separate 455-bit analog shift registers on a single chip and, therefore, provided data on two separate shift registers per device package. Electrical measurements were taken at time 0, 24, 168, 500, and 1,000 hours of stress time. An additional 500 hours of stress was applied to the 125°C dc n-channel BCCD test group for a total time of 1,500 hours under stress. Electrical measurements of the devices were
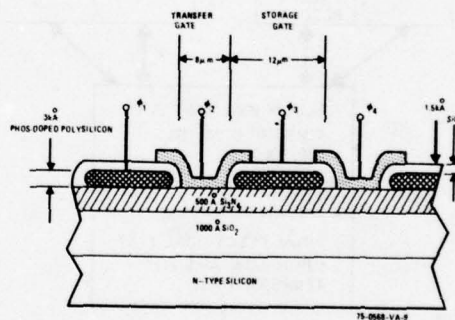
Figure 1. Cross Section of Aluminum/Poly Silicon Four Phase, Coplanar Electrode Configuration

made at room temperature with the precaution taken that devices were cooled to room temperature before electrical stress was removed. The experimental approach is summarized in figure 3.

2.0 Description

The dynamic stress consisted of the normally specified operating waveforms and bias voltage levels. The dc stress for the SCCD devices was −20 volts applied to the transfer gates with respect to the substrate with the input and output diodes back biased at the same voltage. In the case of the BCCD devices, the connec-
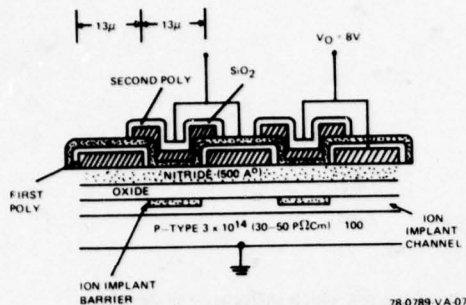
Figure 2. Cross Section of CCD-321 Structure

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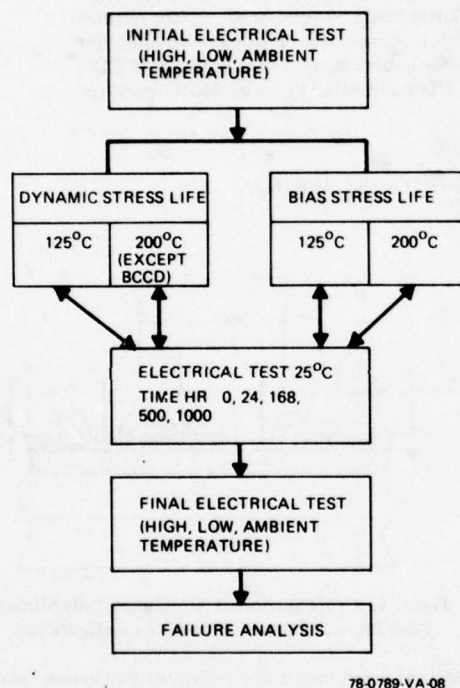
Figure 3. Life Test Plan for CCD Devices

tions were similar except that the initial positive dc stress applied to the transfer gates was 6 volts for the first 500 hours and then increased to 20 volts for the remaining 1,000 hours. Some of the electrical parameters measured were:

- Input Transfer Characteristics
- Full Well Capacity
- Dark Current
- Transfer Efficiency
- Insertion Loss
- Dynamic Signal Range
- g_m of Output Electrometer (SCCD's only).

Full well capacity is the maximum amount of signal charge which can be handled by a charge-coupled device. It was measured by the maximum output voltage difference between empty charge packets (when charge injection was cut off) and the largest charge packets the CCD can transfer when the output was saturated.

Dark current is the accumulation of additional carriers in potential wells from generation recombination centers found both in the bulk and at the silicon-silicon dioxide interface. The three major sources of dark current are thermal generation at the SiO_2-Si interface, thermal generation in the depleted bulk, and thermal generation in the nondepleted bulk within a diffusion length of the depletion region. This latter source is small compared to the former sources. The dark current density (or leakage current) can be expressed as:[2]

$$= (1/2)\pi k T q N_i V_{th} \sigma_S N_{ss} + (1/2) q N_i \sigma_D V_{th} X_d N_t$$

(1)

where σ_S and σ_D are the capture cross section of surface and bulk traps respectively, N_{SS} and N_t are the surface and bulk trap densities, x_d is the depletion width and V_{th} is the thermal velocity of carriers. Surface trapping states are distributed uniformly across the band gap and distributed in emission time constants. Bulk trapping states which contribute to dark current are discrete and located within ± 0.1 eV of the middle of the band gap.[3] The dark current degrades stored information with increasing time causing a nonuniform noise distribution in system applications in which the CCD clocks are not operating continuously or for signals which take different paths through the device to the output. In the case of continuous clocking, increased dark current reduces dynamic range. For the SCCD devices, the dark current density was determined by measuring the difference in reset current flowing to the charge collection diode with the shift register running in the forward direction and reverse direction, with no charge injected by the input structure. Using this procedure, all charge collected in the potential wells is due to dark current. In the forward direction, the dark current is delivered to the collection diode, while in the reverse direction it is swept away from the collection diode and therefore, only the output amplifier noise is present. The difference between forward and reverse

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clocking is the dark current. The BCCD device was not amenable to this measurement technique because charge transfer directivity is built into the structure during fabrication. The dark current measurement was made for the BCCD by first stopping the clock with one phase high for a period of time to collect leakage charge. After a suitable integration period the charge packets were then clocked at high speed to the output. The output waveform contained the signal voltage both with and without the leakage current integration. The voltage difference (ΔV) between the signal voltage, with and without integration, was due to the dark current. For readout times negligible to integration time ($> 10:1$) the dark current is related to the voltage difference by:

$$J_D = \frac{C_{out} \Delta V}{t\, A_{SF}} \qquad (2)$$

where C_{out} is the total CCD output load capacitance, A_{SF} is the source follower voltage gain, and t is the integration time.

Charge transfer efficiency (or its complement, charge transfer inefficiency) is an important measure of device performance for analog signal processing. Transfer inefficiency is due to the trapping of charge at either the SiO_2-Si interface or within the depleted bulk and/or insufficient transfer time. As clock frequency is increased, a break point is reached after which transfer inefficiency increases sharply because the time available for free charge transfer is reduced to the decay time constant associated with the longitudinal electric fringe field. The physical parameter which may change under stress which influences the decay time constant is the mobility of the carriers. A degradation in charge transfer efficiency in the clock frequency region in which free charge transfer effects do not dominate can result from the introduction of defects in the silicon, an increase in fixed charge loss and/or a change in the fixed charge density within the oxide. The first mechanism is manifested by an increase in interface or bulk trap density and/or a decrease in minority carrier mobility. The last mechanism is manifested by the trapping of electrons or holes in the oxide near the oxide-nitride interface necessitating a change in operating voltages for optimum performance. (This situation is undesirably from a user's viewpoint.) The effect of charge transfer inefficiency on the transfer function characteristics of serial in/serial out analog sampled data CCD's is given by the expression:

$$\frac{A_{out}}{A_{in}} = \left(\frac{g_m R_s}{1 + g_m R_s}\right)\left(\frac{C_m}{C_{out}}\right)\left(\frac{n^2}{1 + \epsilon^2 - 2\epsilon \cos(2\pi f/f_c)}\right)^{N/2}$$

$$k \text{ sinc } k; k < 1 \qquad (3)$$

where g_m is the transconductance of the output electrometer, R_s is the output electrometer source resistance, C_{in} is the effective input capacitance, and C_{out} is the output capacitance of the reversed biased readout diffusion. The term η is the charge transfer efficiency while ϵ is the charge transfer inefficiency defined as $\epsilon = (1-\eta)$. The term f is the input signal frequency, f_c is the clock frequency, N is the total number of transfers, and k is the ratio of signal output aperture time to clock period. The insertion loss, in dB, is then given by the ubiquitous relationship:

$$dB = 20 \log \left(\frac{A_{out}}{A_{in}}\right) \qquad (4)$$

for a specified input frequency, clock frequency and value of k. Insertion loss was measured experimentally using a spectrum analyzer. The expression used to calculate transfer efficiency from the experimental data is:[4]

$$\eta = (1-\epsilon) = 1 - \frac{L_L}{N-1+L_L} \qquad (5)$$

where L_L is the total loss in the leading edge of a string of pulses. This expression yields a value of transfer efficiency per transfer. The usual pulse measurement technique was used for all tests to obtain the data for transfer efficiency calculations.

Dynamic range was measured as the difference, in dB, between the fundamental tone output of the CCD and its second harmonic when the second harmonic power equaled the rms noise power output of the device. The measurements were made using a spectrum analyzer. The spectral content of the noise was predominantly white with little contribution to total noise power due to 1/f noise for both groups of CCD's tested.

All measurements presented in the tables were made at a clock frequency of one MHz. A frequency of 0.225 MHz was used for the test signal while making insertion loss and dynamic range measurements.

3.0 Experimental Results and Discussion

A summary of the test data is presented in tables 1 through 6 and figures 4 through 7. Each data value in

the tables represents the mean and standard deviation of 10 measurements (10 devices) per category for the SCCD's and 14 measurements (7 devices) per category for the BCCD's. The g_m of the output transistor for the SCCD's was measured initially and at the end of stress testing, and was essentially unchanged. The output amplifier of the BCCD was not available for separate measurement of its g_m. Referring to table 1,

Table 1
Full Well Voltage Variation Over 1,000 Hours of Stress (Measurements Made at Room Temperature)

Device Type	Voltage Stress	Stress Temperature	Full Well Voltage			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	0.66	0.14	0.58	0.08
SCCD P-Channel	dynamic	125°C	0.59	0.09	0.61	0.11
SCCD P-Channel	dc	200°C	0.57	0.11	0.57	0.11
SCCD P-Channel	dynamic	200°C	0.58	0.11	0.59	0.08
BCCD N-Channel	dc	125°C	1.83	0.13	1.84	0.13
BCCD N-Channel	dynamic	125°C	1.78	0.14	1.78	0.14
BCCD N-Channel	dc	200°C	1.75	0.14	1.94	0.13

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no significant change in full well capacity was observed for either the SCCD's or the BCCD's under stress testing except the BCCD 200°C dc test group showed an increase in capacity of 11 percent. Tables 2 and 3

Table 2
Dark Current Variation Over 1,000 Hours of Stress Testing (Measurements Made at Room Temperature)

Device Type	Voltage Stress	Stress Temperature	Dark Current nA/Square Cm			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	118/31*	234/11*	80	40
SCCD P-Channel	dynamic	125°C	30	9	1825/194*	2893/138**
SCCD P-Channel	dc	200°C	55	45	122	94
SCCD P-Channel	dynamic	200°C	44	35	204	121
BCCD N-Channel	dc	125°C	37	25	44	32
BCCD N-Channel	dynamic	125°C	73	64	57	61
BCCD N-Channel	dc	200°C	34	16	47	20

*Data with all sample values/data with two of ten samples deleted.
**Data with all sample values/data with three of ten samples deleted.

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give the test data results for dark current and transfer efficiency for the various stress categories. The data shows a uniform trend towards increased dark current with temperature stress for all SCCD test categories. A constant ratio difference of the initial and final measurements between the dynamic and dc stress SCCD categories can also be determined from the data with the dynamic category always the larger. A possible explanation is that for the dc stressed devices the entire voltage drop occurred across the gate oxide

because the surface was inverted. On the other hand, the devices stressed with dynamic voltages had a depleted region at the silicon surface over which some voltage drop occurred. An increase in leakage current of MOS devices has been shown to be caused by an increase in fast interface state density and fixed positive charge when stressed with temperature and dc bias.[5] A change in interface state density would also manifest itself as a decrease in charge transfer efficiency. Although a marked decrease in CTE was observed for the 200°C SCCD test categories, a similar decrease was not observed for the 125°C SCCD test categories although their leakage current did change appreciably. Table 6 shows the data representing the CCD input gate "threshold" voltage for the SCCD test categories. (This measurement is not analogous to the usual threshold measurement of MOSFET's but does give some information on fixed charge in the oxide.) The data shows a larger degradation for dynamic stressed devices than for dc stressed devices. In an attempt to separate degradation effects due to changes in carrier mobility and interface state density, the transfer inefficiency was measured as a function of clock frequency for pulse waveforms with 10 percent bias charge and then as a function of time between pulses without bias charge (the so-called double pulse technique).[6] The results of the first measurements are shown in figure 4 for selected SCCD's. The characteristic break point occurs at roughly the same clock frequency for all categories implying that minority carrier mobility does not change radically.

The results of the double pulse experiment for selected SCCD's are shown in figure 5. Comparison of these graphs for the 200°C and 125°C categories show a change in slope on the order of ~ 2 which represents a factor of two increase in interface state density. Comparison of the initial and final transfer efficiency for the 125°C and 200°C test categories show that this factor of two increase in interface state density reasonably explains the difference in values. Although the factor of two also causes a proportional increase in leakage current which is reasonably consistent with the 125°C and 200°C dc SCCD stress results, the factor of approximately four change for the leakage current in the 125°C and 200°C dynamic SCCD stress categories cannot be readily explained by the data shown in figure 5. The data in tables 3 and 4 show that neither the dynamic range nor the insertion loss changed dramatically for any of the SCCD test categories. Although the CTE did change substantially for 200°C stressed SCCD's, the devices are only 44 stages which is to short to impact insertion loss and dynamic range.

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Table 3
Transfer Efficiency Variation Over 1,000 Hours of Stress Time (Measurements Made at Room Temperature)

Transfer Efficiency per Transfer

Device Type	Voltage Stress	Stress Temperature	Initial				Final			
			0% F.Z.		10% F.Z.		0% F.Z.		10% F.Z.	
			Mean	S.D.	Mean	S.D.	Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	0.9986	0.0005	0.9994	0.0003	0.9983	0.0005	0.9994	0.0003
SCCD P-Channel	dynamic	125°C	0.9990	0.0005	0.9995	0.0006	0.9979	0.0010	0.9993*	0.0003*
SCCD P-Channel	dc	200°C	0.9984	0.0007	0.9994	0.0005	0.9966	0.0018	0.9984	0.0011
SCCD P-Channel	dynamic	200°C	0.9990	0.0003	0.9997	0.0001	0.9970	0.0014	0.9982	0.0013
BCCD N-Channel	dc	125°C	0.9990	0.0002	0.9999	0.0000	0.9987	0.0002	0.9999	0.0001
BCCD N-Channel	dynamic	125°C	0.9991	0.0002	0.9999	0.0000	0.9989	0.0001	0.9999	0.0000
BCCD N-Channel	dc	200°C	0.9991	0.0002	0.9999	0.0000	0.9953	0.0006	0.9968	0.0004

*Data with three of ten samples deleted
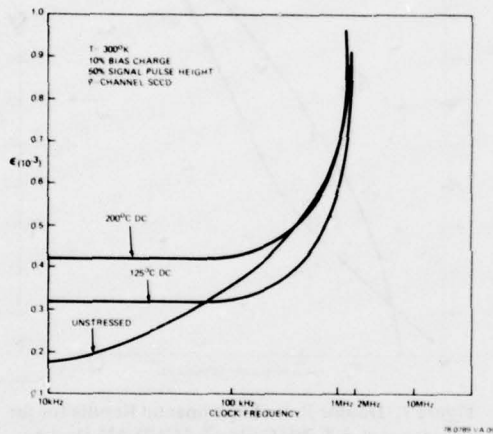
Figure 4. Surface Channel CCD Transfer Inefficiency as a Function of Clock Rate
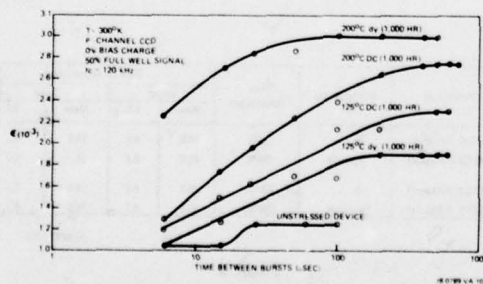
Figure 5. Double Pulse Measurements for Stressed and Unstressed SCCD's

Device Type	Voltage Stress	Stress Temperature	Insertion Loss dB			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	-25.9	1.3	-29.0	1.4
SCCD P-Channel	dynamic	125°C	-26.1	2.1	-25.7	1.4
SCCD P-Channel	dc	200°C	-26.1	1.7	-26.4	1.8
SCCD P-Channel	dynamic	200°C	-25.6	1.1	-26.8	3.0
BCCD N-Channel	dc	125°C	-13.7	0.5	-11.6	1.0
BCCD N-Channel	dynamic	125°C	-13.6	0.5	-12.1	1.2
BCCD N-Channel	dc	200°C	-13.7	0.5	-31.2	5.0

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Table 4
Insertion Loss Variation Over 1,000 Hours of Stress Time (Measurements Made at Room Temperature)

The experimental results for the BCCD do not lend themselves to easy physical interpretation. Although the device is a buried channel CCD, the data given in table 3 shows a marked improvement in transfer efficiency with the addition of a bias charge. The devices use an n+ floating diffusion for making several corner turns in the shift register. This corner turn technique has been modified by the manufacturer in later generations of the device type with the reported result that excellent transfer efficiency is achieved without bias charge.[7] Unlike the SCCD, there is no consistent increase in leakage current for the BCCD stressed devices. However, a substantial degradation in transfer efficiency occurred in the 200°C group. This loss in transfer efficiency could not be compensated by an increase in bias charge or by increasing or decreasing the clock voltages. Transfer efficiency measurements made as a function of frequency are shown in figure 6 for an unstressed device and the mean of all 200°C stressed devices. Differences are clearly apparent between the two 455-bit shift registers on the same device for the 200-degree dc results as well as a general shift of the break point toward lower fre-
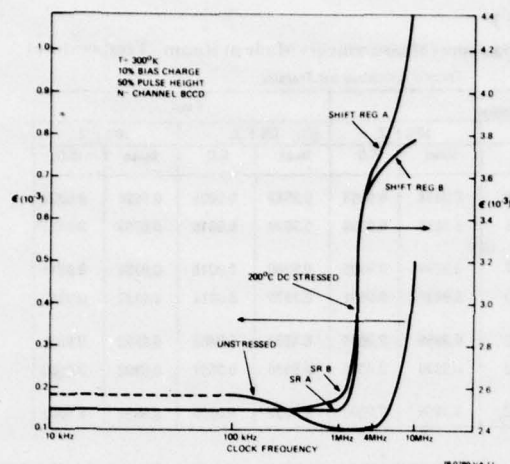
Figure 6. Transfer Efficiency versus Clock Frequency for BCCD's

quencies. The double pulse results for a single 200°C dc stressed device and an unstressed device are presented in figure 7. The shape of the curves for the unstressed device is consistent with measurements made by others of BCCD's[8][9][10] implying a single level of mid-gap electron trap states. However, the 200°C dc stressed curve is essentially different showing a peculiar twist at ~800 μsec which may be caused by multiple trap levels. Such traps, if not near the middle of the band gap, would not contribute to dark current but would contribute to a decreased CTE. Because of the poor transfer efficiency of the device, it was not possible to make meaningful measurements below 20 μsec at room temperature. Therefore, it has not been determined if the 200°C dc curve melds into the unstressed curve as the time between bursts goes to zero. If they do meld together, the observed loss in CTE for the 200°C category is due to other fixed charge losses than to bulk traps. Such other charge loss can be due to changes in the potential profile and/or loss out of the channel. The degradation in insertion loss and dynamic range for sinusoidal signals shown by the data in tables 4 and 5 for the 200°C dc BCCD stress category is consistent with the decreased transfer efficiency of these devices.

An Arrhenius relationship can be used to relate stressed measurements to degradation rate at room temperature. Assuming a thermal activation energy of 1 eV (a reasonable choice for silicon MOS devices) and screening devices that succumb to infant mortality, room temperature devices would degrade to the final values measured at 125°C after 8.54 x 10[4] hours and to the final values measured at 200°C after 5.13 x 10[6] hours.

Table 5
Dynamic Range Variation Over 1,000 Hours of Stress Time (Measurements Made at Room Temperature)

Device Type	Voltage Stress	Stress Temperature	Dynamic Range dB			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	43.0	1.3	40.2	1.7
SCCD P-Channel	dynamic	125°C	44.0	1.9	45.0	3.7
SCCD P-Channel	dc	200°C	43.7	3.9	39.6	5.1
SCCD P-Channel	dynamic	200°C	44.2	1.3	44.6	0.9
BCCD N-Channel	dc	125°C	47.3	1.3	53.1	2.1
BCCD N-Channel	dynamic	125°C	47.6	1.2	51.5	0.9
BCCD N-Channel	dc	200°C	45.0	3.1	27.0	5.0

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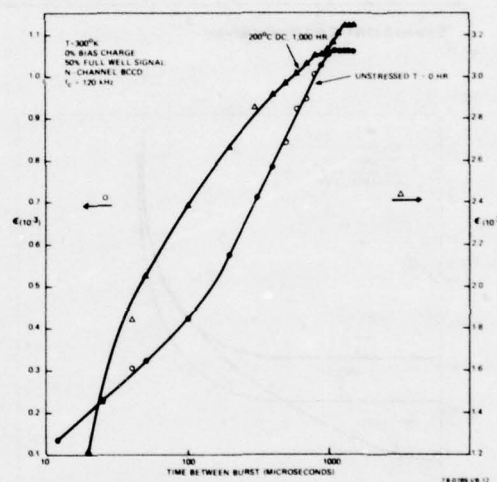
Figure 7. Double Pulse Experimental Results for the Unstressed and 200°C Stressed CCD-321 Devices

Device Type	Voltage Stress	Stress Temperature	Gate Threshold (volts)			
			Initial		Final	
			Mean	S.D.	Mean	S.D.
SCCD P-Channel	dc	125°C	14.9	0.2	14.9	0.1
SCCD P-Channel	dynamic	125°C	15.6	0.6	14.7	0.3
SCCD P-Channel	dc	200°C	15.6	0.2	15.0	0.2
SCCD P-Channel	dynamic	200°C	15.6	0.2	14.8	0.1

78-0789-TA-6

Table 6
Input Gate "Threshold" Voltages for the SCCD Test Categories (Measurements Made at Room Temperature)

4.0 Conclusions

The results of temperature bias stress of p-surface channel CCD's and n-buried channel CCD's have been presented. A basic trend towards increased dark current and decreased charge transfer efficiency in the SCCD devices can be attributed to an increase in interface state density. A result of the stress testing on SCCD's is that dynamic testing appears to degrade parameters faster than dc stressing. A decrease in charge transfer efficiency under 200°C stress for 1,000 hours for the BCCD remains unexplained with the data currently available. The room temperature operating time necessary to achieve the worst case values is in excess of 5×10^6 hours.

Acknowledgement

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CHARACTERIZATION OF LEAKAGE CURRENT WITH PHOSPHORUS GETTERING IN CHARGE COUPLED DEVICES

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ABSTRACT. Gettering is a process designed to remove from a silicon wafer impurities and structural defects which can act as generation-recombination centers and so cause reduced lifetime and increased leakage. In an oxide-isolated double-polysilicon gate surface p-channel CCD process, gettering is performed at the same time that the polysilicon layer is doped with phosphorus. The gettering effectiveness of the phosphorus is dependent on the temperature of the phosphorus deposition to take advantage of the increased phosphorus solubility limit at higher temperatures. The phosphorus deposition temperature employed for the gettering comprised of 925, 975, and 1025°C. Also included were a group of control wafers with no phosphorus gettering.

The effectiveness of gettering was determined by performing leakage measurements on 128-bit CCD shift registers so that results obtained from more than 1,000 devices were found to be significant to a confidence level of greater than 99.9%. Also, leakage in CCD shift registers as a function of temperature and reverse substrate bias variations were also obtained.

Gettering experiment results produced three main conclusions: (a) gettering reduces average leakage on all wafers, (b) the wide variation of leakage generation of ungettered wafers is dramatically reduced, and (c) gettering at higher temperatures leads to lower leakage and narrower distribution of leakage.

INTRODUCTION

A critical parameter affecting the yield of large scale charge coupled devices for memory and imaging arrays is the leakage current density associated with each cell of the array[1]. Leakage current generation produces erroneous data in CCD memories by generating a ONE instead of a ZERO in the data pattern. In CCD imaging applications, leakage current manifests itself by blooming and streaking in the video output signal [2].

Leakage current generation is dominated by oxidation-induced and bulk stacking faults where heavy metals precipitate [3],[4]. Several techniques for reducing these stacking faults have been investigated [2],[5],[6]. One of the easiest to implement is the technique of phosphorus gettering[2]. Consequently, fabrication procedures were developed to minimize leakage current generation by optimizing the phosphorus gettering process.

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PHOSPHORUS GETTERING

Gettering is a process designed to re-move from a silicon wafer impurities and structural defects which can act as gener-ation-recombination centers and so cause reduced lifetime and increased leakage[6]. Heavy metal ions are known to precipitate in the vacancy structure associated with dislocations, stacking faults, and other material imperfections. These heavy metal ions are nearly all interstitial diffusers, and so, if a sink for them can be formed on the back of the wafer, they can be effectively removed from the active surface of the wafer during reasonably short diffu-sion times. One way of doing this is to diffuse phosphorus into the back of the wafer[5], leaving a layer of silicon oxide heavily doped with phosphorus on the back. Such a glass layer is molten at moderate temperatures and becomes a sink for the metal ions. A heat treatment at the temper-ature at which this glass is molten can, therefore, getter impurities. It is also shown that gettering occurs in a region of strain on the back of the wafer[6] because the very high concentration of vacancies in the strained region provides a concentration gradient of impurities away from the active surface. Because high phosphorus concen-trations cause high strain in the silicon lattice, phosphorus gettering may be effective by both mechanisms under favorable circumstances.

In an oxide-isolated CCD double-polysilicon gate surface p-channel process, phosphorus gettering can be formed at the same time that the second polysilicon-layer is doped with phosphorus. Thus, gettering is done as late as possible in the process; i.e., during the last high temperature step. The oxide is stripped from the back of the wafers so that this phosphorus is diffused into the wafers from the back as well as into the polysilicon on the front. This causes both strain and a phosphorus-glass layer on the back of the wafer. This glass layer maintains the high concentration of phosphorus in the back of the wafer during subsequent heat treat-ments.

A layer of silox is deposited on the backside phosphorus glass to prevent its removal during subsequent etching steps. By retaining the phosphorus glass on the wafer back, the phosphorus concentration will be maintained at (or close to) its solubility limit at the surface in spite of subsequent diffusions. It is expected that the considerable lattice strain produced by phosphorus in the back of the wafer will provide a high concentration of vacancies which may act as a sink for interstitially-diffusing metallic impurities known to give rise to recombination-generation centers in silicon. Such impurities, then, may be "gettered" from the front of a wafer, where the active device regions are located, and immobilized in the back.

The gettering effectiveness of phos-phorus is expected to be dependent on the density of vacancies in the wafer back. More strain, and, therefore, (presumably) more vacancies, can be produced by increasing the phosphorus concentration in the wafer. This is most conventiently done by increasing the phosphorus deposition temperature to take advantage of the increased phosphorus solu-

bility limit at higher temperatures (at least in the temperature range under consideration).

EXPERIMENTAL INVESTIGATION OF PHOSPHORUS GETTERING

An experiment was designed to investigate and optimize phosphorus gettering procedures. The main parameter available for changing either the strain in the wafer or the phosphorus density is the temperature at which phosphorus gettering is performed. Because temperature controls the solid solubility of the phosphorus in the silicon, it, therefore, controls its concentration in the wafer. Accordingly, the phosphorus gettering process incorporates four variations: Control wafers (no phosphorus gettering) and gettering with phosphorus deposition temperatures of 925, 975 and 1025°C. Each group consisted of six wafers.

FABRICATION TECHNIQUE

A summary of the oxide-isolated *double* polysilicon processing sequence is as follows:

a. Starting silicon substrate <100>, 3 ohm-cm, n-type Czochralski.

b. Si_3N_4 deposition, delineation, field implant.

c. Local field oxidation

d. Gate oxidation

e. Polysilicon deposition and delineation.

f. Threshold shift implant

g. Second gate oxidation

h. Polysilicon deposition and delineation.

i. Contact mark and etch

j. Aluminum metallization, mark, and etch.

h. Anneal

A cross-section of the device is depicted in Fig. 1.

TEST PROCEDURES

The effectiveness of gettering was determined by making measurements on a 2-phase 128-bit CCD shift register. The clock frequency was found at which an empty bucket would become one-third full during the total time it was being clocked through the register. This clock frequency is a direct measure of the average rate, r, of charge generation in the register, since $r=Q/t_d$, where Q is that charge required to fill one-third of a bucket and t_d is the delay time through the register. Since $t_d=n/f$, where n is the number of bits and f is the clock frequency, then $r \propto f$. Note that this technique does not distinguish between high background generation rates, and low background with localized highly-generating point defects, but rather provides an overall average leakage density. The leakage current density, J_L, is related to the clock frequency, f_L, at which the bucket becomes one-third full by

$$J_L = \frac{C_{out} V_{out}}{A_{BIT} A_V \left(\frac{1}{f_L} - \frac{1}{f_H} \right) n} . \tag{1}$$

where C_{out} is the total capacitance at the output floating diffusion node, A_V is the gain of the source follower, A_{BIT} is the area where charge generation exists, n is the number of bits in the shift register, f_H is the high clock frequency of CCD operation, and V_{out} is the increase in output voltage due to charge generation at frequency f_L.

A different test procedure[1] is employed to separate leakage spikes and back-

ground leakage density. The clocks are stopped or held for a period of time Δt. In this manner, charge is collected during the time Δt and then clocked out of the shift register. Clocking the data out serially provides an output signal proportional to the leakage current at the appropriate cell locations. Thus, non-uniformity and spike leakage current density are obtained. In this case, the leakage current density is given by

$$J_L' = \frac{C_{out} V_{out}}{A_{BIT} A_V \Delta t} \qquad (2)$$

where Δt is the shift register holding time. The above methods were examined and result in excellent agreement. The former method has the advantage of providing fast discernable data without excess data reduction and was used throughout the data gathering process. As noted before, each group comprised six wafers, providing a total of 1072 CCD shift registers for subsequent evaluation. Results are statistically significant to a confidence greater than 99.9%.

RESULTS

Experimental results are summarized in two histograms given in Fig. 2. Fig. 2(a) shows results from 17 wafers which were gettered and includes 640 measurements on individual registers. The histogram of Fig. 2(b) shows results from six non-gettered wafers, including measurements on 432 registers. Note that one block on the histogram is 1 KHz wide. There are no values above 5 KHz from the gettered wafers, but about 27% of the distribution for the controls is above 5 KHz. The primary conclusion is that, of the two groups, the

gettered wafers have significantly less leakage. The distribution in Fig. 2(b), however, is strongly bimodal because the six ungettered wafers themselves fall into two quite distinct groups.

Fig. 3 shows two histograms: Fig. 3(a) for wafers #24, 25, and 26, and 3(b) for wafers #27, 28, and 29. Each block is 10 KHz wide. Note that the results in Fig. 3(a) are wholly contained in the 0-10 KHz block, but that 48% of the results in 3(b) lie above 10 KHz. Figs. 4 and 5 contain the same data as in Fig. 3, but are replotted with expanded abscissa scales so that the detail of these distributions may be seen.

If Figs. 2(a) and 4(a) are compared, it is seen that the "good" ungettered wafers #24, 25, and 26 are not much worse than the total gettered wafer population. However, the difference between the mean of the "good" ungettered wafers of 0.76 KHz and that of the gettered wafers of 0.46 KHz is statistically significant to a confidence level greater than 99.9%.

The question arises, would the three "bad" ungettered wafers, #27, 28, and 29 have improved if they had been gettered? Fig. 6 shows separate histograms of these three wafers. It is seen that these wafers have different characteristics, and, in particular, wafer #28 is closer to the group of "good" ungettered wafers than it is to the other two wafers in the "bad" group. It is at least arguable that wafers in the large batch from which those for this experiment were selected are extremely variable in the sense of their leakage

characteristics after processing, as evidenced by the six ungettered wafers. It is unlikely that wafers #26, 27, and 29 were the only ones out of the sample size of 24 that were bad (based on the criterion of this experiment). With no bad wafers occurring in the group of seventeen which were gettered, we may plausibly conclude that gettering can effectively reduce the very high leakage resulting from the wafers which fall into the "bad" classification.

Fig. 7 shows histograms of the three experimental groups of gettered wafers, i.e., those gettered at 925, 975, and 1025°C. The mean frequencies for these groups are 0.48, 0.50, and 0.38 KHz, respectively. There is no difference between the results at the temperatures of 925 and 975°C, but the difference between the results at these temperatures and those at 1025°C is statistically significant to a confidence level greater than 99.9%.

The effect of gettering at the various temperatures may be seen by listing the means of the frequencies for each wafer in their appropriate groups. This is done in Table 1, where wafers are listed in order of increasing mean value.

A summary of the above results is presented in Fig. 8, where leakage current density is plotted for each gettering group. The control wafers are shown to have two distinct categories: One having an average leakage current density of about 28 nA/cm^2 and the other 266 nA/cm^2. The group gettered at 925°C has four wafers with an average of about 16 nA/cm^2 and one wafer out of proportion. A similar case exists for

975°C gettering. The 1025°C gettered wafers, however, have an overall tight distribution with an average of 12 nA/cm^2.

TEMPERATURE AND REVERSE SUBSTRATE BIAS CHARACTERIZATION OF CCD LEAKAGE CURRENTS

The leakage current of the 128-bit CCD structures were characterized as a function of temperature and reverse substrate bias. In the investigation, spike leakage was also included to determine its variation with temperature and reverse substrate bias. In order to distinguish between background and spike leakage, the technique described earlier, employing clock disabling for a time Δt, was used.

Results are shown in Fig. 9. Normal operating conditions employ a +5 volt reverse substrate bias, V_{ss}. When V_{ss} is increased to +12 volts, both spike and background leakage increase by a factor of about 2.3. The depletion layer increases by a factor of 1.2, thereby contributing to the bulk leakage term. This implies that the remainder of the leakage is probably surface generated. This is demonstrated by temperature characterization of the devices. Measurement of leakage current versus temperature indicated that as temperature is increased to 65°C, the slopes for several values of V_{ss} are relatively constant, indicating that spike and background leakage both increase at approximately the same rate (viz., doubling every 10 degrees). In this temperature range, the leakage generation rate is dominated by an activation energy of 0.59 eV and is probably due to surface induced leakage[7].

CONCLUSIONS

The experimental evaluation of phosphorus gettering has produced the following results:

(i)   Gettering reduced the average leakage for all wafers.

(ii) The wide spread of leakage generation in ungettered wafers is dramatically reduced.

(iii) Gettering at higher temperatures leads to lower leakage and a tighter distribution of leakage.

Temperature characterization has shown that spike and background leakage increase with temperature at the same rate and, thus, have the same activation energy of about 0.59 eV. The substrate bias characterization has shown that both bulk and surface leakage generation occur and that the latter is dominant.

ACKNOWLEDGMENTS

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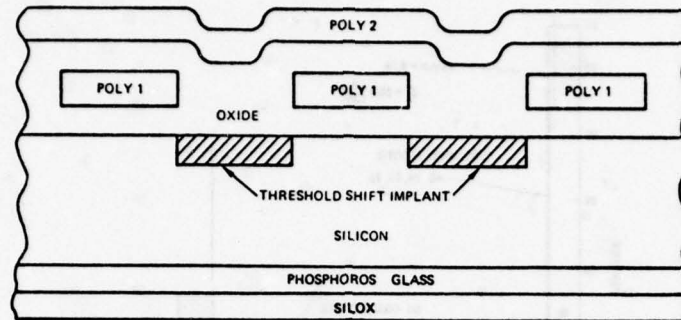
Figure 1. Cross-section of CCD After Phosphorus Gettering
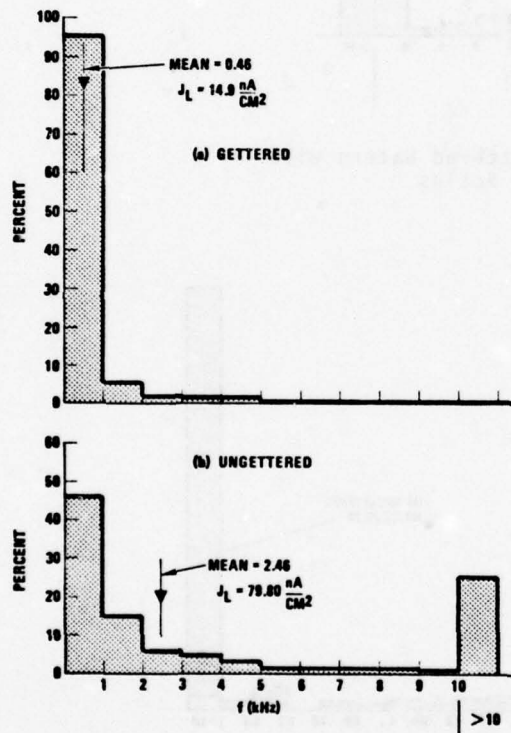
Figure 2. Histograms of Gettered and Ungettered Wafers
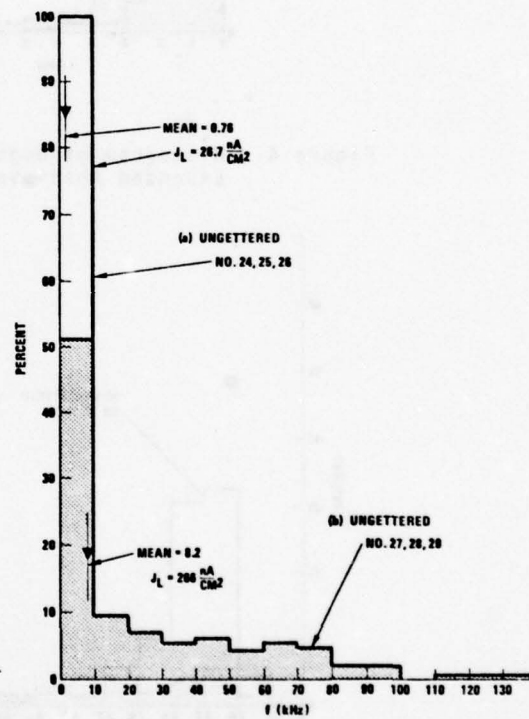
Figure 3. Histogram of Ungettered Wafers
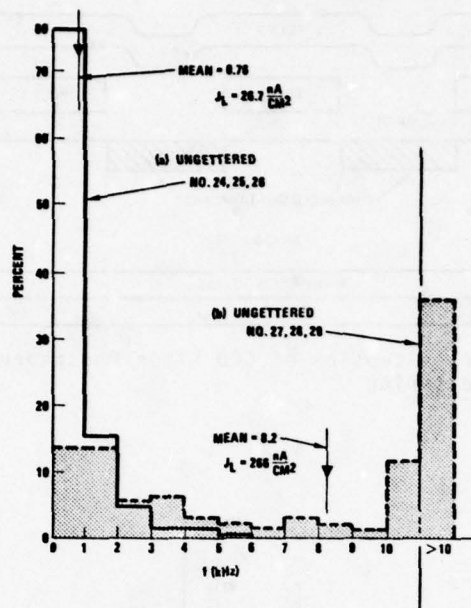
Figure 4.   Histogram of Ungettered Wafers with
Expanded Abscissa Scales
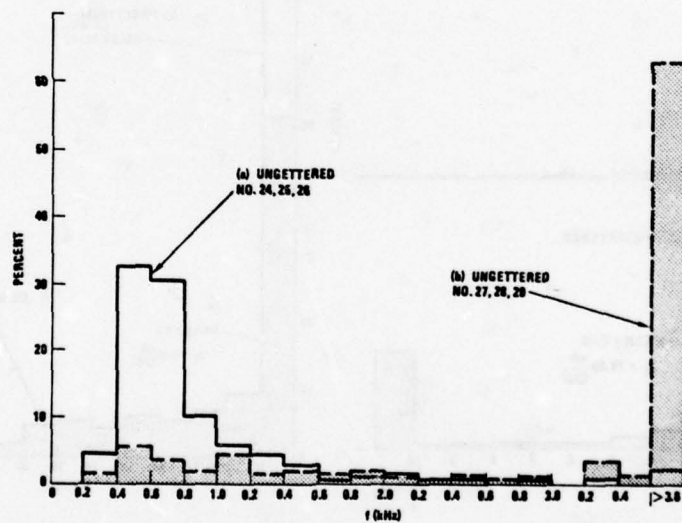
Figure 5.   Histogram of Ungettered Wafers Depicting
Bimodal Quality

4-36
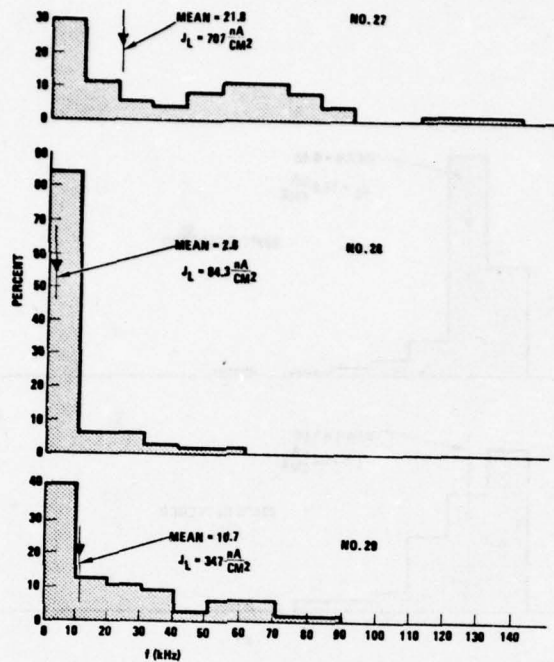
Figure 6. Histogram of "Bad" Ungettered
Wafers

TABLE 1.   WAFER AND OVERALL LEAKAGE
CURRENT DENSITY MEANS

	NOT GETTERED	925°C	975°C	1025°C
WAFER MEANS (KHz)	.72	.33	.36	.25
	.75	.39	.36	.36
	.80	.52	.46	.39
	2.63	.52	.52	.44
	10.74	.52	.81	.50
	21.80	1.00	-	.51
OVERALL MEANS (KHz)	2.46	.48	.50	.38
J_L (nA/cm^2)	79.80	15.60	16.20	12.30
R	30.30	3.00	2.30	2.00

R is the ratio of the highest mean in a group
to the lowest mean.
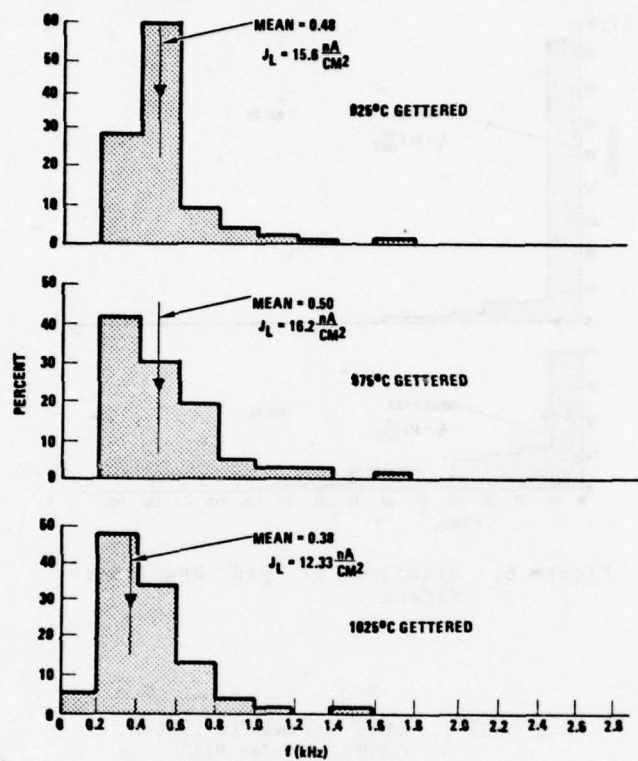
Figure 7. Histograms of Gettered Wafers at Various
           Temperatures
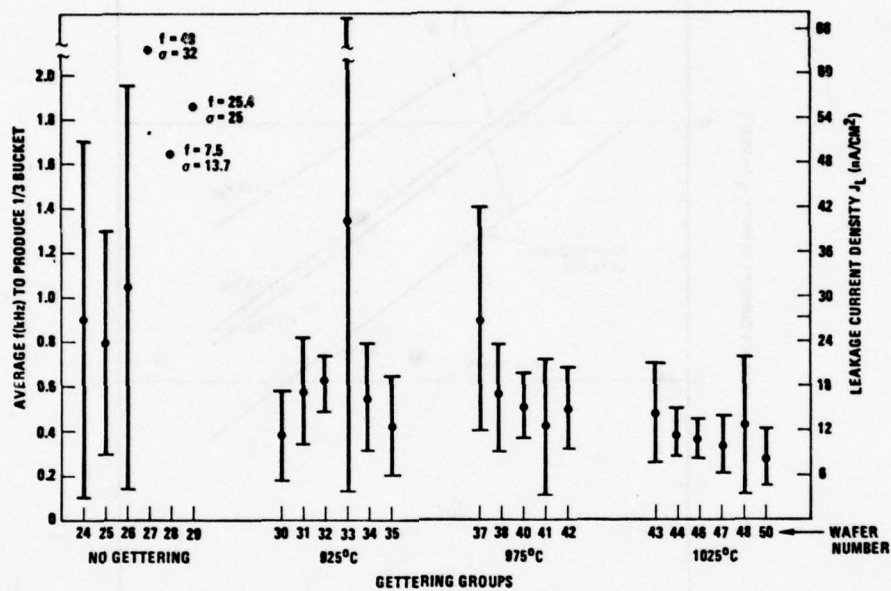
Figure 8. Leakage Current Density as a Function of Phosphorus Gettering Groups
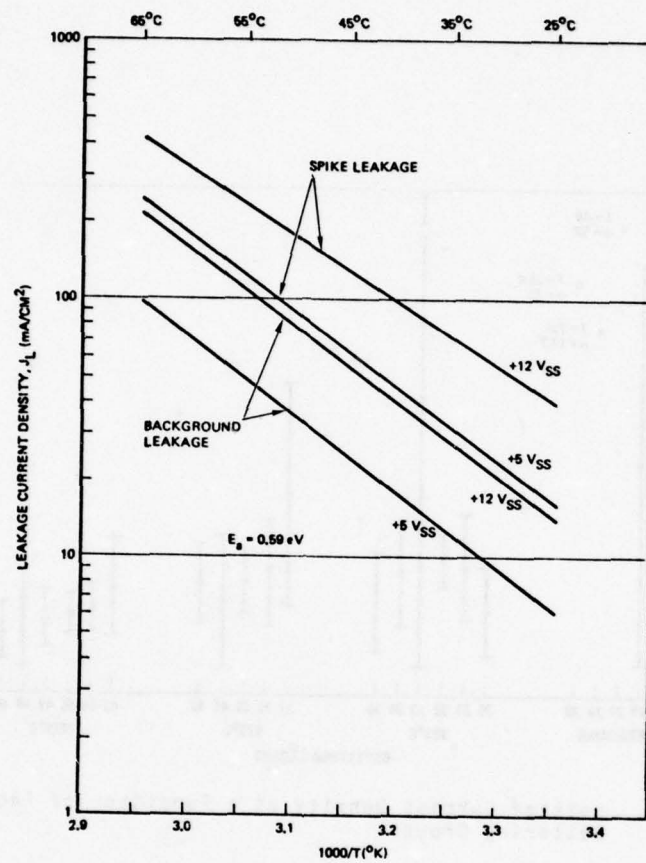
Figure 9. Leakage Current Density Versus Operating Temperature

ELECTRONIC PROCESSING OF INFRARED SCANNER SIGNALS USING CCD
MEMORY TECHNIQUES

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ABSTRACT

This paper describes the design of a video
quick look which electronically processes
signals of an infrared linescanner to a
moving-map presentation on TV display. The
image memory for display is composed of 16-
kbit dynamic Charged Coupled Devices (CCD).
These CCD memories are line addressable
which is attractive in the case of the line
scan orientation of sensing and display.

The paper gives a description of the video
quick look and outlines the design of the
CCD image memory. An application of the
video quick look is shown in the field of
thermal infrared remote sensing.

Keywords: Charge Coupled Device, Quick
Look, Infra Red Scanners, Data Acquisition.

1. INTRODUCTION

A video quick look system has been built
which functions as an element in the pro-
cessing of airborne-recorded infrared (IR)
data. The use of the quick look
presentation of the infrared data is two-
fold:
(i) Control of the quality of the signals
    from sensing equipment (Reconofax IR

line scanner) and the airborne recording
(ii) Selection of significant images out of
     the large amount of imagery recorded
     during flight. The procedure of
     selecting the IR images directly from
     the flight tape prior to image pro-
     cessing reduces computer time (figure
     1).
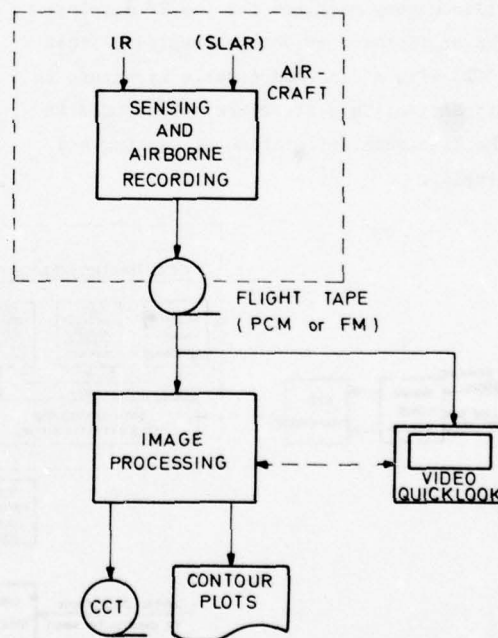
Figure 1. Recording and processing of infra-
red image data

The video quick look system accepts both FM analog and PCM high-density signal recordings. The system electronically processes the IR scanner signals to a moving-map presentation on TV display. At present the spatial resolution is determined by the 128*128-pixel presentation on the display. Expansion till a 512*512-pixel format is planned. The dynamic range corresponds to an 8-bit dataword per pixel. A flexible pseudo-color coding of the pixel values has been used to maintain the required dynamic range on the display.

A central part in the electronic processing of the IR line scanner data is the CCD image memory. This memory stores the incoming IR data with a linescan frequency of 380 Hz and functions as a high-speed video memory required for the TV display. The application of Charge Coupled Devices (CCD) with a line-addressable structure is attractive. This structure corresponds to the line-scan orientation of sensing and display.

For the video quick look system a 128-kbit image memory has been composed from 16-kbit dynamic CCD's.

The color coding circuitry has been developed in co-operation with the Technological University of Twente.

2. SYSTEM DESCRIPTION

The functional blockdiagram of the video quick look system is shown in figure 2. The modules of the system are: (i) the input handling, (ii) the CCD image memory, (iii) the color coding, and (iv) the presentation on color TV display.

(i) Input handling

The input section performs the signal conditioning and the analog-to-digital conversion of the analog recorded IR signals. This section also has an electronic zoom facility which determines the interval of sampling and the sampling frequency.
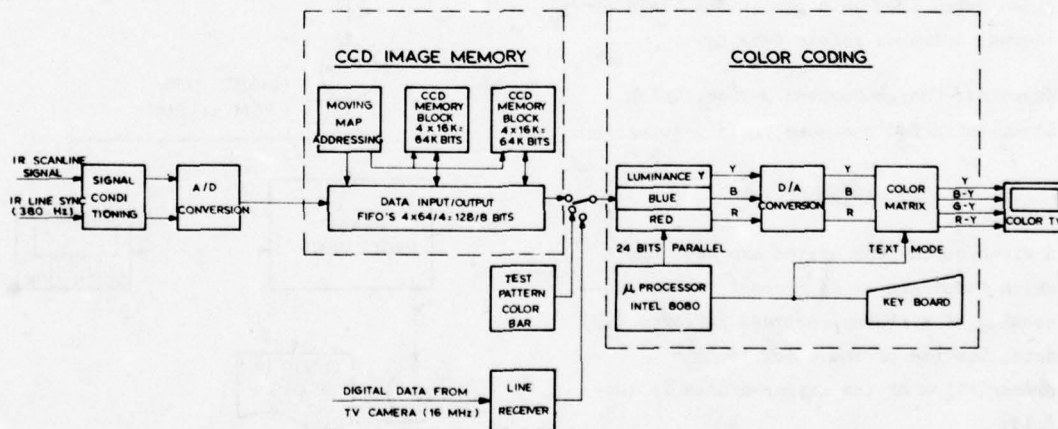
Figure 2. System blockdiagram of the video quick look

The resulting change in the spatial resolution in cross-track direction requires an equivalent change in the number of IR lines on display. This is to balance the resolution in cross-track and flight direction.

(ii) CCD image memory

The CCD image memory accepts digitized IR lines with a line frequency of 380 Hz. A selected IR image consisting of a sequence of 128 scanlines can be stored in the memory and is available for display without time limit. A real-time playback of the flight with the IR scanner is possible using the moving-map addressing of the CCD memory. The CCD image memory will be described in Section 3 in more detail.

(iii) Color coding

The color coding of pixel points is performed by means of look-up tables. The look-up tables are stored in fast random-access memories under control of the microprocessor. In this way the gray value of a pixel is translated into three separated values: luminance Y, blue B and red R. These digital values are converted into analog signals. The color matrix takes care of the transformation into luminance and color difference signals acceptable for the TV display.

Using the "text mode", three color tables can be stored, each color table containing 17 decimal values. The color-coding circuitry performs a linear interpolation between the selected color values. The decimal values of the color coding are shown on the TV display. The resulting color codes for each of the possible pixel values are made visible by means of a test pattern which generates a color bar on the display.

(iv) Presentation on color TV display

The resolution on display is determined by the 128x128 pixel presentation. It is realized by 128 pixels per TV line and 2 TV lines per IR scanline for one TV raster of 312.5 or 312 TV lines. This technique is compatible with the standard TV signal in 625 line format or in a special 624 line format. The IR images are displayed from TV line 1 to 512 included the interleaving. The color bar, generated by a testpattern, is displayed from TV line 512, thus at the foot of the picture. This color bar is available together with the IR image and can be used for calibration purposes.

3. THE CCD IMAGE MEMORY

The design of the CCD image memory is given in figure 3. The CCD image memory consists of three segments: (i) the CCD memory structure, (ii) the moving-map address circuitry, and (iii) the data input/output control.

(i) CCD memory structure

The 128-kbit memory consists of 8 Charged Coupled Devices (CCD), type Fairchild CCD461. These CCD's are dynamic line addressable RAM (LARAM) memories, each with 16-kbit memory. The CCD 461 has a 10 msec refresh period at an ambient temperature of $+ 55 \, ^\circ$C. The operating frequency is 2.5 MHz and the power demand is less than 200 mW. The CCD contains four sections of 32 lines and each line has a length of 128 bits. The sections have a separate 1-of-32 decoding matrix, recirculating loop and data input/output circuits.

MOVING-MAP ADDRESSING   CHIP SELECT 1-OF-8   CCD MEMORY 128 K BITS

3 BITS

TV LINE/FRAME BLANK → TV LINE ADDRESS COUNTER (8 BIT)

FRAME RESET   COMPARATOR 8 BIT

IR SCANLINE SYNC = $\frac{380}{n}$ Hz → IR LINE ADDRESS COUNTER (8 BIT)

5 BITS   1 2   8

READ/WRITE ENABLE

A_0-A_4 LINE ADDRESS   RE   WE
NR1 CCD 461 LINE MEMORY 32×128×4 BITS   DI-4 BITS

A_0-A_4 LINE ADDRESS   RE   WE
NR2 CCD 461 LINE MEMORY   DI-4 BITS

DATA INPUT/OUTPUT CONTROL

IR DATA → FIFO'S 4×64/4 = 128/8

IR SCANLINE SYNC   SHIFT IN   SHIFT OUT
IR DATA CLOCK ~ 75 kHz   WRITE CONTROL ÷ 128

TV LINE BLANK → TV LINE START DETECTION → START → READ CONTROL ÷ 128 → 2.5 MHz → TWO PHASE CLOCK DRIVER
CLOCK 10 MHz → 10 MHz

P ⎱ EXTERNAL
DT ⎰ CLOCKS
AE

P
DT
AE

DO-4 BITS

OUTPUT 8 BITS PARALLEL DATA
TO COLOR CODING AND TV DISPLAY

DO-4 BITS

Figure 3. Design of the CCD image memory

This means that the CCD is organized as 32 serial shift registers with 4-bit data in/out and a length of 128 data points. Common to all sections are the external clocks, the control signals and the addresses (A0-A4). The external clocks are Precharge (P) and Data Transfer (DT); the control signals are Address Enable (AE), Read Enable ($\overline{RE}$), and Write Enable ($\overline{WE}$).

The required 128*128-pixel format on display permits a straightforward use of the CCD line structure. The 128 lines on display are composed of 4 CCD's activated by the "chip select" decoder. The pixel value of 8 bits is attained by the parallel operation of 2 blocks of 4 CCD's.

A two-phase clock driver has been developed for the required external clocks (Precharge and Data Transfer) and the Address Enable. The total capacitive loading on the 0 V-12 V drive inputs is about 1000 pF.

The CCD line addressing operates on the TV line frequency of 15.625 kHz. Most of the time the data in the addressed lines are recirculated and refreshed.

In the Read mode, the data of the addressed line appears at the output with a data rate of 2.5 MHz. In the Write mode, the new 128 datawords are stored in the addressed line.

(ii) Moving-map address circuitry

The contents of the TV line address counter is updated at the TV line rate of 15.625 kHz. The contents determines the Read mode for the addressed CCD register. The roll-stabilized synchronization signal of the IR scanline continuously updates the contents of the IR line address counter. The IR line sync has a low frequency of $380/n$ Hz, where n is the line reduction factor.

The Write mode is activated when the addressed CCD register corresponds to the contents of the IR line address counter.

The moving-map addressing is present when the contents of the TV line address counter at the start of a new TV frame is given by the current value of the IR line address counter. This mechanism is outlined in figure 4. A "picture freeze" is simply realized by disconnecting the IR sync signal.
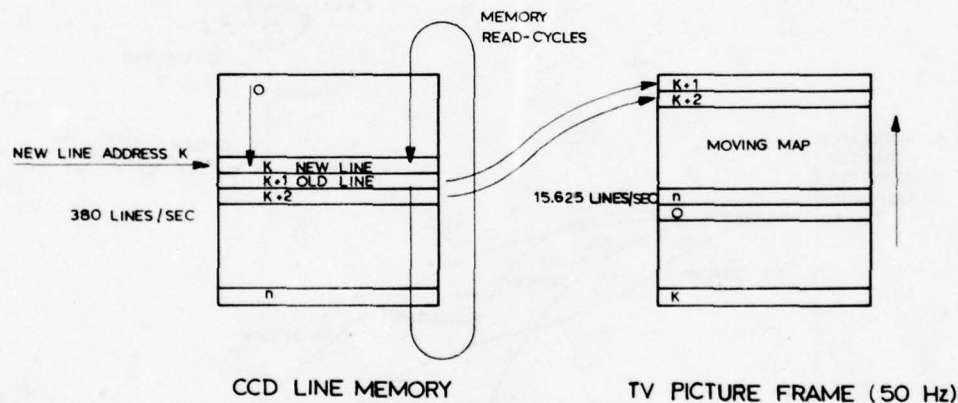
Figure 4. Moving-map display

(iii) Data input/output control

The CCD memory continuously operates at the standard TV line frequency with a pixel rate of 2.5 MHz. The conversion of the IR scan-lines with a relatively low frequency to the TV line frequency requires a line buffer memory accepting a wide range of input/output data rates. FIFO line buffers with a

register of 64×4 bits and maximum operating speed of 10 MHz have been selected. Shift-out of the IR line data of 128 pixels is activated by the address circuitry. Transfer of these data to the addressed line of the CCD memory occurs at the 2.5 MHz data rate.

The advantage of this design of the CCD image memory is that the support circuitry can be kept limited. Only three printed circuit boards (Euroformat: size 10*16 cm^2) have been required: one print each for the two-phase clock driver, the address circuitry and the data input/output control. The present 128*128-pixel memory is constructed on two printed circuit boards. The design is made in a modular way, e.g. extension to a 256*256-pixel format on display will be possible.

4. SYSTEM RESOLUTION

The design of an electrooptical imaging system requires a careful analysis of the spatial resolution of the system (Ref. 2). The use of Charged Coupled Devices introduces a two-dimensional sampling process, which in the flight direction is performed by the line-scan mechanism and in the cross-track by means of digitizing into picture elements. The system resolution can be analyzed using the Modulation Transfer Function Technique.
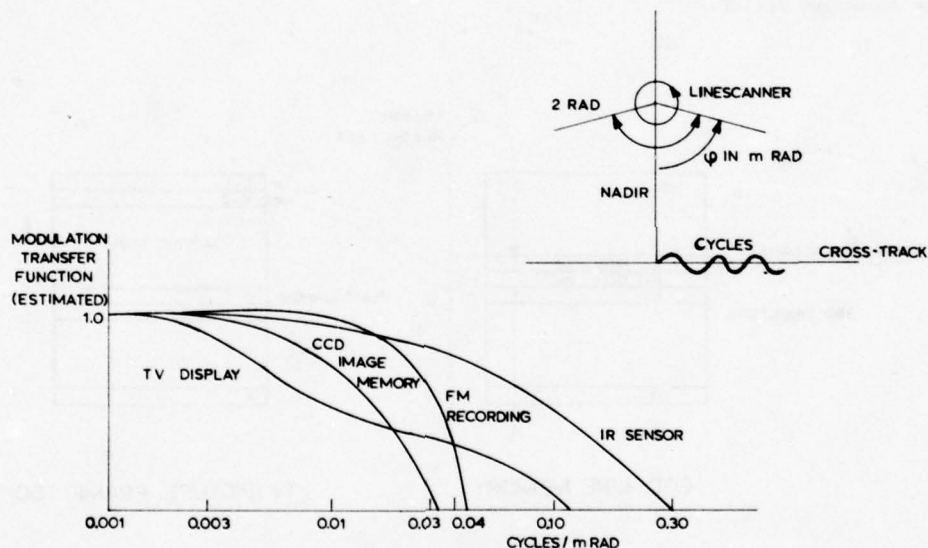
System Component	Characteristic	Estimated Resolution $\left(\frac{cycles}{mrad}\right)$
Sensor	Instantaneous Field of View(IFOV)	0.3
Magnetic Recording	FM:Bandwidth DC to 40 kHz	0.04
CCD Image Memory	Pixels per addressed line: 128	0.03
TV Display	Horizontal line response	~0.15

Figure 5. Estimated resolution in cross-track of system components

The MTF describes the sine wave response of the system components or the overall system. Figure 5 gives a survey of the estimated resolution in cross-track of the system components. In this case the system components are the (i) Reconofax IR line scanner with a scanfrequency of 380 Hz and an IFOV of 3 mrad, (ii) FM analog recording, (iii) CCD image memory determining the pixel format on display, (iv) spatial frequency response on the TV display. The survey of figure 5 shows that the recording and the memory format are the limiting factor in the system. It can be shown that this is also the case in the resolution in the flight direction. Therefore, the aim of further investigations will be improving the recording method (PCM high-density recording) and expanding the CCD image memory.

5. RESULTS

Flight 1191 has been carried out to investigate the cooling-water discharge near a power station in the North Sea coastal area. For this flight the NLR laboratory aircraft has been equipped with the Reconofax infrared scanner. Figure 6 shows the flight tracks over the North Sea area near the power station (Maasvlakte).
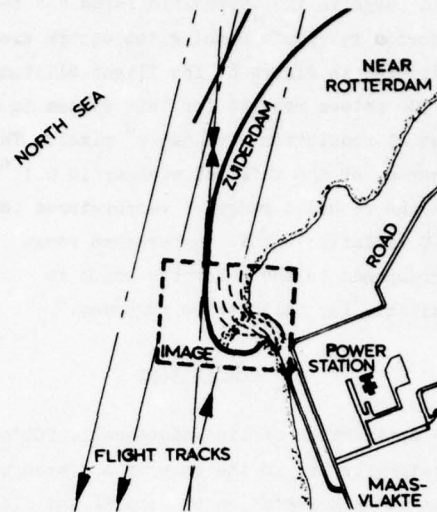
Figure 6. Flight tracks over the North Sea area near the power station – Maasvlakte. Flight 1191 – Project Rijkswaterstaat.

Figure 7 gives an example of the color-coded image on TV display.

Unfortunately, time did not permit the inclusion of color.

Figure 7. Color-coded image on TV display of the thermal infrared radiation pattern.

This image in the thermal infrared has been recorded by remote sensing the square area indicated in figure 6. The flight altitude of 300 meters results for this system in a spatial resolution with 5×5 m^2 pixels. The accuracy of the infrared scanner is 0.1 $^{\circ}$C and the recorded range of temperatures is 8 $^{\circ}$C (relative). This temperature range corresponds to the color bar which is available for calibration purposes.

6. CONCLUSIONS

The application of line-addressable CCD's is straightforward in the case of a system with a linescan orientation of sensing and display. The CCD's are organized as serial shift registers operating at video rates. This organization involves a minimum of support circuitry required to operate the CCD image memory.

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DEVELOPMENT AND DESIGN OF A NOVEL TWO LEVEL 64k-BYTE CHARGE-COUPLED MEMORY SYSTEM FOR MICROCOMPUTER APPLICATIONS.

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ABSTRACT: Charge-Coupled Device memory technology offers potential economic advantages over semiconductor random-access memory technologies. However, the limitations incurred by the serial nature of the Charge-Coupled Device (CCD) have restricted most efforts to apply CCD memory technology to large memory systems. This paper demonstrates the feasibility of a CCD memory technology for moderate size memory systems.

A 64k-byte memory system using commercially available Charge-Coupled Devices has been developed for microcomputer applications. Design objectives included low-cost, adequate performance, reliable operation, small size and low power consumption as well as simple interfacing to standard microprocessors. The design of the developed memory system features a two-level organization which includes a RAM to buffer the Charge-Coupled Device serial memory; this improves the average access time and simplifies interfacing with standard microcomputers.

By taking advantage of the track-sector organization of the Intel 2416 CCD memory device, a relatively simple hardware implementation of the memory system was realized; this eliminated the need for the software implemented operating system which characterizes many other bulk storage memory systems.

The developed memory system fills a gap between high performance semiconductor random-access memory and the slower serial magnetic memory technologies. Design details of the memory system and experimental results obtained with a 16k-byte prototype will be presented in this paper. Testing of the memory system prototype with a KIM-1 microcomputer system demonstrated that the technical objectives have been successfully realized. It is anticipated that the memory system can be easily modified to use the new Intel 2464 which is 64k word X 1 bit CCD memory device.

I. INTRODUCTION

Charge-Coupled Device (CCD) memories offer significant economic advantages for bulk storage of digital data [1] relative to MOSFET and bipolar RAMs. However, the serial organization of data in CCD memories has the disadvantage that the random access of data is slow due to the serial latency time. Typical values for commercially available designs are 100 μs average [2] and 0.8 ms maximum [3]. Thus CCDs cannot directly compete with semiconductor RAMs where the high speed random access of data is important. However it is anticipated that CCDs may find usage in microcomputer systems where a CCD memory buffered by a random access memory offers a logical solution to the problem of economic bulk memory.

The intention of our paper is to demonstrate

the feasibility of this concept. Features of our developed 64k-byte two-level memory system include simple interfacing with standard microprocessors, parity checking, low power consumption and small size.

II. CONSIDERATIONS FOR A TWO-LEVEL CCD MEMORY SYSTEM

The cache memory concept makes use of the fact that data in a memory system is seldom accessed from memory locations at random [4]. Consequently selected blocks of data from a large and slow primary memory (M_p) can be stored in a small fast cache memory (M_c) where they may be rapidly accessed by the Microprocessor Unit (MPU). Requests for other data in the memory system necessitate the comparitively slow transfer of the requested data from M_p,

either directly or via M_c with some consequent reduction in the average memory system speed.

The simplified direct address buffer organization defined in Figure 1, is the simplest possible cache memory organization. It involves the division of the 2^n word primary memory (M_p) into pages of 2^m words in length. The (n-m) highest order address bits of a word determine the page that it is located in (the page address), while the remaining m lowest order address bits define the location of the word within the page. The cache memory (M_c) provides random access storage of a single page of data. The MPU can directly address a word of data within this page by using the m lowest order address bits.

Page oriented cache organizations such as the direct address buffer organization are well suited for applications with CCD primary memories. Pages of data may be stored in a CCD shift register memory on consecutive sectors (shift register data locations) in one or more tracks (shift registers). After the latency time required to reach (search for) the first bit in the page, data may be transferred at a rate equal to the product of the data shift rate and the number of tracks accessed on each data shift. Consequently one search operation (for the first bit of the page) is sufficient for the transfer of the entire page.

The average time to transfer a page of data will then be:

$$t_{pt} = t_\ell + \frac{p}{d_{max}} \text{ where } t_\ell = \text{latency time,}$$

p = page size.

d_{max} = CCD average data rate for uninterrupted data transfer from consecutive sectors.

Accordingly the average data rate (d) during the page transfer will be:

$$d = \frac{p}{t_{pt}} = \frac{d_{max}}{1 + \frac{t_\ell \; d_{max}}{p}}$$

Normally $t_\ell \gg \frac{1}{d_{max}}$, so the average data rate is substantially increased for page sizes much larger than 1 word.

The serial nature of the CCD memory becomes a useful property for data transfer between M_c and M_p since a single data bus is sufficient. With appropriate three-state logic techniques, the same data bus may be used to interface M_c to the processor. Another useful design economy may be realized by using the CCD memory sector address counter to generate the address for M_c during data transfers between M_c and M_p.

These factors all favour a hardware rather than a software implementation of a two-level memory system. A hardware implementation offers useful performance advantages since normally a limited set of logical operations will be performed for each memory access; these can be realized with specialized logic modules of sufficiently high performance that system speed is not adversely affected. A hardware implementation may be designed to be almost completely transparent; i.e., the memory system is functionally identical to a conventional memory system based on random access memory technology except for the necessity of requiring the processor to enter a wait state during internal data transfers between M_c and M_p resulting from data requests for new pages.

A most fundamental design problem is to determine the optimum sizes of M_c and M_p. Clearly M_p should be much larger than M_c, otherwise a single-level memory system would be both simpler and more economical. On the other hand, M_c should be large enough that the ratio of the number of times that requested data is in M_c to the total number of data requests (the h or "hit" ratio) should be high; otherwise the memory performance will be poor.

Parity checking may be performed either on the M_c I/O buffer or on the M_p I/O. The former has the advantage that parity checking is effective on M_p as well as M_c while the latter requires fewer components since M_c need not store parity bits.

III. MEMORY SYSTEM DESIGN AND IMPLEMENTATION

Basically our memory system consists of the four components blocks illustrated in Figure 2; the Primary Memory M_p realized with commercially available 16k-bit CCD memories for economic bulk data storage, the Cache Memory M_c for random access storage of data pages fetched from M_p, and the I/O

Buffer to interface M_c to the external data bus, and the Control Unit which generates the control signals for both M_p and M_c.

A design capacity of 64k words x 9-bits (including parity bits) for M_p was selected as a suitable value for potential microcomputer requirements. This also provides some hardware compatibility with the new 64k-bit CCD memories. Due to the modular design philosophy employed, word length expansion can be directly achieved by the parallel operation of additional M_p and M_c units from a common control unit.

To realize a 64k word x 9-bit memory capacity for M_p, the Intel 2416 16k x 1-bit CCD memory devices are conventionally organized as a 4 x 9 matrix (Fig. 3). The 2416 memory device is internally organized as a linear array of 64 recirculating shift registers which are each 256-bits in length. As a consequence of the serial nature of the CCD memory, the memory system uses two modes of addressing to access data in the 2416 memory devices:

(i) Track addressing: Each 2416 track (representing a 256 bit recirculating shift register) has a single I/O port which may be used to access a bit of data stored in a sector (representing a shift register storage cell). The decoded 6-bit CCD track address ($A_0 - A_5$) selects 1 of 64 tracks for data I/O operations. Between shift operations performed by the 4ϕ CCD clocks, it is permissible to sequentially access different tracks for I/O operations by utilizing this track addressing feature. In this respect, the 2416 memory I/O design resembles that of a 64-bit dynamic RAM, the major difference is that only 1 of 256 sectors in each track is addressable by the track address at any given time, whereas every data location in a RAM is addressable.

A 1 x 9 device organization in each row of Figure 3 corresponds to a 16k word x 9-bit data organization when both sector and track addressing modes are used. Memory Bit/Word expansion is most directly accomplished by affecting a track expansion; additional rows of 2416s are operated in parallel with data selected from the appropriate device in each column. This is demonstrated in Figure 3 where the two additional address bits, CA_{14} and CA_{15}, are decoded to select 1 of 4 rows via the 2416 Chip Select (CS) inputs. In each column the 2416 data inputs and outputs are connected in parallel and WIRED-OR con-

figurations respectively. The unselected devices continue to recirculate their data, but their inputs and outputs are disabled. The four devices in each column are thus functionally equivalent to an array of 256 tracks of which 1 is selected for data I/O by an eight-bit track address for a total data capacity of 64k x 1 with both track and sector addressing.

The organization of the track address bits in the memory system is closely related to the memory data page organization. The 64k word x 9-bit capacity of the CCD memory (M_p) is divided into 256-byte pages for data transfer operations to the cache memory (M_c). Each page of data in M_p corresponds to 16 consecutive sectors x 16 tracks in each column of Figure 3. On page transfer operations, the CCD $A_0 - A_3$ track address bits are stepped from 0 through 15 on each data shift by the $CA_0 - CA_3$ address generated by a 4-bit binary counter C_1 in the Control Unit. These address bits partially define data locations within a page. The $CA_{12} - CA_{15}$ address bits select blocks of 16 tracks from which data is accessed by the $CA_0 - CA_3$ address bits on each data shift during page transfers, therefore pratically defining the page address.

(ii) Sector Addressing: The basic CCD data storage element is the shift register. Each of the shift registers in the 2416 memory device is composed of paired 128-bit shift registers multiplexed to function as a 256-bit recirculating shift register. A data or sector location in each shift register will physically change with each data shift; returning to the same location after 256 data shifts. To access a particular sector, it is necessary to perform a data search operation by waiting for the desired sector to be shifted to the track I/O port by the CCD 4ϕ clocks. As each sector is cyclically shifted through 256 shift register cells, and the relative locations of the sectors are fixed, the relative location of the sector at the shift register I/O port is defined as a sector address which can be specified by the output of an 8-bit binary counter clocked at the data shift rate.

In the memory system Control Unit (Figure 4), and 8-bit counter, C_2, is clocked at the CCD data shift rate by the ϕ_B clock to generate the sector address bits $AC_4 - AC_{11}$ ($\triangleq CA_4 - CA_{11}$ during data transfers between M_c and M_p). Address bits $AC_8 - AC_{11}$ define blocks of 16 consecutive sectors on each track, thereby specifying a page address in combination with track address bits $CA_{12} - CA_{15}$. Page trans-

fers are permitted by the Control Unit when the page subaddress $AD_8 - AD_{11}$ in the M_c Page Register corresponding with the page to be transferred matches $AC_8 - AC_{11}$. Sector addressing thus consists of counting and comparison operations performed in the control unit; no explicit sector addresses appear in M_p.

A page address is completely specified by the $CA_8 - CA_{11}$ sector address bits and the $CA_{12} - CA_{15}$ track address bits while the word address within a page is defined by the $CA_0 - CA_3$ track address bits and the $CA_4 - CA_6$ sector address bits. Thus 16 address bits define a word location in the 64k word memory M_p.

During page transfers, $CA_8 - CA_{15}$ define the page address of the data being transferred while address $CA_0 - CA_8$ is incremented from 0 through 255 to effect the transfer of 16 consecutive sectors of data from 16 tracks for each bit/word. This is illustrated in Figure 5 for a conceptual page transfer involving Page 0 in M_p.

The design of the M_p memory is illustrated in Figure 6. The 2416 address lines $A_0 - A_5$, CE, CS and WE lines are driven by Intel 3245 quad TTL to MOS level translators. These devices have the advantage that they offer suitable output levels for the CCD memory devices without additional power supplies. The CCD 4ϕ clocks are driven by a 5224 quad clock driver for each 4 memory devices. The 5224 is specifically designed for the required output levels and transition times for the 2416 memory devices.

Page transfers between M_p and M_c involve the serial transmission of eight-bit parallel words. The ninth bit is used for single error detection on the M_p data lines. A 74LS280 parity generator/checker generates single parity bits for each word of input data to M_p; these parity bits are stored in M_p with the corresponding 8-bit data word. Another 74LS280 performs a parity check on the M_p output data. A JK flip-flop is used to monitor the parity check output for error indications during data transfers from M_p to M_c. A momentary contact switch permits the flip-flop to be manually reset.

The directly addressed cache memory of figure 7 has a capacity of 1 page (256 words x 8-bits). Static MOS/RAMs of the 2101A-2 type were employed because they offer adequate performance and their simple timing requirements facilitated interfacing M_c to both M_p and the MPU data bus. Intel 3212 latch/buffers with 3 state outputs are used to interface M_c to the bidirectional MPU data bus. The address organization of M_c

is equivalent to that used by M_p with the difference that the $CA_4 - CA_7$ address bits exist explicitly since M_c is a random access memory.

During memory system operation, the Control Unit executes the sequence of operations defined in Figure 8 in response to the MPU I/O signals. There are basically two modes of operation:

(i) I/O Mode: When the MPU requests data from a page stored in M_c, M_c is placed under the direct control of the MPU I/O signals via the I/O logic. M_c then looks like a conventional static RAM to the MPU which addresses it via the $SA_0 - SA_7$ address bits.

During the I/O mode, data is recirculated in M_p at the minimum shift rate (55 KHZ) to reduce AC clock power requirements. The M_p I/O is forced into an inactive state by keeping the CCD CE and WE signals low and disabling the outputs of the latch used to buffer the CCD data outputs.

(ii) Page Transfer Mode: When data from a new page is requested by the MPU, the Memory Management Logic implements the required data transfer operations between M_c and M_p to reach the conditions satisfying the I/O mode criteria. During the page transfer mode, the MPU is placed in a wait state via the Mready signal and the I/O Logic is disabled.

A major difference between the two modes of operation is that M_c is synchronized to the MPU clock in the I/O Mode, and to the CCD 4ϕ clocks in the Page Transfer Mode.

The essential purpose of the I/O Logic is to use the MPU I/O control signals to interface the MPU to M_c via the I/O Buffer and address latches A and B. The I/O Logic was designed after a study of the I/O signals from several standard MPUs. The major restriction is that the MPU can be placed in a wait state with a Wait or Ready signal after a valid address is available. This is to permit the Control Unit to place the MPU into a wait state during the Page Transfer Mode following a request for data in a new page by the MPU. Many MPUs such as the Intel 8085 and 8080, the Zilog Z-80 and with some restrictions, the MOSTEK 6502 can readily meet this requirement.

IV. EXPERIMENTAL RESULTS

A prototype of the CCD memory system was constructed with a reduced M_p capacity of 16k x 8, (Figure 9). A total of 53 integrated

circuits on two 9" x 4 1/2" circuit boards were required. The total number of integrated circuit package, and types required for both 16k word x 8 bit and 64k word x 9 bit memory systems is given in Table 1.

The memory system functioned as intended. Figures 10 and 11 illustrate the major control signal waveforms used in serial data transfers from M_p to M_c; the CCD ϕ_1, CCD CE, $\overline{RAM\ WE}$ and CCD $\overline{D_{out}}$ signals in Figure 10 and the CCD ϕ_1, CCD CE, $\overline{RAM\ WE}$ and CCD A_0 waveforms in Figure 11. The relative timing of the CCD CE and $\overline{RAM\ WE}$ signals is very important since the timing of the data output from M_p will be dependent on the CCD CE signal, and in turn the $\overline{RAM\ WE}$ signal must be set up to write the data from M_p into M_c. The data track and sector organization used in the memory system results in 16 data cycles on each shift, or 32 for each complete 4ϕ clock cycle; the relationship of the CA_0 address bit used for the A_0 track address bit on the CCD memory device to the CCD ϕ_1, CCD CE and CCD WE signals can be seen in Figure 11.

A MOS Technology K1M-1 microcomputer was successfully interfaced to the memory system with the aid of some additional support circuitry to:

1. Buffer the K1M 6502 I/O.
2. Synchronize the Mready signal to the MPU $\phi2$ clock.
3. Fully decode the MPU address lines.
4. Temporarily store the MPU data and address during write operations to new pages. This is necessary as the 6502 MPU will enter a wait state only during a read operation.

Tests conducted with the K1M microcomputer demonstrated that the major technical criteria for a memory system were fulfilled:

(i) Performance: Conservative timing margins were obtained in the I/O mode for the standard 1 MHz clock frequency of the K1M microcomputer. In the Page Transfer Mode, an average latency time of 128 μs and a page transfer time of 144 μs were achieved without difficulty. The average time to perform a data transfer between M_c and M_p is therefore 144 μs + 128 μs = 272 μs which corresponds to the average memory cycle time if data in M_c has not been modified. Otherwise two page transfers are required and yield an average memory cycle time of 544 μs.

(ii) Reliability: Reliability is a fundamental memory system consideration. It is essential that the memory system be free of pattern sensitivity problems which may manifest themselves as troublesome "soft" errors. It has been demonstrated that a few simple test patterns predicated on the CCD internal organization are sufficient for adequately testing a CCD memory.

Tests conducted with the recommended test [5] patterns revealed reliable memory operation was possible over a wide range of supply voltages.

(iii) Power Consumption: Three standard power supply voltages are required by the memory system: + 12 V, + 5 V, - 5 V. The measured current requirements for the 16K x 8 prototype are shown in Table 2.

The + 12 V current consumption may be extrapolated for the full 64k x 9 memory capacity to yield a total I/O Mode power consumption of only 13.8 μw per bit.

V. CONCLUSIONS

The use of two-level memory organizations featuring a CCD primary memory is both feasible and practical in microcomputer systems.

VI. REFERENCES

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VII. ACKNOWLEDGEMENTS

TABLE 1. MEMORY SYSTEM INTEGRATED CIRCUIT LIST

	Integrated Circuit Type	Quantities	
		16K word x 8-bit	64K word x 9-bit
2416	CCD Memory Device	8	36
5224	Quad CCD Clock Driver	2	9
3245	Quad TTL to MOS Buffer	2	3
2101A-2	256-Bit x 4 Memory	2	2
8212/74S412	Octal Latch/Buffer	6	6
74LS00	Quad 2-Input NAND Gate	1	1
74LS04	Hex Inverter	6	6
74LS08	Quad 2-Input AND Gate	1	1
74LS28	Quad 2-Input NOR Buffer	1	1
74LS37	Quad 2-Input NAND Buffer	3	3
74LS74	Dual D-type Flip-Flop	2	2
74LS76	Dual JK Flip-Flop	2	3
74LS85	4-Bit Comparator	3	3
74LS86	Quad 2-Input EXCLUSIVE-OR Gate	1	1
74123	Dual Monostable Multivibrator	4	4
74LS126	Quad 3-state Buffer	2	2
74LS132	Quad 2-Input NAND Schmitt Trigger	1	1
74LS138	3 to 8 Line Decoder	1	2
74LS161/	4-Bit Binary Counter	3	3
74LS163			
74LS164	8-Bit Shift Register	1	1
74LS221	Dual Monostable Multivibrator	1	1
74LS280	9-Bit Parity Checker/Generator	-	2

TABLE 2. MEMORY SYSTEM POWER CONSUMPTION*

		I_D	Power
+ 12.0 V	I/O MODE	49mA (220mA)	.59W (2.64W)
Page Transfer Mode	Data Search	170mA (765mA)	2.04W (9.18W)
	Data Transfer	105mA (472mA)	1.26W (5.66W)
+ 5.0 V		1.1A	5.5W
- 5.0 V		~ several µA	

* for 16k x 8 prototype memory system, values in parenthesis pertain to estimates for full 64k x 9 capacity.

Figure 1. Direct Address Memory Organization.

PAGE   Mp DATA
ADDRESS (2^n WORDS)

0

$2^m - 1$

0

$2^{n-m} - 1$

0

$2^m - 1$

Mc DATA
(2^m WORDS)

0

$2^m - 1$

$\Rightarrow$ MPU

$\left(\begin{array}{c}\text{MICROPROCESSOR}\\ \text{UNIT}\end{array}\right)$

WRITE
TAG BIT

Mc PAGE
REGISTER

2^m WORDS = 1 PAGE
2^n WORDS = 2^{n-m} PAGES
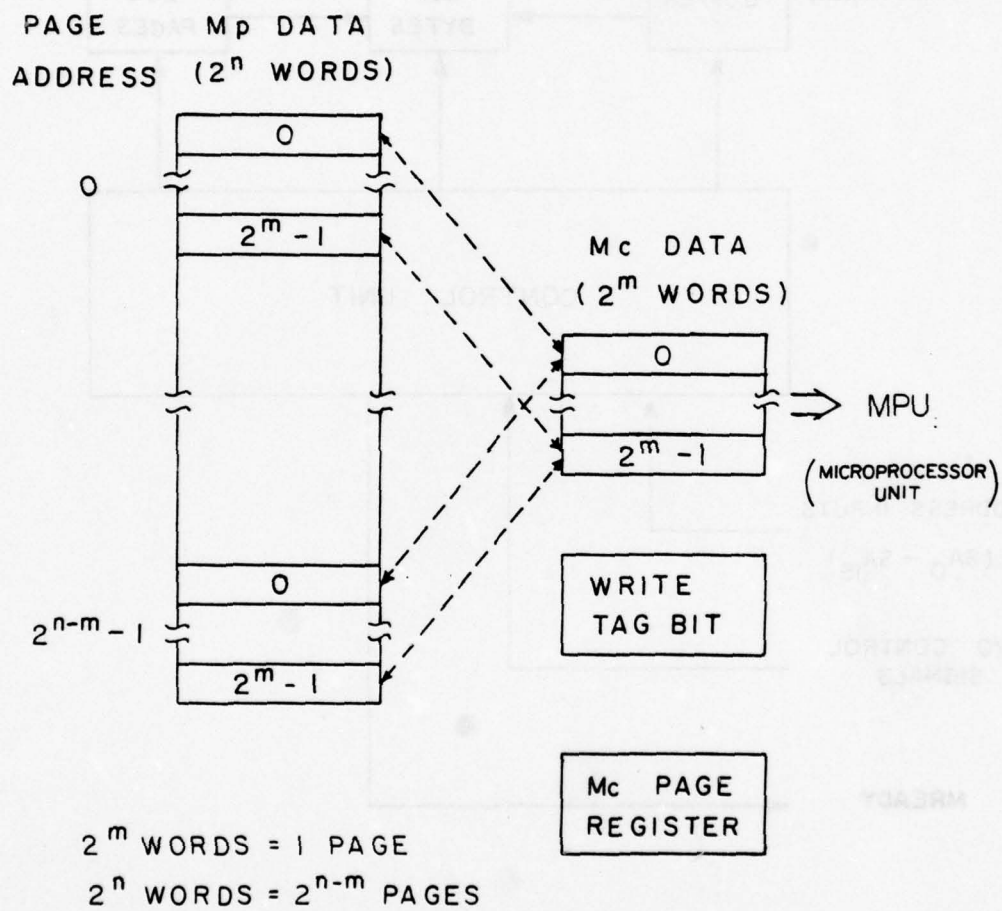
DIRECT   ADDRESS   ORGANIZATION
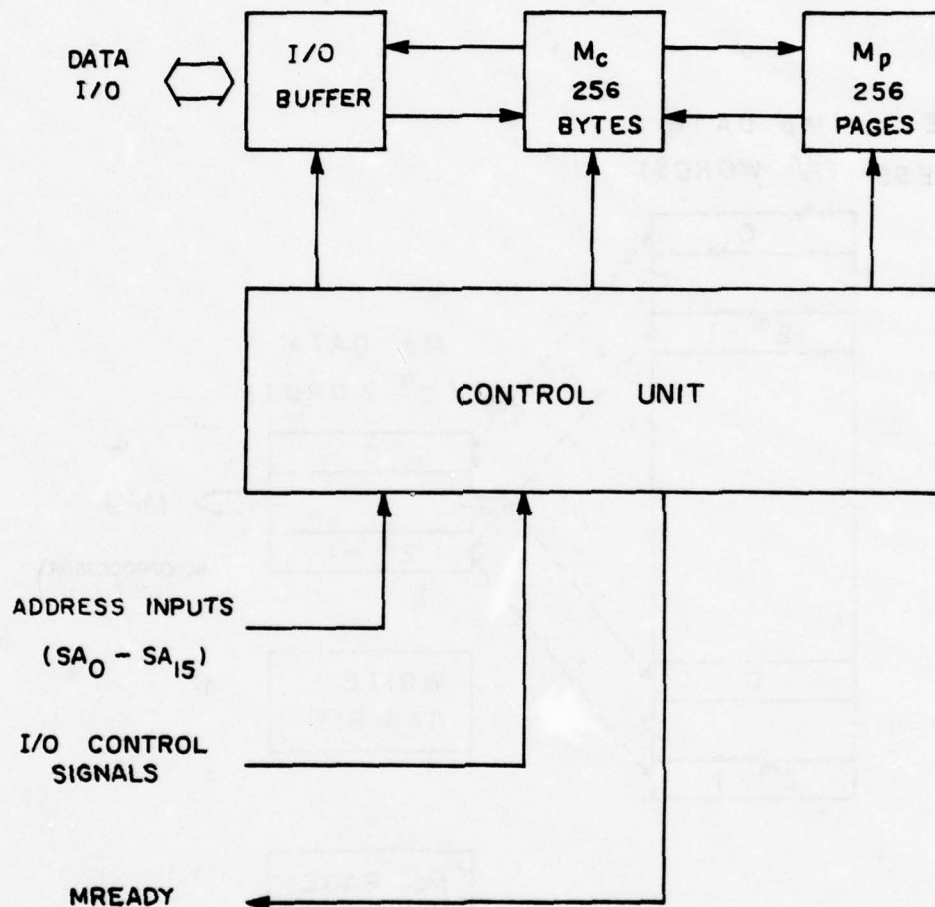
Figure 2.   Block Diagram of a Simplified
Two-Level Memory System Using A
CCD Primary Memory
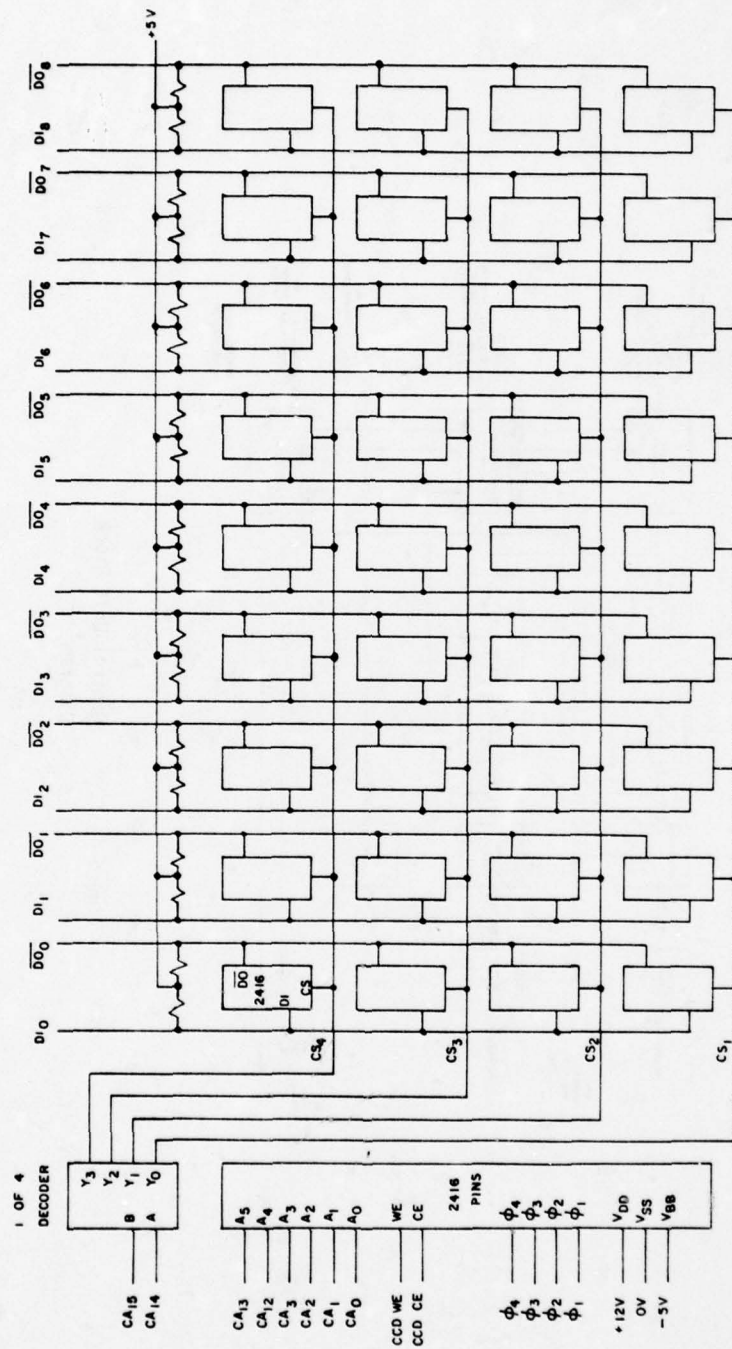
Figure 3. Organization of 16K word X 1 bit CCD Memory Devices for 64K word x 9 bit Memory Capacity

4-57
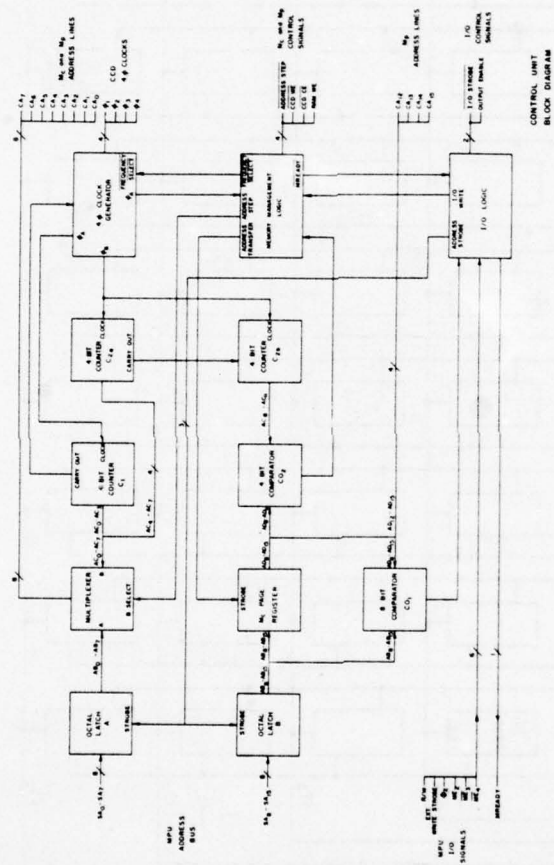
Figure 4. Control Unit Block Diagram

Figure 5.   Representation for the Addressing of Data in M_p During a Typical Page Transfer.
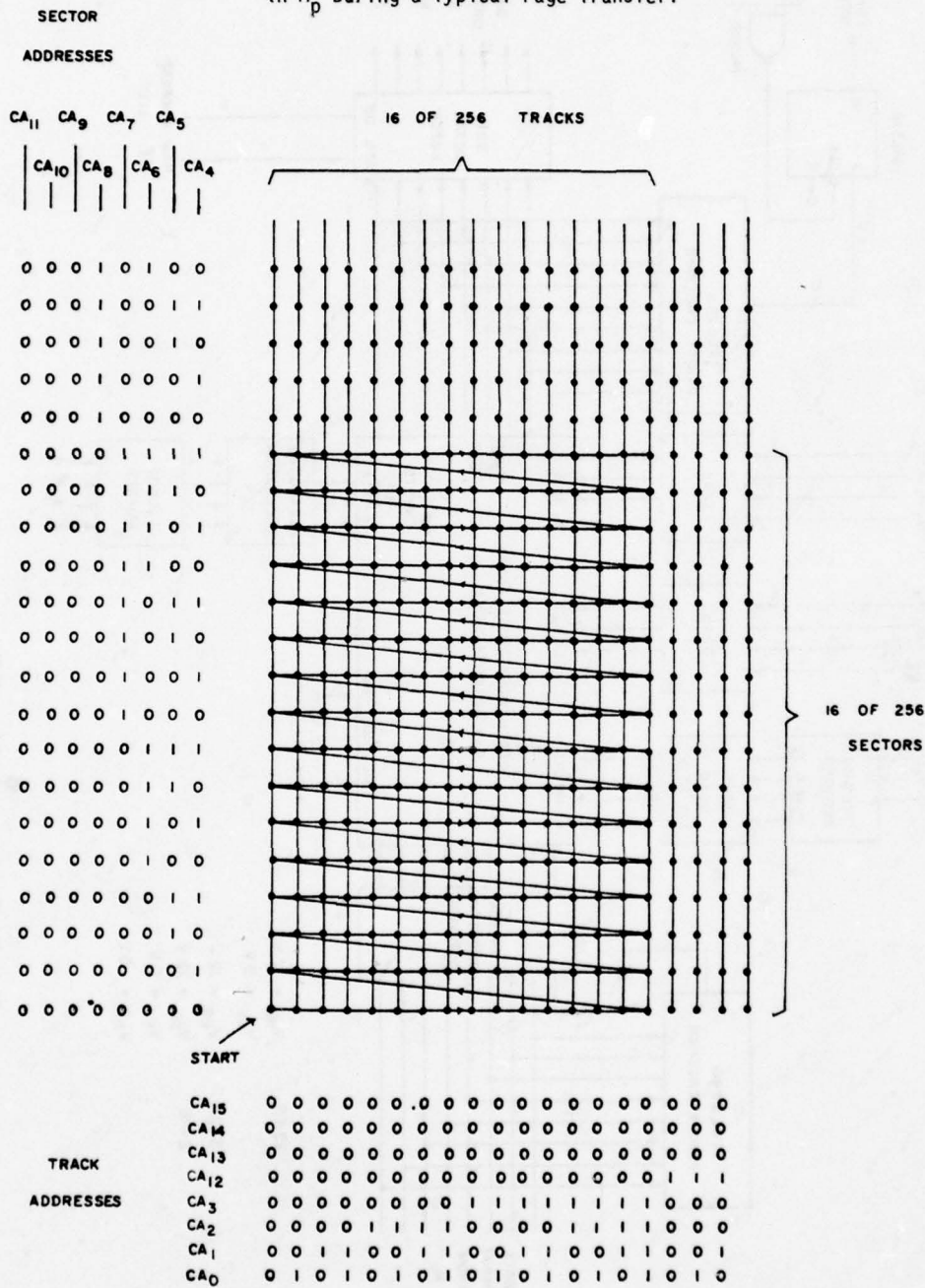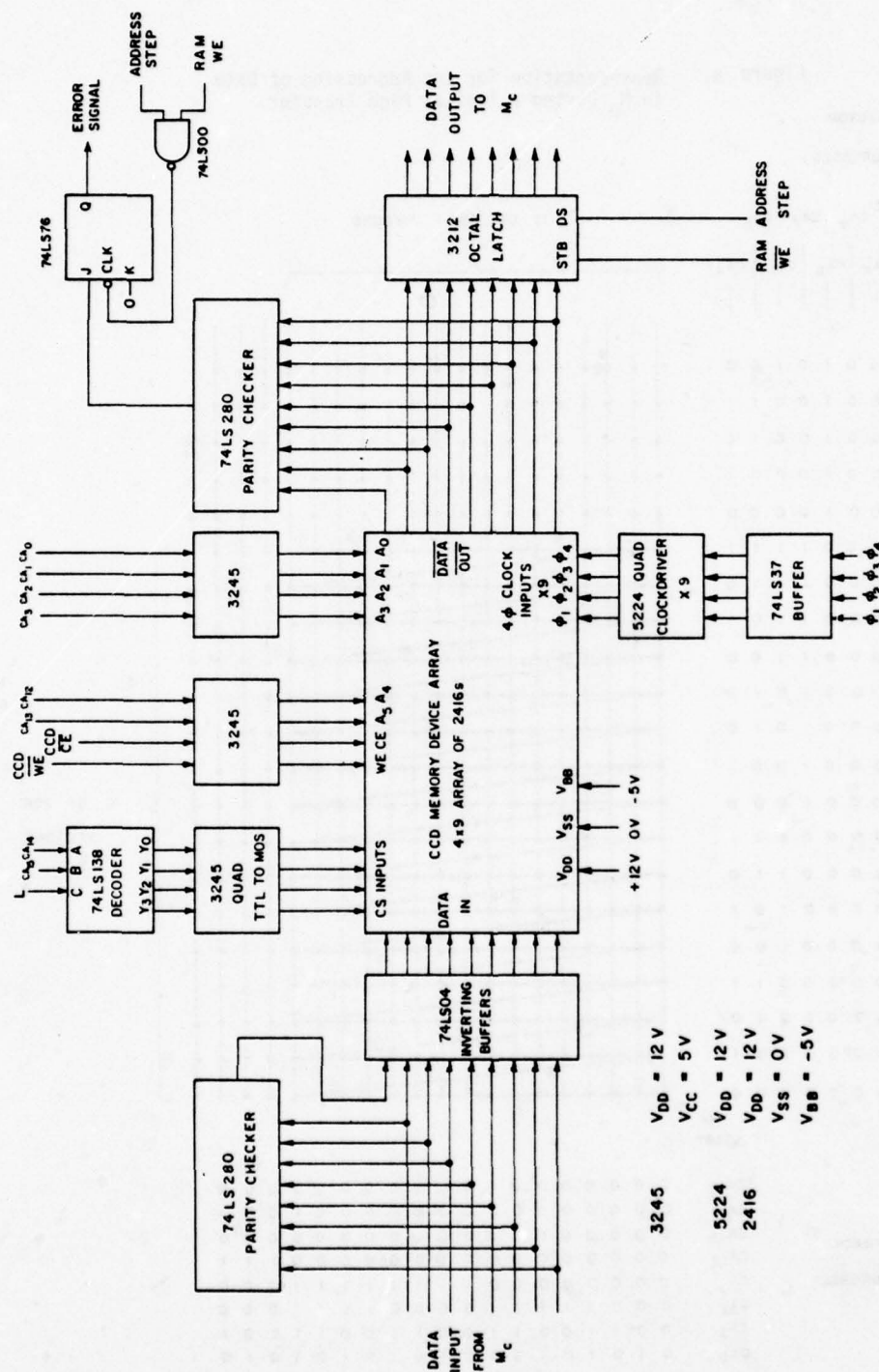
Figure 6. Organization of M_p with Support Circuitry
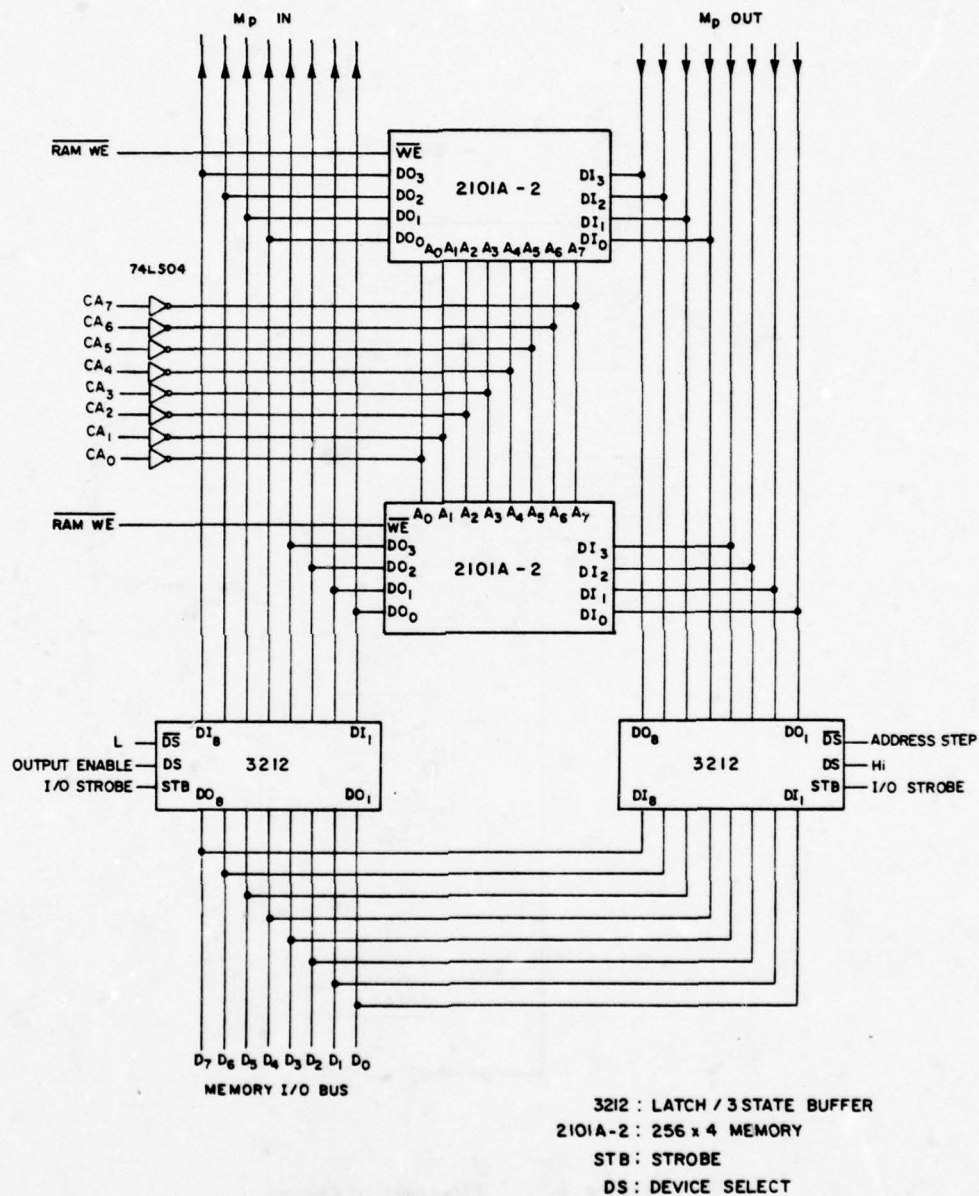
Figure 7. Organization of M_c and I/O Buffer

3212 : LATCH / 3 STATE BUFFER
2101A-2 : 256 x 4 MEMORY
STB : STROBE
DS : DEVICE SELECT
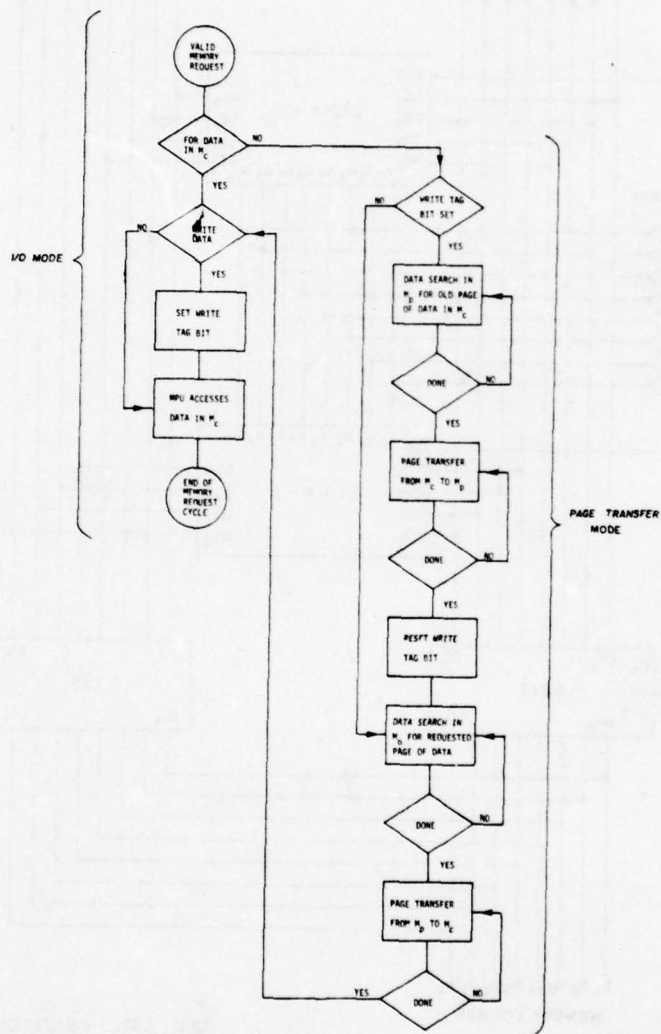
Figure 8.   Flowchart of Memory
System Operation

Top view of the Memory Board containing M_c, M_p, and the I/O Buffer.
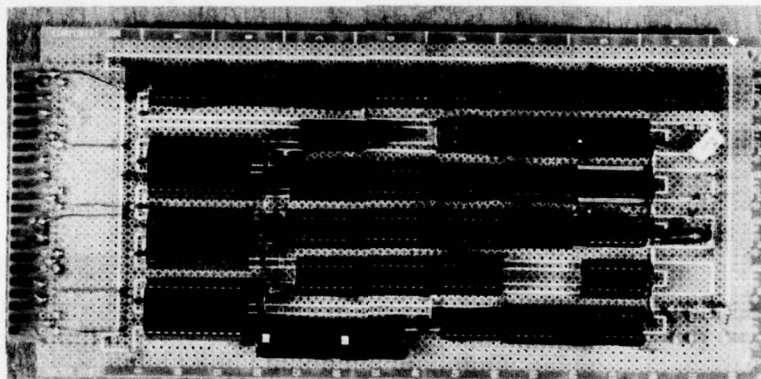
Top view of the Control Unit Board.
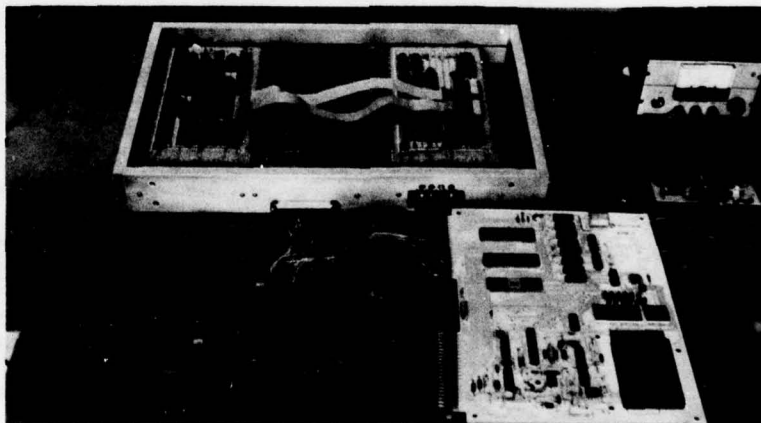
Figure 9. View of the 16k x 8 memory system prototype with 6502 Interface Adapter, KIM Buffer Unit, and the KIM-1 microcomputer.

Figure 10. Waveforms for data transfer from M_p to M_c.

Figure 11. Waveforms for data transfer from M_p to M_c.

SAW/CCD BUFFER MEMORY*

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ABSTRACT

A surface acoustic wave (SAW) piezoelectric delay line has been integrated with a silicon CCD shift register to produce a fast-in, slow-out buffer memory. A prototype device with an 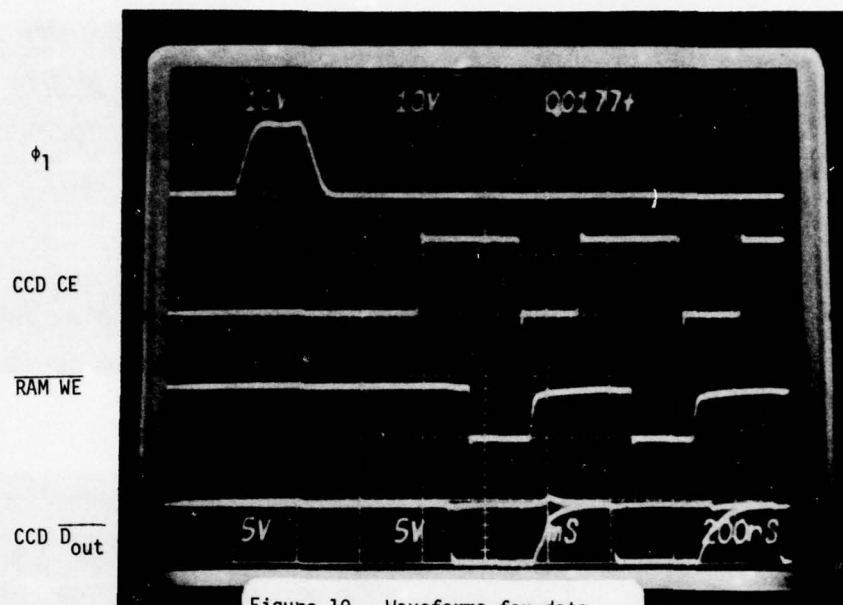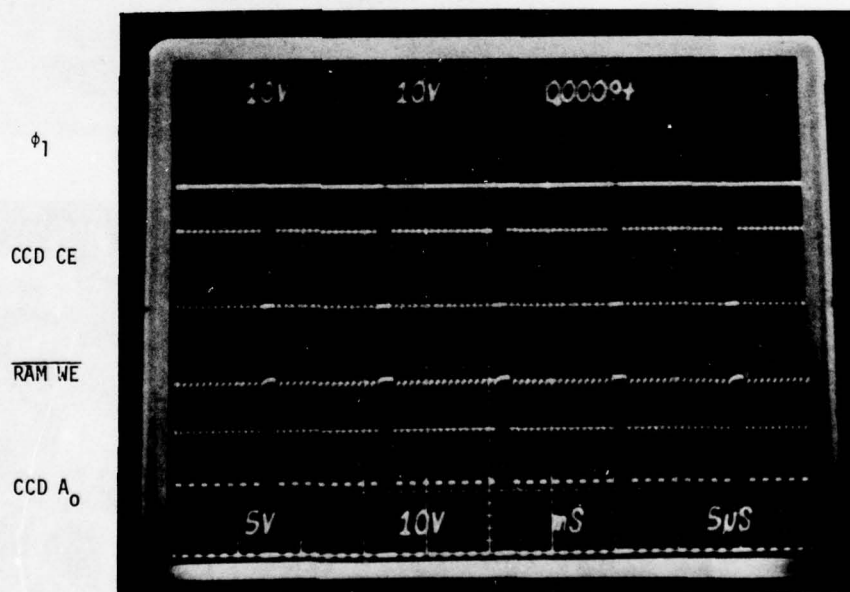input bandwidth of 40 MHz centered around 107 MHz, a maximum input signal duration of 3.5 μs, and an output clock rate of 100 KHz has been fabricated and tested. The SAW/CCD device consists of a lithium niobate ($LiNbO_3$) piezoelectric substrate, which functions as a SAW delay line, in close proximity (typically 300 nm) to an array of 300 sampling fingers connected to a 300-stage CCD on a silicon substrate. The output of the CCD retains both amplitude and phase of the input signal.

INTRODUCTION

New signal-processing capabilities are achievable by integrating a surface acoustic wave (SAW) device with a suitable CCD by coupling the piezoelectric fields associated with the surface wave directly to the charge in the CCD. Such a combination could make use of the advantages and compensate for the limitations of each of the two classes of devices. We report here the first step toward such a class of integrated SAW/CCD devices, a buffer memory device with wide input bandwidth and temporary storage capability. The fast-in, slow-out buffer memory device is shown in Fig. 1. It consists of a CCD shift register with parallel inputs connected to a set of sampling fingers, all on a single silicon substrate. The substrate is pressed against spacer-rails on a piezoelectric crystal with an acoustic delay line on its surface. The rails produce an air gap between the delay line and the CCD sampling fingers.
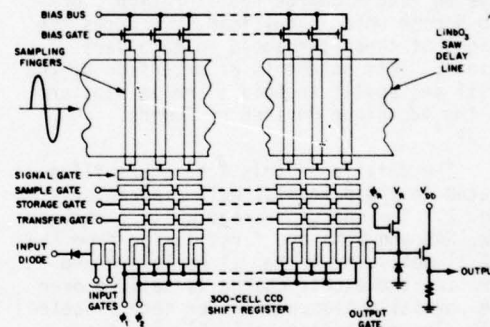
Fig. 1. Schematic diagram of an acoustoelectric SAW/CCD fast-in, slow-out buffer memory.

THEORY OF OPERATION

A schematic diagram of the device is shown in Fig. 1, and the sequence of device operation is as follows. Prior to the application of an input signal, the sampling fingers are pre-charged to the potential of the bias bus by means of the linear array of enhancement-mode MOS transistors. The sampling fingers are allowed to float by opening the bias gate, and a wideband data signal is applied to the input transducer of the SAW delay line. The piezoelectric RF field associated

with the acoustic wave modulates the potential on each of the sampling fingers and thus modulates the charge in a set of signal wells under the signal gates shown in Fig. 1. Charge is exchanged between these signal wells and a set of storage wells through a set of sampling wells. At the time when it is desired to capture the signal, the sampling gates are closed by an applied voltage step with a transition time which is short relative to one-half an RF period, and a sampled replica of the SAW waveform is now stored in the CCD storage wells. The transfer gate is then opened to parallel-load these charge packets into the CCD shift register, whereupon the data, which had been riding on the SAW signal, is shifted out in serial fashion at a rate determined by the CCD clock.

FIXED-PATTERN NOISE

The dynamic range of these devices is limited by fixed-pattern noise caused by threshold voltage variations in the CCD. We have devised a charge equilibration clocking scheme which significantly reduces the effect of these threshold voltage variations. This scheme is an extension of the "fill and spill" technique and is similar to the technique devised by Emmons, et al[1,2].

The details of this scheme are illustrated in the potential well diagram of Fig. 2. The charge storage wells (labeled SAW, SAG and STG) are first filled from the CCD $\phi 1$ wells. Next the $\phi 1$ wells are emptied and the excess charge is spilled over the partially closed transfer gate (labeled XG). The sampling gate (SAG) is closed momentarily in order to make the total charge independent of its threshold voltage. With the sampling gate open and the transfer gate closed, the RF piezoelectric displacement field causes charge to be exchanged between the two wells labeled SAW and STG. After the sampling gate is closed to capture the charge pattern resulting from the RF data signal, this charge pattern is transferred to the CCD by again partially opening the transfer gate and skimming off the signal charge from the storage well (STG) as shown at the bottom of Fig. 2. If some charge is left behind in the storage well, the output charge will be proportional only to the difference in charge, and will therefore be independent of all threshold voltages.
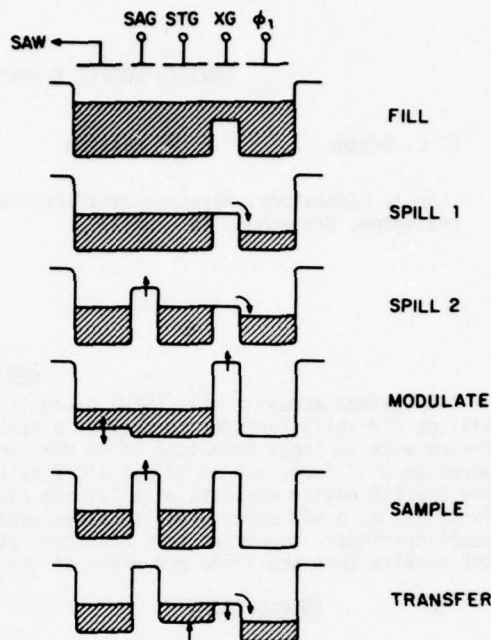
Fig. 2. Potential well diagram of the charge transfer states in the SAW/CCD device.

UNDER-SAMPLING

It is not necessary to recover the full spatial content of the piezoelectric wave if the input signal is of limited bandwidth, Δf. The required spacing of the sampling fingers can be determined by defining an effective sampling frequency, f_s, which is related to the spatial period of the sampling fingers, S_c, through the velocity of the surface acoustic wave, V_a, by

$$f_s = V_a/S_c \qquad (1)$$

S_c also defines the length of the CCD cell since there must be one CCD cell for each sampling finger. Since the input signal is contained in a limited band from $f_c - \Delta f/2$ to $f_c + \Delta f/2$, where f_c equals the center frequency of the input signal spectrum, the piezoelectric wave can be under-sampled at a frequency below the input spectrum as shown in Fig. 3a. With this sampling scheme,

the effective output center frequency is translated down by an amount equal to f_s.
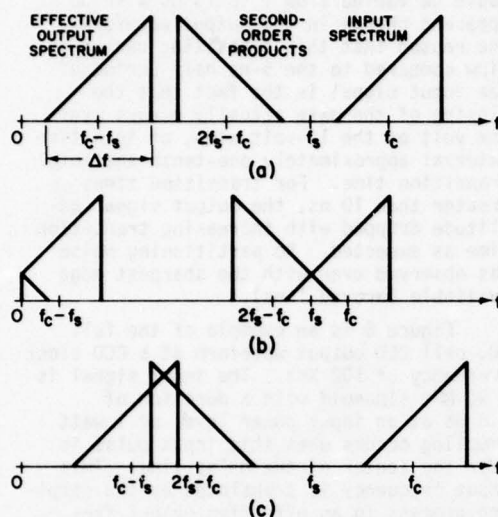
Fig. 3. Frequency spectrum of an input signal centered around f_c and under-sampled at a frequency f_s: (a) f_c acceptable, (b) f_c too low, and (c) f_c too high. Frequencies above the input spectrum are not shown.

The frequencies f_s and f_c must be chosen carefully so that the output sampled data stream from the CCD is an accurate replica of the input signal and does not contain undesirable signal distortions as a result of the sampling process. In sampled data theory such distortions are called "aliasing", or "frequency folding". Folding and spectral overlap can be seen in Figs. 3b and 3c. In the following paragraph, we will derive a set of inequalities which can be used to select f_s and to find the maximum bandwidth for a given f_s.

According to the sampling theorem, the effective sampling frequency must be greater than twice the desired information bandwidth

$$f_s > 2 \, \Delta f \qquad (2)$$

This relation can be used to select the effective sampling frequency. Once a samp-

ling frequency has been chosen, there are limits on the permissible range of input frequencies. The input frequency f_{in} cannot be below the sampling frequency:

$$f_{in} > fs. \qquad (3)$$

There is also an upper limit on the input signal frequency. Second-order mixing products (sidebands of the second harmonic of the sampling frequency) must not overlap the output spectrum (see Fig. 3c):

$$2 \, f_s - f_{in} > f_{in} - f_s \qquad (4)$$

Inequalities (3) and (4) can be rearranged into one relation for the acceptable range of input signal frequencies:

$$f_s < f_{in} < 3 \, f_s/2 \qquad (5)$$

This relation can be used as a guide in designing the SAW input transducer.

For our initial experiments we chose a convenient CCD cell size of 40.6 µm which defines f_s to be 85.7 MHz for a lithium niobate ($LiNbO_3$) delay line with a propagation velocity of 3480 m/s. This sampling frequency constrains the input signal to be in the range of 85.7 to 128.6 MHz for a maximum bandwidth of 42.9 MHz. A 300-stage device with this cell size is 12.2 mm long and has an acoustic delay time of 3.5 µs.

FABRICATION

A prototype device has been fabricated and tested; a photomicrograph of the die is shown in Fig. 4. It is 14 x 3.7 mm and is dominated by the 2.8-mm long polysilicon sampling fingers which dwarf the CCD shift register running along the bottom of the chip. A 2-phase, implanted barrier structure is used, with polysilicon for storage gates and aluminum for the barrier gates[3]. An n-type ion-implanted buried channel is used to ensure high-speed exchange of charge between the signal well and the storage well. Alignment marks are etched on the ends of the die for precise angular alignment of the sampling fingers with the wavefronts generated by the SAW transducers on the delay line. The finished die is attached to a specially fabricated header using a flexible sheet of Kapton so that it can be pressed against spacer rails on the

SAW crystal. Fig. 5 shows the SAW crystal mounted on a base and ready to be mated with the silicon-Kapton header sub-assembly. This assembly scheme is based on the technique developed for acoustoelectric convolvers[4], and is described in more detail elsewhere[5].

Fig. 4. Photograph of a 300-stage SAW/CCD buffer memory device. Die size is 14 x 3.7 mm.
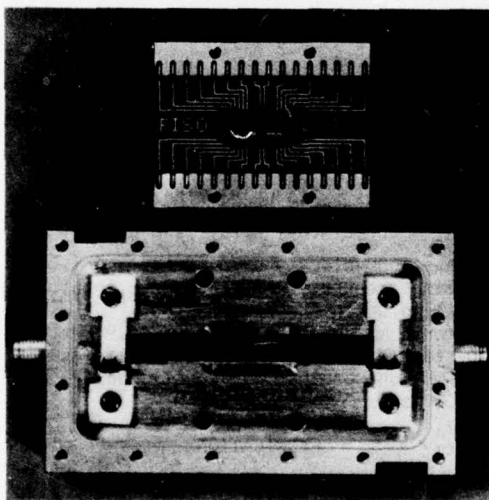

Fig. 5. Photograph of a partially assembled SAW/CCD device including silicon CCD die, Kapton sheet, LiNbO$_3$ delay line, and metal parts.

EXPERIMENTAL RESULTS

The prototype has been tested at a CCD clock rate of 100 KHz and at input signal frequencies between 80 and 130 MHz. From the sampling theory presented above, one would expect frequency folding to occur at 85.7 and 128.6 MHz. Frequency folding occurred in the prototype at 85.6 and 128.4 MHz, within 300 KHz of the predicted values. The output signal amplitude should be critically dependent upon the fall time of the 10-volt negative-going step applied

to close the sampling gate when the fall time approaches the 5-ns half-period of the input signal. In fact, this fall time could be varied from 1 to 10 ns with no apparent change in the output waveform. The reason that this transition can be so slow compared to the 5-ns half-period of the input signal is the fact that the closing of the gate actually occurs over one volt of the 10-volt step, or in a time interval approximately one-tenth the total transition time. For transition times greater than 10 ns, the output signal amplitude dropped with increasing transition time as expected. No partitioning noise was observed even with the sharpest edge available (around 1 ns).

Figure 6 is an example of the full 300-cell CCD output waveform at a CCD clock frequency of 100 KHz. The input signal is a 90 MHz sinusoid with a duration of 1.8 μs at an input power level of 1 watt. Sampling occurs when this input pulse is near the center of the delay line. This input frequency is translated by the sampling process to an effective output frequency of 4.4 MHz, which is the difference between the input of 90 MHz and the 85.6 MHz effective sampling frequency. As a result of this frequency translation, the sampled output waveform in Fig. 6 has 4.4 MHz x 1.8 μs = 7.9 cycles rather than the 90 x 1.8 = 162 cycles contained in the 1.8-μs pulse at the input. The amplitude
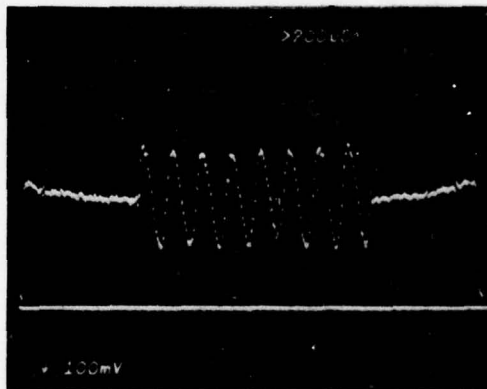

Fig. 6. Oscillograph of SAW/CCD buffer memory operation at an input carrier frequency of 90 MHz and an output clock rate of 100 KHz. The input pulse width is 1.8 μs.

and phase of the output signal tracks that of the input signal as expected. A clock generator to fully implement the charge equilibration scheme depicted in Fig. 2 is not yet available, so that excessive fixed-pattern noise is visible in Fig. 6. Even so, a dynamic range of 25 dB has been observed. With the more sophisticated clocking scheme, a higher dynamic range is expected.

CONCLUSION

We have used successfully the acousto-electric interaction between a piezo-electric surface wave and a silicon CCD to implement a fast-in, slow-out buffer memory function. This compact solid-state device serves to store wideband analog signals and read them out at a slow data rate. Devices of this type promise to provide wideband analog buffer memory functions for as many as 1000 discrete samples.

ACKNOWLEDGEMENTS

The authors wish to express their gratitude to D. J. Silversmith and R. W. Mountain for fabricating the CCD wafers, to L. L. Grant, D. M. Klays and I. M. Coates for assembling the packages, and to W. H. McGonagle for assistance in device testing. Thanks also go to Captain John Neff of AFOSR and to Fan King of BMDATC for their help and encouragement.

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A 1024-CELL CTD SHIFT REGISTER CAPABLE OF DIGITAL OPERATION AT 50 MHz*

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M. J. McNutt, W. E. Meyer

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ABSTRACT. We have recently designed and fabricated a 1024-cell CTD shift register that was successfully tested at 50 MHz. This is a peristaltic buried channel device that utilizes a dual channel 2 x 512 cell approach in which the channels are offset by 180° or two gates in the four gate/cell configuration. The offset provides automatic input and output multiplexing to allow 25 MHz operation in each channel while maintaining a 50 MHz total data rate. The individual cell has a 20 x 65 μm geometry designed to store 6×10^5 electrons and to transfer the charge at up to 100 MHz rates.

The four-phase clock voltages are provided by a tuned circuit with a Q of 10 that lowers the driver power from 4 mW/bit to 0.4 mW/bit. A correlated sampling circuit eliminates the clock interference and the charge transfer inefficiency (CTI) effects as well as amplifying the signal. The complete off-chip driver circuit also provides the input sampling and output reset pulses.

From the output signal test data, we determine a total CTI around 15% or a CTI/gate = 7×10^{-5}. The signal voltage is about 0.12 volts and the rms noise voltage is about 1 mV, yielding a signal/noise ratio of 120. This number combined with the total CTI suggests a bit error rate less than 10^{-100} in binary operation.

INTRODUCTION

The goal of this project was the development of a family of digital delay line devices suitable for use in a pipeline fast fourier transform convolution processor. Here we will describe the most elaborate device in this family, namely a 1024-cell CTD capable of 50-100 MHz continuous operation. The device is driven by an external driver with an output processor that eliminates the clock and reset signals picked up at the output and makes the output signal ECL logic compatible.

DEVICE DESIGN

The cross-section of a typical high speed silicon CTD fabricated at Rockwell is shown in Figure 1. This is the profiled peristaltic buried channel structure [1] that combines some of the charge storage advantage of the surface channel design with the transfer speed and efficiency of buried channels. The gate configuration is four-phase as shown with a two-level overlapping polysilicon structure. The bus lines feeding the gate arrays must be overlaid with aluminum, however, to ensure low RC charging time constants.

In this device, the charge is stored in the more heavily doped ion implant layer near the surface where it is most sensitive to the clocking voltages applied to the input and transfer gates. The completion of charge transfer from gate to gate, however,

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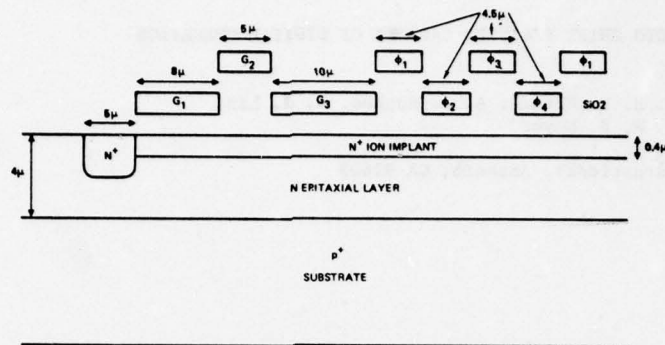
Figure 1. PCCD Input Configuration

takes place in the epitaxial layer well removed from the surface. This transfer region provides a high mobility layer free from trapping surface states where transfer-aiding fringing fields are near their peak. The so-called peristalsis analogy is apt because, during transfer, the charge is squeezed by the strong vertical field against the reverse biased junction at the N epilayer/P substrate boundary where the transverse fields are strong. Since the volume under the adjacent gate is a nearly empty potential well for electrons, the charge naturally flows into it.

Figure 2 contains a theoretical family of curves for the normalized transverse electric field versus distance below the gate at the gate center where the field drops to a minimum from the gate edges. This data comes from a solution of Laplace's equation (i.e. no mobile charge, fixed ionic charge treated by superposition) so it is most accurate for the transfer of the last increment of charge. This is the main point of interest for good transfer efficiency any-way, so this simple analysis has considerable relevance.

A gate width that is easily obtainable with the present projection alignment photolitho-graphy systems and can give some yield in a .1024-cell device is 4.5 µm. This produces a cell width, W, of 18 µm. The figure indi-cates that a typical epitaxial layer that is 4 µm deep (i.e. X_o = 0.22W) can give a peak

electric field that is about 75% of the potential maximum field ($\sim$V/W) at the gate
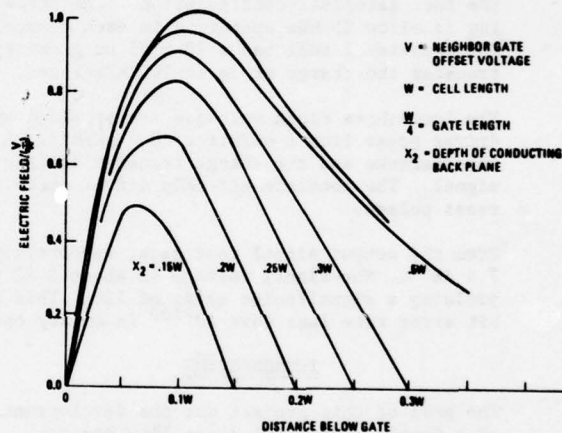
Figure 2. Normalized Transverse Electric Field at Center of Gate Electrode Operating in Four-Phase for Buried Channel CTD with Conducting Back Plane

center. V is the neighbor gate offset vol-tage. This peak field occurs about 0.1W or 1.8 µm below the gate, which happens to be the region in the epitaxial layer between the surface and junction depletion layer to which the charge is squeezed.

If we assume that V = 10v and V/W = 5.6 x 10^3 v/cm, a reasonable value for the field might be half this or 2.8 x 10^3 v/cm. At this field strength, the velocity of electrons in silicon is about 4 x 10^6 cm/s, so that the transit time across an 18 µm

cell is 0.45 ns. This suggests permissable clock rates approaching 1 GHz, but certainly 50–100 MHz is easily achieved with the 4.5 μm gate dimension. In fact, we have demonstrated the practicality of 1 GHz transfer rates in similar structures [2].

Figure 3 contains some calculations [3] of charge storage capacity versus the implantation dose in the profiled layer. This is a one-dimensional solution of Poisson's equation assuming two regions of constant doping density. The requirement for ECL logic compatibility gives an input voltage on the order of one volt. On the other hand, we must be able to saturate the charge capacity with an applied clocking gate voltage of around 10V. This will insure that the CTD channel can be pinched off to isolate the charge packets. From the figure, there is an allowable dose range of 0.75×10^{12} – 1.75×10^{12} cm^{-2} which satisfies these two conditions, so a design goal of 1.25×10^{12} cm^{-2} seems appropriate.

The calculations indicate that the storage capacity is fairly insensitive to substrate doping and epitaxial layer thickness and also to epitaxial layer doping in the 10^{15} cm^{-3} range. At a fixed voltage swing, the charge capacity decreases with increasing implant layer thickness, but not drastically so until the thickness approaches three times the minimum oxide thickness. That is the point where the oxide capacitance equals the pinched off semiconductor depletion capacitance. We want to get the charge as far away from the surface as possible for transfer efficiency, so an implant depth approaching 0.45 μm (i.e. 3 times the 0.15 μm typical oxide thickness) is a good choice. For a 1 volt input, this will give a charge capacity of about 10^{11} cm^{-2}, if the signal is slightly DC biased. An input storage gate 10 μm long x 65 μm wide will then provide about 6.0×10^5 electrons per charge packet, which will give adequate signal strength. In transfer, the charge is stored in effective storage lengths of $2 \times 4.5/\sqrt{2} = 6.4$ μm when using four-phase sinusoidal clock drives, but the factor of 1.5 decrease from the input storage gate length is easily made up by the increased clock voltage swing (∿10V) in the transfer gates.

The input and clocking gate structure is shown in the cross-sectional view of Figure 1. The dimensions shown are the result of the charge transfer and storage
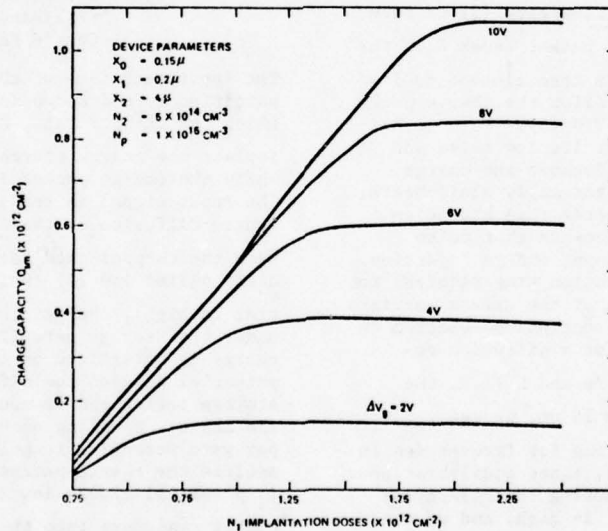

Figure 3. Charge Capacity Q_{sm} as a Function of N_1 Layer Implant Doses for Different Gate Voltage Swing ΔV_g; X_o = Oxide Thickness, X_1 = Implant Thickness, X_2 = Channel Thickness, N_2 = Channel Doping, N_p = Substrate Doping.

capacity analyses we have done. The input consists of three gates: G_1 is used optionally to provide additional isolation or gating of the N+ diffusion charge source; G_2 is a metering gate used as a backflow gate or a chopper gate; G_3 is the input charge storage gate.

The three available input techniques are shown in Figure 4. The first of these in Figure 4(a) is the very simple pulsed diffusion method whereby a signal raising the N+ source potential injects charge directly into the first transfer gate. The input gates are biased to turn on the channel. This method is simple to operate but does not provide a well-defined charge packet or sample aperture. The second input technique in Figure 4(b) is the fill-and-spill or charge equilibration method. Here the input signal is applied to either G_2 or G_3 while the other input gates are fixed. The charge source is pulsed to a high potential (1) to fill the G_3 storage gate region with mobile charge. At this time, ϕ_1 is also at a high potential to help define the G_3 potential well. Then the source potential is dropped (2) and the excess charge under G_3 diffuses back over the G_2 backflow gate (3) to form a well-defined charge packet under G_3. The first transfer gate is then clocked to its low potential (4) to allow the charge packet to transfer into the CTD (5). This technique is widely used for its low noise and good linearity [4]. Because the charge packet is allowed to thermally equilibrate, input noise sources other than kTC noise are removed. These include shot noise associated with the input charge injection. However, the equilibration time required for the thermal diffusion of the excess carriers is obtained from the continuity equation to be $\tau_{th} = 4L^2/\pi^2 D_n$. For a diffusion coefficient $D_n = 25$ cm^2/s and L (i.e. the width of G_2 and G_3) = 15 μm, we get $\tau_{th} = 36$ ns. This is too long for frequencies in excess of about 5 MHz, since equilibration can only take place during the half cycle when the ϕ_1 potential is high, and we need at least $3\tau_{th}$ for good equilibration.
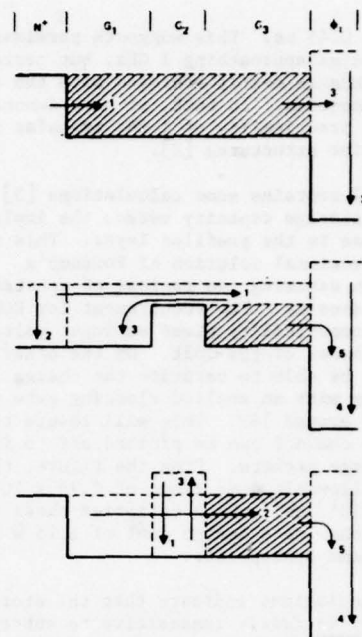
Figure 4.   Input Modes
(a)   Pulsed Diffusion
(b)   Charge Equilibration (Fill-and-Spill)
(c)   Charge Partition

The input technique of choice is the charge partition method shown in Figure 4(c), in which the chopper gate, G_2, is used to isolate the charge source from the CTD while the charge packet is being loaded. The input signal is applied to either the source diffusion or the G_3 storage gate.

When the chopper gate potential is periodically pulsed low (1) (while the ϕ_1 potential is high), charge flows into the region under the storage gate (2). The amount of charge is determined by the difference in potential between the diffusion and the storage region and is continuously tracking the input. Sampling occurs when the chopper gate potential is pulsed high (3) to isolate the charge packet just before the ϕ_1 potential clocks low (4) and the charge packet transfers into the CTD (5). The input shot noise is not fully equilibrated as it is in the charge equilibration input, but, as we will see later, this is not a

significant problem. The sample aperture is particularly small in this input technique and is determined by the rise time of the chopper pulse.

The speed of the charge partition input is very high, being determined by the field-aided injection time of the charge across G_1 and G_2. An experiment to determine this time is described in Figure 5 using a similar device. In the experiment, the CTD was clocked at a slow rate, and the injection time was controlled by a well-defined diffusion source pulse width. In the first example, a potential well was formed under the ϕ_1 and ϕ_2 gates during the quarter cycle when they are both at low potential. The pulse was applied during this interval to inject charge over the 30 μm barrier and fill the well. Any excess injected charge has time to flow back to the source after the pulse relaxes just as in a normal fill-and-spill. The relationship between the amount of charge in the well and the pulse width indicates the injection time required. In this case, the well saturates in about 21 ns.
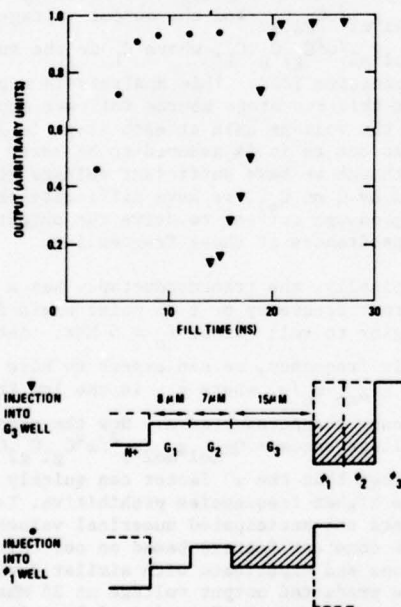

Figure 5. Input Charge Injection Time Experiment

In the second example, the well is formed under gate G_3 while the ϕ_1 potential is high. The charge is then injected 15 μm over the barrier and into the well. The injection time for the 15 μm injection distance is about 9 ns. In the design of Figure 1, the 13 μm injection distance under gates G_1 and G_2 suggests an injection time less than 9 ns from an extrapolation of the above results. This is within the 10 ns half-cycle window available in an input to be run at 50 MHz or below. Higher frequency operation can be achieved by narrowing or eliminating the G_1 gate which is usually only an optional addition.

The long, single channel CTD structure presents many problems, especially at high speed. The first of these is a long aspect ratio which would be about 280 for the active region 65 μm wide and 4.5 x 4 x 1024 = 18432 μm long. Even with the 5 mil bonding pads, scribe lines and bus lines all located on the short dimension, the chip aspect ratio would be about 40. Also the long dimension would be nearly 2 cm which is too long for routine step-and-repeat mask making. Serpentine structures used to alleviate this problem at low frequencies do not work well at high frequencies due to poor transfer at the corners. Another problem related to the *length is the* amount of bulk state trapping that occurs due to the large number of bulk impurities seen by a charge packet in its long journey down the channel. This trapping is the most important source of transfer inefficiency at frequencies below 100 MHz in these devices, and it also contributes significantly to the system noise.

A technique for reducing channel length by going to a dual channel arrangement is shown in Figure 6. The two channels employ overlapping gates to maintain matched characteristics and to minimize capacitance from additional gate clock bus lines. The key to efficient operation, however is the 180° (two gates) offset at the input and output that provides automatic multiplexing of the signal. Figure 6 concentrates on the input structure showing the common input to the two source diffusions. The G_3 and G_1 gates are also common to both channels, so only the G_2 chopper gates are separate. By operating the chopper gates 180° offset from each other in synchronization with the automatic offset of the first transfer

gates, alternate charge partition input sampling occurs.

The dual channel approach decreases the active region aspect ratio a factor of four and cuts the channel length in half. This also reduces by one-half the dominant bulk trap transfer inefficiency and the trapping noise. Because of the input and output multiplexing, the transfer frequency of the CTD is halved to maintain the data rate and time delay. This proportionately reduces the wideband power consumption in the circuits needed to drive the transfer gate capacitances.
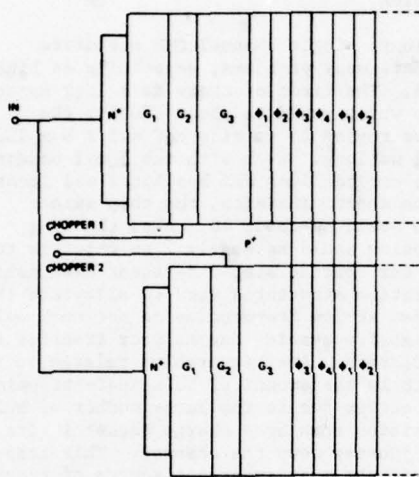

Figure 6. Self-Multiplexing Dual Channel Charge Partition Input

The output circuit used in this device is shown in Figure 7. It is an FET source follower with reset arrangement designed to drive a small capacitive load at the 25-50 MHz frequency required for each of the dual channel outputs. The inset in the figure illustrates the source follower FET which has a serpentine structure to provide a large gate width ($\sim$200 µm) with a short gate length (5 µm) in a limited chip area. This will give a large transconductance, g_m, with a high rolloff frequency, ω_o. After the CTD charge has been transferred to the output FET gate and the final transfer gate is at its high electron potential, the reset FET is turned on by applying a positive pulse to the reset gate. This drains the charge off

the output FET gate to the reset drain. Because of the channel offset the two channel outputs operate 180° out of phase with different final transfer gates, and the two outputs can be recombined off chip.

A simple gain calculation indicates the adequacy of this design. The AC source current of a MOSFET is given by $V_g g_m$, where V_g is the gate signal. The gate signal on the output FET is Q/C_{g1}, where Q is the CTD charge output and C_{g1} is the output FET gate capacitance plus a small stray capacitance. The reset FET is turned off when the charge is transferred onto the output gate, so it presents a very large impedance. Combining these results, the output FET source current is $Q g_{m1}/C_{g1}$ and the source follower FET gate signal is $Q g_{m1}/\omega C_{g1} C_{g2}$. C_{g2} is the source follower FET gate capacitance plus a small stray capacitance, and the assumption here is that the bias FET offers a small AC load by comparison. The output current can now be written as $Q g_{m1} g_{m2}/\omega C_{g1} C_{g2}$ and the output voltage is $Q g_{m1} g_{m2}/\omega^2 C_{g1} C_{g2} C_L$, where C_L is the output capacitive load. This analysis is accurate for this two stage source follower amplifier if the voltage gain at each stage is less than one as it is assumed to be here. Although we have sufficient voltage generated by Q on C_{g1}, we have difficulty obtaining enough current to drive the output load capacitances at these frequencies.

Typically, the transconductance has a corner frequency or 6 db point where it begins to roll off at $f_o \approx 5$ MHz. Above this frequency, we can expect to have $g_m \cong g_{mo} \omega_o/\omega$, where g_{mo} is the low frequency transconductance. Now the output voltage becomes $Q g_{mo1} g_{mo2} \omega_o^2/\omega^4 C_{g1} C_{g2} C_L$ and we see that the ω^4 factor can quickly make the higher frequencies prohibitive. Table 1 lists the anticipated numerical values of the constant factors based on our calculations and experience with similar devices. The predicted output voltage at 25 MHz per channel into a 5 pF load is 0.15 volts.

A photograph of the fabricated device is shown in Figure 8. It has 29 bonding pads, but requires only a 22-pin package, since
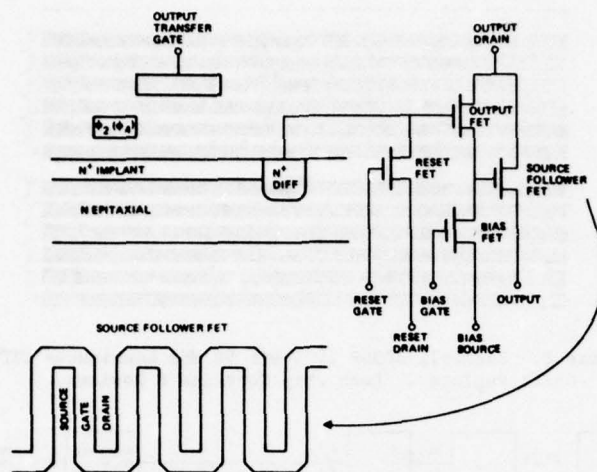
Figure 7. FET Source Follower with Reset Output Circuit
Showing Long Channel FET Source Follower Structure

some of the pins are bonded to two pads, each at opposite ends of the long device. This is required to minimize long bus lines and their associated RC time constants. Even so, aluminum must be deposited on the transfer gate polysilicon bus lines and on certain input and output lines to insure low resistance. The individual gates themselves, however, do not suffer from charging time limitations for frequencies less than 1 GHz. In the figure, the input is at left and the output is at the right.

Table 1. Output Transistor Parameters

g_{mo1} = 0.2 mmhos	f = 25 MHz
g_{mo2} = 1.0 mmhos	C_{g1} = 0.1 pF
Q = 10^{-13} Coulombs	C_{g2} = 0.5 pF
f_o = 5 MHz	C_L = 5 pF

DRIVER CIRCUITRY

The fundamental power requirement of the CTD is the power required to propel the charge packets down the CTD channel and make up their scattering losses. In buried channels, this real power is approximated by I^2R, where R is the channel resistance and I is the average CTD charge packet current, Qf. Even

though the power is proportional to f^2, it is still less than 1 mW in the 1000-cell device operating at 100 MHz. In practice, however, the main power loss is due to the reactive power given by $P = (C_G + C_{DL})V^2f$ required to drive the gate and drive-line capacitances, C_G and C_{DL}. V is the voltage swing and f again is the clock frequency. In a wideband driver, this power must be dissipated in the driver amplifiers. If the cell gate area is 65 μm x 20 μm = 1.3 x 10^{-5} cm^2, then C_G is about 0.2 pF/cell or about 200 pF in a 1000-cell device with gate oxides averaging around 2000Å. The bonding pads and drive-lines will add another 10 pF or so. For V=10 volts and f=100 MHz, the power requirement is about 2 watts, or 2 milliwatts per bit. If a 2 x 512 cell device is used, the driving frequency is halved and the power reduces to 1 watt or 1 milliwatt per bit.

If the CTD is to be operated in a continuous high speed mode at a single frequency, it is possible to utilize an inductor to resonate the gate capacitance and thereby reduce the power dissipation by an amount equal to the Q of the resonant circuit. A block diagram showing the resonant circuit driver is given in Figure 9, and the accompanying timing diagram is in Figure 10. The clock input is first shaped into a square wave by a differential amplifier and Schmitt trigger to

Figure 8. Rockwell 30309 1024-Bit 50 MHz Continuous CTD
Shift Register. Each Chip Contains 6 Devices.
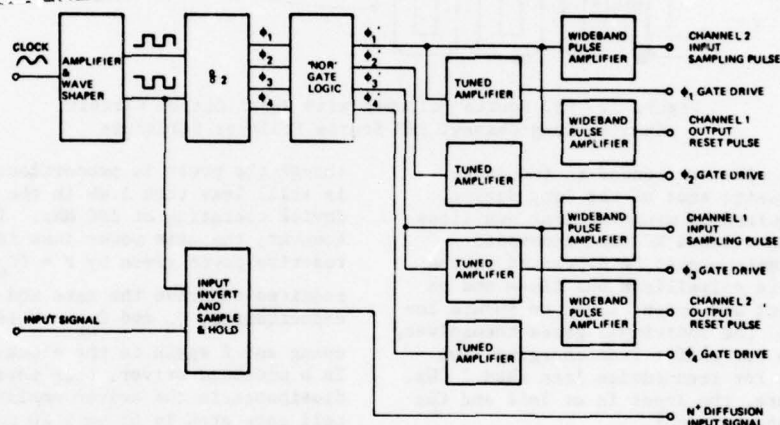
Figure 9. Block Diagram of CTD Test Circuitry Using
Tuned Gate Drive Amplifiers

permit a wide variety of driver input waveforms. The final amplifier in this series provides complementary outputs of the shaped and buffered square wave. These two square waves are then fed into a dual flip-flop divide-by-two circuit that gives four outputs at half the original frequency offset from each other by 90° phase shifts. The first two of these clock phases, ϕ_1 and ϕ_2, are shown in the timing diagram. In the next step, the four-phase square wave signals are gated through four "nor" gates to obtain the logical outputs denoted as ϕ_1'-ϕ_4' in the timing diagram. These are pulse trains in a four-phased array, and they are used to drive the transfer gate voltage amplifiers and the input chopper gate and reset FET

gate amplifiers.

The circuit diagram for one of the four channel gate amplifiers is shown in Figure 11. As stated earlier, it is designed to drive a tuned load consisting of an inductor, the CTD gate capacitance and a variable tuning capacitor. The output is a sine wave, as shown in the timing diagram, that peaks at the same time as the input pulse. This is accomplished by inverting the signal twice, once in a digital inverter and then again in the single transistor amplifier. The once-inverted pulse input to the PNP transistor turns it on when the CTD drive signal is near its peak. This means that the voltage across the transistor and, thus, its power dissipation is small and this tends to keep the Q

CLOCK

ϕ_1 = CLOCK/2

ϕ_2 = CLOCK/2

$\phi_1' \cdot \overline{\phi_1 \cdot \phi_2}$

$\phi_2' \cdot \overline{\phi_2 \cdot \phi_3}$

$\phi_3' \cdot \overline{\phi_3 \cdot \phi_4}$

$\phi_4' \cdot \overline{\phi_4 \cdot \phi_1}$
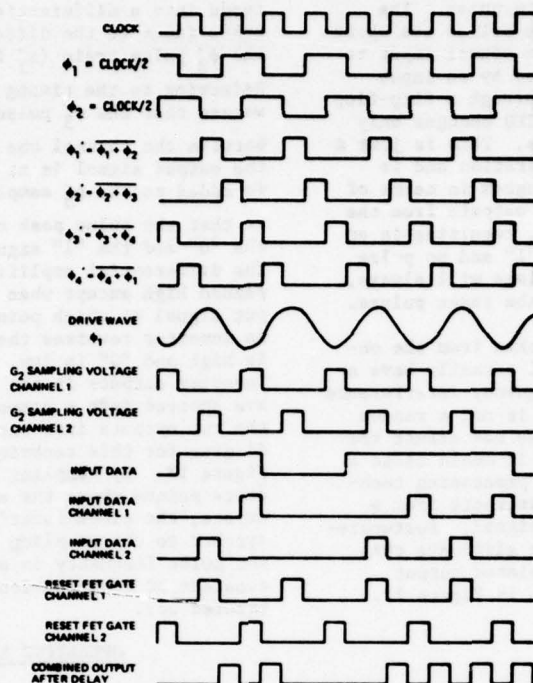
DRIVE WAVE
ϕ_1

G_2 SAMPLING VOLTAGE
CHANNEL 1

G_2 SAMPLING VOLTAGE
CHANNEL 2

INPUT DATA

INPUT DATA
CHANNEL 1

INPUT DATA
CHANNEL 2

RESET FET GATE
CHANNEL 1

RESET FET GATE
CHANNEL 2

COMBINED OUTPUT
AFTER DELAY

Figure 10. Timing Diagram for CTD Test Circuitry Using
Tuned Gate Drive Amplifiers

10Ω

100Ω

500Ω

-6.2 V

ϕ_n
PULSE
TRAIN

2N5583

300Ω

-6.2V

TO CCD
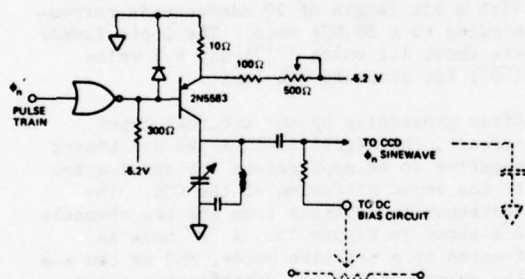ϕ_n SINEWAVE

TO DC
BIAS CIRCUIT

Figure 11. Tuned CTD Channel
Gate Drive Amplifier

of the circuit high. The pulsed transistor
output into the resonating load is analo-
gous to punching a damped oscillating
spring at appropriate intervals to maintain
oscillation. The transistor supplies the
power required to compensate for the finite
circuit Q. In practice, the Q of the tuned
load is about 20 and the Q of the entire

circuit is around 10. This reduces the
power consumption of the CTD channel gate
drive by a factor of 10 from 1 watt
(2 x 512 cells) to 0.1 watts and from 1
milliwatt per bit to 100 microwatts per bit.
The driver clock voltage is around 20 volts
peak-peak.

The inputs to the channel gate drivers are
also used in the output reset gate and
input control gate driver circuits. No
attempt has been made to tune these circuits,
however, because the load capacitances are
so small. These circuits are just simple
inverters cascaded into one transistor amp-
lifiers. The sampling voltages applied to
the two input control gates and the voltages
applied to the two output reset FET gates
in a dual-channel device are shown in the
timing diagram. Notice that the channel one
input sampling pulse train and the channel
two output reset pulse train are identical
to the ϕ_3^- channel gate pulse train. Also,
the channel two input sampling pulse and
the channel one output reset pulse are the

same as the ϕ_1^- channel gate pulse. The reset and sampling voltage pulses are about 4 volts in amplitude. The signal input to the system is also buffered by an input amplifier and processed through a flip-flop so that the input to the CTD changes only between sampling intervals. This is just a simple sample-and-hold operation and is depicted in the timing diagram in terms of an example. Finally, the outputs from the two channels are combined, resulting in an output pulse to denote a "1" and no pulse for a "0". The output pulses will always, of course, occur between the reset pulses.

The CTD output as it is taken from the on-chip output amplifier will normally have a large amount of clock frequency interference superimposed on it. This is not a random noise effect and so it does not affect the bit error rate. However, it could cause a problem in certain signal processing techniques downstream and it detracts from a potentially clean output signal. Fortunately, it is fairly simple to eliminate this interference using a correlated output sampler such as that shown in Figure 12.

Figure 12. Correlated Sampler and Amplifier Circuit for Output Signal

The CTD output signal is first amplified in a single one-transistor buffer circuit which feeds into a differential amplifier. The other input to the differential amplifier is the ϕ_3^- pulse train (ϕ_1^- for channel two).

Referring to the timing diagram in Figure 10, we see that the ϕ_3^- pulse occurs exactly between the channel one reset pulses when the output signal is at a peak. A DC bias is added to the ϕ_3^- sampling pulse and tuned so that the pulse peak occurs halfway between the "0" and the "1" signal output values. The differential amplifier output is always pinned high except when there is a "1" output signal at which point it is pinned low. An inverter reverses the signal so that "1" is high and "0" is low, and the two ECL inverter outputs in the dual channel set-up are shorted into a common load to combine the two outputs into one signal. The timing diagram for this technique is shown in Figure 13. By sampling the output at discrete points where the actual signal pulse exists, the clock interference which is synched to the sampling pulse and occurs at the pulse frequency is equivalent to a constant DC contribution and is simply subtracted out.

OPERATING RESULTS

Figure 14 shows a typical input of a repeated 16-bit word, namely 1100111100000000. The total word length is 320 nanoseconds with a bit length of 20 nanoseconds corresponding to a 50 MHz rate. The logic levels are about 1.2 volts ("1") and 0.3 volts ("0") for standard ECL logic.

After processing by the external input circuit, the signal is inverted and biased negative to be appropriate for application to the input diffusion of the CTD. The corresponding outputs from the two channels are shown in Figure 15. A "1" here is denoted by a negative pulse, and we can see the substantial clock interference superimposed on the signal. The upper trace is the channel one signal and the lower trace is the channel two signal. Figure 16 shows the final output after processing by the external output circuit. The signal has been inverted, the clock interference has been eliminated and the dual-channel output has been combined. Also, the signal size is an ECL compatible 0.8 volts. Finally, Figure 17 contains the input (upper trace) and output (lower trace) of the total system on a compressed time scale of 10 μs/div. Thirty-two (32) words of 16 bits each
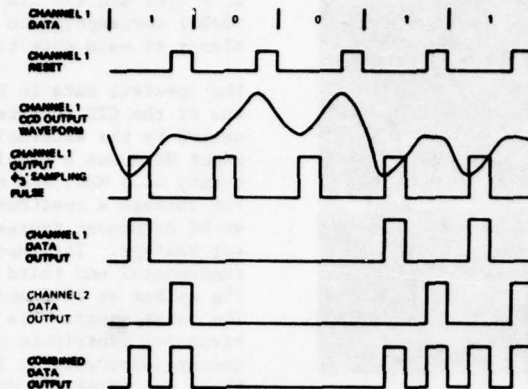
Figure 13. Timing Diagram for Output Signal Processor Circuit
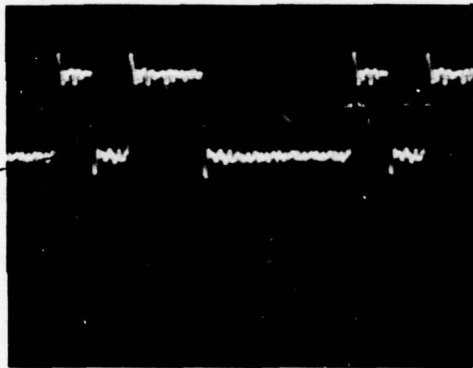

Figure 14. Oscilloscope Photograph
of 30309 Device Operation Showing
Input Data

Vertical Scale: 0.5V/Div.
Horizontal Scale: 50 ns./Div.
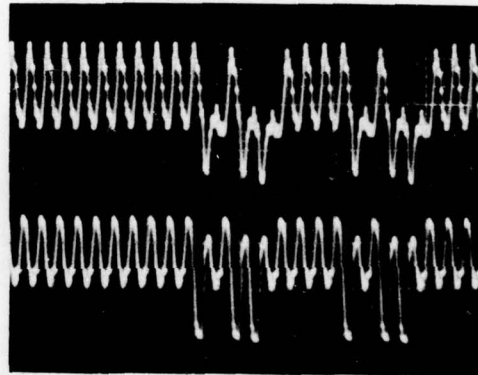Center Line: 0V

Figure 15. Oscilloscope Photograph
of 30309 Device Operation Showing
Dual Channel Output Data
("1's" Preceded by a String of "0's").

Vertical Scale: 0.1V/Div.
Horizontal Scale: 100 ns./Div.

separated by 32 completely zero words are
used to fill the 1024-bit storage capacity.
The input signal is similar to that of
Figure 14 which exhibits some high frequency
noise. This noise is contained in the deep
white bands of Figure 17. The output signal
is significantly cleaner, and of course, it
is delayed by 20.48 μs or the channel transit
time.

The worst case charge transfer inefficiency
(CTI) will occur for a "1" or full charge

packet preceded by a string of "0's". This
charge packet will not pick up any charge
left by previous packets to compensate for
its own transfer losses, and it must fill
bulk states that have been thermally empty-
ing for many periods. Therefore, we can
deduce CTI from the waveforms of Figure 15.
In channel one, the first "1" following many
"0's" is down about 17% from the "1" that
follows it. The "1" that follows another
"1" should have practically no loss because
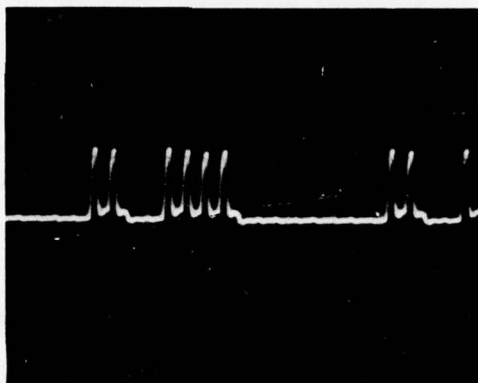it picks up the charge loss from the

Figure 16. Oscilloscope Photograph
of 30309 Device Operation Showing
Processed and Combined Output Data
from Figure 15.

Vertical Scale: 0.5V/Div.
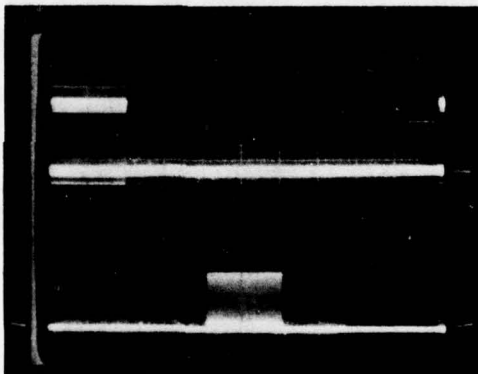Horizontal Scale: 50 ns./Div.

Figure 17. Oscilloscope Photograph
of 30309 Device Operation Showing
Total Shift Register Input
(Upper Trace) and Output (Lower Trace) Data

Vertical Scale: 0.5V/Div.
Horizontal Scale: 10 μs/Div.

preceding "1" to compensate for its own loss
and does not have to fill the bulk states.
Therefore, we can use it as a reference.
If the total transfer inefficiency is $\epsilon_T =$
0.17, the CTI per cell is $\epsilon = \epsilon_T/512 =$
3.4×10^{-4}. In channel two, however, the
results are somewhat better, and we get

$\epsilon_T = 0.07$ and $\epsilon = 1.4 \times 10^{-4}$. This latter
number corresponds to a transfer ineffi-
ciency at each gate transfer of 3.5×10^{-5}.

The spectral data in Figure 18 was taken at
one of the CTD outputs before it was pro-
cessed by the external output circuit. The
input data was a simple square wave of fre-
quency 12.5 MHz, and the output data was
run through a spectrum analyzer. The 0 Hz
or DC component represents the system off-
set voltage. The input square wave
fundamental and third harmonic give rise to
the spikes at 12.5 and 37.5 MHz respectively.
The input square wave second and fourth
harmonics contribute partially to the fre-
quency components at 25 and 50 MHz, but
these are primarily due to the sampling
and clock frequency at 25 (fundamental) and
50 (second harmonic) MHz. The magnitude of
the 12.5 MHz data output signal is about
0.12 volts as taken from Figure 15, so this
becomes the reference for determining volt-
age values from the spectrum analysis.

The white noise can be determined by exam-
ining the flat portion of the spectrum
above 25 MHz. In the figure, the noise at
high frequency is a constant 74 db below
the signal output. The spectrum analyzer
bandwidth is 100 KHz, so, if the data signal
power is $(0.12 \times 0.12/10^5 =) 1.44 \times 10^{-7}$
V^2/Hz, the noise power is $(1.44 \times 10^{-7}/$
$2.5 \times 10^7 =) 5.8 \times 10^{-15} V^2/Hz$. Integrating
over 50 MHz, the noise power is 2.9×10^{-7}
V^2 and the RMS noise voltage is 0.54 mV.

In addition to the white noise, there is
substantial 1/f noise at frequencies below
25 MHz. Since this 1/f noise amplitude
just about equals the white noise at 25 MHz,
in channel one it can be characterized by a
noise power voltage of $(5.8 \times 10^{-15} \times$
$2.5 \times 10^7/f =) 1.45 \times 10^{-7}/f V^2/Hz$. When
this is integrated from 100 KHz to 50 MHz,
we get a noise power of $9.0 \times 10^{-7} V^2$ or an
RMS noise voltage of 0.95 mV. Combining
the two noises gives a noise power of
1.19×10^{-6} or an RMS noise voltage of 1.1
mV. This noise plus the 0.17 total transfer
inefficiency implies a bit error rate less
than 10^{-100} at the 50 MHz combined data
rate and 2×10^{-2} at the 100 MHz rate. This
drastic change is based on the calculated
ω^{-4} drop-off in signal output. For refer-
ence, a bit error rate of 10^{-17} implies
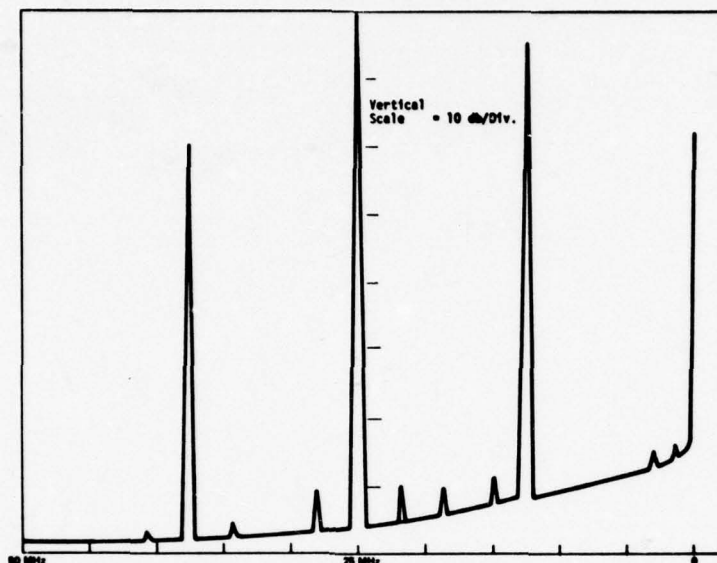less than one error per year at the 50 MHz
rate.

Figure 18. Spectrum Analyzer Characterization of CTD Output Signal

SUMMARY

We have presented design criteria and demonstrated the performance of a 50 MHz, 1024-bit CTD digital shift register. The typical device bit error rate appears negligible at this frequency. Although there is additional speed to permit increasing the frequency in the CTD input and charge transfer sections, the output circuit limits operation to 50-75 MHz. For transient data recorder schemes, where data is input fast, stopped and output slow, this is not a limitation, and we have achieved operation at 340 MHz (i.e. the ECL logic limit) in the laboratory. However, for continuous delay lines such as we have been discussing here, the output circuit speed will need to be improved. This will probably occur through the use of bipolar, V-groove or DMOS technology.

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DESIGN AND ANALYSIS OF NEW HIGH SPEED PERISTALTIC CCD'S

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ABSTRACT

Novel embodiments of silicon peristaltic CCD's for high speed operation are presented and analyzed. Included is a description of an input technique which shows promise of charge injection over a wide linear range at frequencies approaching 1 GHz. A nondestructive readout technique capable of greater than 100 MHz bandwidth, as well as on-chip drive circuits for reducing reactive power dissipation are described. Analysis is also presented showing that high speed transfer can be achieved with short gates and channel depths not exceeding several microns, allowing the buried channel to be implemented by ion-implantation rather than by epitaxial deposition. Such ion-implanted structures result in lower thermal leakage current than comparable epitaxial structures.

1.0 Introduction

Historically, peristaltic CCD's have been fabricated using an epitaxial structure[1]. Signal charge is confined in the epitaxial layer away from the surface in a region in which the electric fringe field between transfer gates is a maximum. The last fraction of charge under a gate is then efficiently transferred at high clock rates. *Charge transfer experiments using a uniphase clock have projected clock rates of ~1 GHz with charge transfer inefficiencies of ~10^{-4}[2].* However, devices taking advantage of such data rates have not been realized because of limitations resulting from the CCD input and output structures, efficient clocking techniques at high speed, and degradation due to leakage charge and charge transfer inefficiency arising from epitaxial crystal quality. The following paper describes new techniques which address these difficulties and present analytical results supporting projections of improved performance.

2.0 Analysis of CCD Charge Transfer Characteristics and Bandwidth

In the operation of charge coupled devices, the free-charge transfer characteristics are determined by incomplete transfer of charge due to: (1) insufficient transfer time, and (2) trapping of fast interface states and bulk traps. High-speed operation of CCD's pose interesting problems quite different from the conventional problems associated with input, clocking, and output of signal charge. At the present time, it is certainly not at all clear that low values of transfer inefficiency ($\epsilon < 10^{-4}$) can be maintained when the transfer time is reduced below 5 nsec and still provide distinct isolation of charge packets along the CCD delay line. As the electrode length L is decreased to shorten the characteristic transfer time (i.e., $\tau_c = L^2/\mu$ (1 volt), with μ an effective free carrier mobility), the potential wells that define and isolate the charge packets become "spread-out" in a two-dimensional sense. In order to counter this effect, the substrate doping density is increased which reduces the so-called fringe field that provides efficient charge transfer for the remaining 1 percent of the charge in a potential well. The reduction of fringe field is countered by locating the centroid of the remaining charge further from the Si/SiO_2 interface into the bulk silicon, thereby increasing the coupling of the drive clock voltages to accelerate the free-charge transfer. The result of this action is to reduce the charge-handling capability of the CCD structure which is countered by "profiling" and involves the use of a two-step doping process: (1) a shallow, heavy doped region near the silicon surface to increase the charge-handling, and (2) a deep, lightly-doped region to provide efficient transfer of the remaining charge. Therefore, there is a unique set of device parameters and material parameters needed to obtain a specified level of performance in high-speed operation.

There are three basic mechanisms of charge motion in the CCD structure: (1) self-induced drift, (2) thermal diffusion, and (3) fringe-field drift. The dynamics of free-charge transfer (i.e., transfer in the absence of generation-recombination mechanisms) can be described by a one-dimensional charge transfer equation.[3]

$$\frac{\delta \rho}{\delta t} = - \frac{\delta}{\delta y} (\mu \rho E) \qquad (1)$$

where ρ is the charge density, E the total tangential electric field in the direction of charge transport, y, and μ is the effective free-carrier mobility.

The total electric field is composed of the following terms:

$$E = E_{sd} + E_{th} + E_{fr} \qquad (2)$$

where E_{sd} is a self-induced drift field given by

$$E_{sd} = - \frac{1}{C_{eff}} \frac{\delta \rho}{\delta y} \qquad (3)$$

and $C_{eff.}$ is defined by the expression,

$$\qquad (4)$$

$$\frac{1}{C_{eff}} = \frac{X_0 (eff)}{K_0 \epsilon_o} + \frac{d}{K_S \epsilon_o} \left[1 - \frac{\Delta d}{d} - \frac{Q_S}{2N_{ion}} \right]$$

with X_O the effective oxide thickness (e.g., for a dual-electric system X_O (eff.) = X_O + $(K_O /K_N X_N$ as in the case for $Si_3 N_4 /SiO_2$), and d is the distance from the Si/SiO_2 interface into the silicon, where the centroid of the charge is located. Δd is the width of the charge centroid, Q_s is the signal charge density, and N_{ion} is the effective donar concentration in the epitaxial or ion-implanted region. Equation (4) neglects the repulsive field effects due to the image force in the gate electrode. The thermal field component of the total electric field may be written as,

$$E_{th} = - \frac{kT}{q} \frac{1}{\rho} \frac{\delta \rho}{\delta y} \qquad (5)$$

and the fringe electric field is determined by the geometry, material parameters, and external clock voltage, and may be approximated by the expression[4]

$$E_{fr} (min) = \frac{\Delta V}{L} [e^{-\pi K_S \epsilon_o/3C_{eff.}L} \qquad (6)$$

$$-e^{\pi K_S \epsilon_o/C_{eff.} L}]$$

where $C_{eff.}$ is defined by equation (4) and ΔV is the voltage difference between the transfer electrode and the receiving electrode (L is the length of the transfer electrode). The minimum fringe field is important because for small channel lengths the remaining charge is confined to the center of the gate electrode where the fringe field is a minimum. Plotting fringe field along the channel length under a transfer gate electrode, a linear approximation to $1/E_{fr}$ (where $E_y = E_{fr}$) is observed which is useful in the evaluation of a single carrier transit time given by the expression,

$$\tau_f = \frac{1}{\mu} \int_0^L \frac{dy}{E_F (y)} \cong \frac{L}{2\mu E_F(min)} \qquad (7)$$

The important effect of the fringe field occurs after the initial charge profile is relaxed and within 800 psec, since the charge transfer process becomes dominated by the fringe field term. In the early part of the charge transfer the self-induced drift may dominate for large charge densities (i.e., $\rho/q > 10^{10}$ cm^{-2}); however, within a nanosecond, the effects of thermal diffusion and fringe fields determine the final charge transfer. Thus, approximately 99 percent of the charge in a full well may be transferred by self-induced drift, but to achieve 99.99 percent transfer efficiency (i.e., transfer inefficiencies $\epsilon < 10^{-4}$), the thermal diffusion and fringe fields must be large. Fringe fields enable 99.99 percent transfer efficiencies (in the absence of trapping effects) to be obtained in several nanoseconds. The absence of fringe fields means the charge transfer process is determined by thermal diffusion with typical times of several hundred nanoseconds.

The effect of the fringe field may be included in the field enhanced diffusion constant[5] which may be written as,

$$D_{eff.} = D + \frac{2\mu L}{\pi} E_{fr} (min) \qquad (8)$$

Therefore, the time constant of charge transfer in the final stages is given as,

$$\tau_{eff.} = 4L^2/\pi^2 D_{eff.} \qquad (9)$$

The transfer inefficiency, ϵ can then be written as,

$$\epsilon(t) \approx e^{-t/\tau_{eff}.} \qquad (10)$$

where, in a two-phase clock structure, the time allotted for charge transfer is given by,

$$t(max) = (1/2)f_c \qquad (11)$$

with f_c as the clock frequency.

The analog signal transfer characteristic of a SI/SO delay line is a function of the product $Np\epsilon$, where N is the number of stages of delay, p is the number of transfers per stage, and ϵ is the transfer inefficiency. A useful criteria for defining analog signal bandwidth of a device is when the signal amplitude output suffers a 3-dB attenuation with respect to the input. This criteria can be shown to satisfy the relationship

$$Np\epsilon = 0.2 \qquad (12)$$

for a maximum baseband frequency component satisfying the Nyquist sampling criteria:

$$f_s(max) = BW = f_c/2 \qquad (13)$$

Therefore, combining equations (10) through (13) we have

$$BW = \frac{1}{4 \ \tau_{eff.} \ ln[5Np]} \qquad (14)$$

Finally, by combining equations (4), (6), (8), (9), and (14), the overall expression for the analog bandwidth (BW), in terms of the geometrical, material, and electrical parameters of the CCD structure, can be formulated:

$$BW = \frac{\pi^2 \mu}{16L^2 \ ln[5Np]} \ [kT/q + \frac{2L}{\pi} E_{fr}(min.)] \qquad (15)$$

where $E_{fr}(min.)$ is defined by equation (6). Table 1 illustrates the calculation of BW as a function of charge centroid "d" defined in equation (4) and illustrated in Figure 1, and the electrode length "L" for an 800-stage CCD with the fixed parameters indicated.

d (μm) L (μm)	0.2	0.5	1.0	1.5	2.0	2.5
7.0	82	103	128	145	155	161
5.0	204	246	291	313	319	375
4.0	365	428	484	496	487	---
3.0	753	844	885	849	---	---
2.0	1910	1990	1820	----	----	----

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Table 1
Bandwidth of a CCD Analog Delay Line in MHz as a Function of Gate Length and d

N = No. of stage delays = 800
p = No. of transfers/delay ≈ 4
ΔV = Effective channel mobility of electrons
  = 1,000 cm²/V-sec
X_O = Oxide thickness
  = 1700 A⁰
X_N = Nitride thickness
  = 500 A⁰
K_O = 3.85; K_N = 6.5; K_s = 11.8

The elements in table 1 are not completed for $d > L/2$ because the minimum fringe field $E_{fr}(min.)$ decreases after this point. The important features of table 1 are:
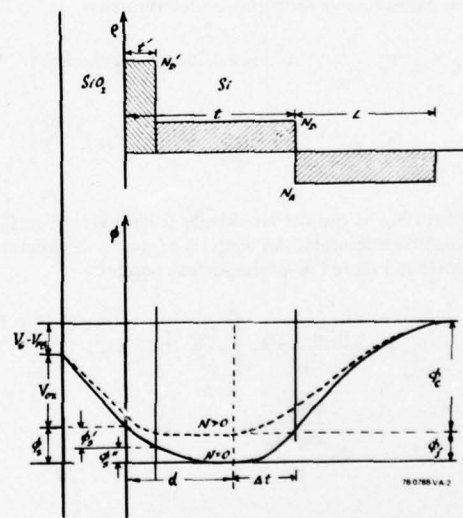
Figure 1. Energy Band Diagram and Potential Plot of PCCD with Profiled Channel

a. High-speed CCD analog delay lines with bandwidths exceeding 400 MHz are possible with 4 μm electrode lengths, 5-volt clock swing, and n epitaxial thicknesses greater than 0.4 μm, where the film thickness is approximately twice the centroid of charge, d.

b. Once the charge is removed from the Si-SiO$_2$ interface, the fringe field influence increases the bandwidth; however, the major contribution is achieved within 0.2 μm for the electrode lengths considered.

The design of the PCCD structure must consider the interrelationships between the geometrical, physical, and electrical parameters of the structure. Figure 1 illustrates the profiled PCCD structure and the designation of the geometrical and physical parameters. Summation of potentials yields:

$$V_G - V_{FB} = \phi_j + \phi_c - V_{ox} - \phi_s \qquad (16)$$

where

$$\phi_j = \frac{q N_D \Delta t^2}{2K_s \epsilon_0} \qquad \phi_c = \frac{q N_A L^2}{2K_s \epsilon_0} \qquad (17)$$

and

$$N_D \, \Delta t = N_A L \qquad (18)$$

The oxide voltage drop may be determined by

$$V_{ox} = \frac{1}{C_{ox}} \times \left[\text{mobile charge + fixed charge} \right] \qquad (19)$$

$$= \frac{1}{C_{ox}} \times \left[N_D (t - \Delta t - t') + N_D \, t' - N_o \right]$$

Where N_o is the carrier density (carriers/cm^2) in the potential minimum. An analysis of the band structure shown in Figure 1 gives the surface potential

$$\phi_s = \frac{q(t - t' - \Delta t)}{K_s \epsilon_0} \left[\frac{N_D}{2} (t - t' - t') - N_o \right] \qquad (20)$$

$$+ \frac{q N_D' t^2}{2K_s \epsilon_0}$$

$$\text{for } N_o \leqslant \frac{N_D}{2} (t - t' - \Delta t)$$

and

$$\phi_s = \frac{q N_D \, t'}{2K_s \epsilon_0} \left[t' - 2 \left(\frac{N_o - \frac{N_D}{N_D'} (t - t' - \Delta t)}{N_D'} \right) \right] \qquad (21)$$

$$\text{for } N_o > \frac{N_D}{2} (t - t' - \Delta t)$$

In the epitaxial PCCD structure, the epitaxial layer doping is variable because $N_N < N_A$ is possible, which confines the extent of the depletion region into the substrate. Figure 2 illustrates a potential profile plot of the epitaxial PCCD for a maximum change handling capacity of $N_{max} = 3 \times 10^{11}$ carriers/cm^2. The plots have been obtained by numerical evaluation of the above equations. Therefore, for an electrode area of 4 μm (length) x 50 μm (width), the total charge capacity is $7 \times 10^5 e^-$. The maximum charge is determined by the condition

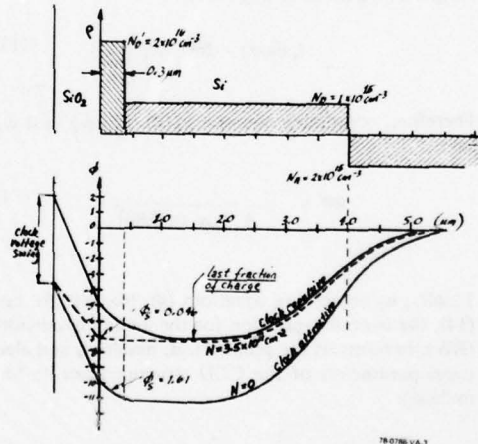$$\phi_s \geqslant 2 \left(\frac{kT}{q} \right) \qquad (22)$$

Figure 2. Epitaxial PCCD (Profiled): Dotted Lines Indicate Full-Well Profile

The last fraction of charge to transfer is located at 1.5 μm from the Si-SiO$_2$ interface and experiences the full magnitude of the electric fringe field. With reference to Table 1, this corresponds to a d = 1.5 μm and gives an analog bandwidth of approximately 500

MHz ($t_c = 1$ GHz) for an electrode length of L = 4 μm. The clock voltage swing is approximately 5 volts in this design analysis. An empty well has a surface potential $\phi_s = 1.61$ volts and after loading in signal charge to a level of 3.5×10^{11} carriers/cm^2 the surface potential drops to $\phi_s = 0.046$ volts or approximately $2kT/q$. This is sufficient to avoid the surface channel mode of operation where the device suffers a transfer efficiency degradation due to charge trapping at the Si-SiO$_2$ interface. As is to be expected, a suitable substrate bias is required to deplete the N region.

A method, which appears very attractive for the construction of PCCD structures, is the use of deep driven ion-implantation to form the channel.[6] This fabrication technique has been used extensively for shallow so-called buried channel CCD structures. An ion-implanted band diagram is shown in Figure 3 using a numerical evaluation for surface potential. In this structure N_D is greater than N_A because of the nature of ion-implantation and diffusion to form junctions by "over-doping" the substrate. The last fraction of charge to transfer is approximately 0.7 μm from the Si:SiO$_2$ interface, and we see from Table 1 that a 4 μm electrode length gives an analog bandwidth of approximately 430 MHz ($f_c = 860$ MHz). Thus, the ion-implanted approach provides the bandwidth and also the charge-handling as $N_O \approx 3.5 \times 10^{11}$ carriers/cm^2 is possible with the design illustrated in Figure 3. A clock voltage swing of approximately 5 V is employed in the potential profiles. As in the epitaxial structure a substrate bias is required to translate the range of clock swing to a suitable level compatible with analog ground in the system.
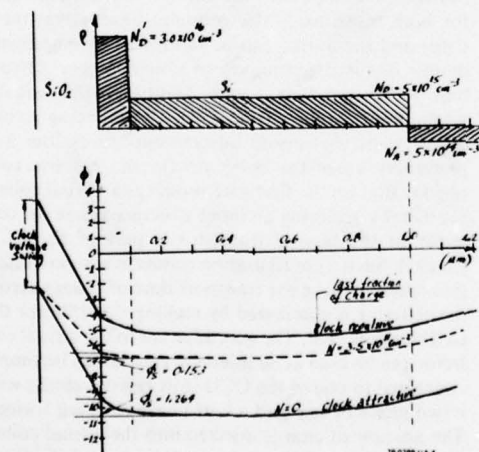

Figure 3. Ion-Implanted PCCD (Profiled): Dotted Lines Indicate Full-Well Profile

In order to achieve two-phase CCD operation, the ion-implantation profile must be adjusted along the length of the CCD device. The analysis performed above is for a full-well and a profiled PCCD. The profile ion-implant layer is adjusted to create a barrier to charge-flow in the reverse direction. With a 5-volt clock swing the barrier can be adjusted to permit 40 percent of full-well charge-handling capability.

The effects of charge trapping on surface channel CCD operation are well known to workers in the field. Analog signal processing requires a dc offset bias charge in the CCD well to enable the processing of bipolar signals. Therefore, the inherent bias charge left in the CCD well fills the interface states, which trap signal charge near the Si-SiO$_2$ interface. Nevertheless, the surface channel structure is still limited in signal processing because the fringe fields are small for reasonable electrode lengths. Therefore, for SI/SO delay line operation, bulk channel or buried channel operation is preferred due to the inherently more efficient transfer at high clock rates. The limitation to transfer efficiency in bulk channel CCD's is the number and location of bulk trapping states. In single crystal silicon, the number of bulk trapping centers is low on the order of 10^{11} - 10^{12} per cm^3, which leads to very high generation-recombination bulk lifetime (e.g., typically 100 μsec) and correspondingly low leakage currents (e.g., typically less than 10 nA/cm^2. The loss of charge due to bulk trapping may be analyzed as follows. When a sufficiently large charge packet enters under an electrode it rapidly fills all the bulk traps up to the conduction band edge. This fill time is strongly dependent on the signal size. In general, this process is extremely fast compared to conventional clock rates (i.e., < 10 MHz) when the charge packet is large. As the charge packet is transferred to the next electrode, the traps in the transfer electrode will re-emit a portion of the trapped signal charge, and this charge transfers along with the "main" signal packet. After the transfer time t, which is 1/1 f_c for a two-phase clock, any additional emitted charge goes into the trailing charge packet resulting in a loss of signal. The entire reasoning involved in this process is related to the filling and emptying of bulk traps. Bulk trapping states, in contrast with surface trapping states, are discrete and located within ± 0.1 eV of the middle of the energy gap; whereas, surface trapping states are continuous throughout the gap in density and distributed in time constants.

Although leakage current densities of the epitaxial or deep ion-implanted region are higher than virgin silicon, bulk traps are ineffective at high clock rates because they cannot emit in sufficient number to create a loss. Therefore, once the bulk traps are filled,

they are located so deep in the gap that they have insufficient time to release. This may be shown by writing the emission time of a bulk trap as

$$\tau_e = \frac{1}{\sigma_c N_t V_{th}} \exp\ (\Delta E/kT) \qquad (23)$$

where σ_c is the capture cross section of the trap, N_t the density of traps, and V_{th} the thermal velocity. ΔE is the activation energy of the trap which is near the center of the gap. If worst case numbers are used such as $\sigma_c = 10^{-15}$ cm^2, $N_t = 10^{16}$ cm^{-3}, $V_{th} = 10^7$ cm/sec, and $\Delta E = 0.45$ eV a value for trap lifetime is calculated:

$$\tau_e\ \text{(bulk traps)} \cong 0.5\ \text{sec} \qquad (24)$$

which is long compared to a transfer time of a charge packet at high speed. The loss of charge per transfer in the first signal packet after "M" empty packets may be written as:

$$N_{loss}(M) = V_{sig.} \sum_i N_{ti} e^{T/\tau_{ei}} (1 - e^{-MT_c/\tau_{ei}}) \qquad (25)$$

where $V_{sig.}$ is the volume that the signal charge occupies, N_{ti} is the density of the ith trapping state which has the emission time τ_e, T is the transfer time (e.g., $T = 1/2\ f_c$), and $T_c = 1/f_c$. Therefore, bulk trapping states responsible for increase in leakage current density cannot be responsible for the loss in the CCD at high frequency since their time constants are much too long to re-emit once they are filled. Equation (25) indicates that in order to observe such losses, the PCCD must be clocked at a slow rate and have a large number of empty packets such that $MT_c = 0.01$ τ_e.

A mode of PCCD operation for which this effect may have consequence is fast/slow clocking. This mode of operation is used for recording high speed transient data or high resolution radar signals. Since the ion-implanted deep driven structure has better physical properties (less defects) than a deposited epitaxial thin film, the former structure can be expected to yield lower leakage current devices with better transfer efficiency because of lower bulk trapping densities.

3.0 A Novel Bipolar CCD Input Structure with a 1-GHz Injection Bandwidth

The CCD input structure limits the maximum information bandwidth of the device. Therefore, any in-

put structure for high frequency CCD's must satisfy guidelines appropriate for high frequency operation. Specifically, the input structure must be made from high frequency components. The procedure for metering analog charge packets into the CCD well should involve only a single step because metering techniques requiring several steps require bandwidths several times larger than the bandwidth of the input signal. Moreover, the input signal level and the impedance of the input structure must be amenable for coupling *with the outside world. Cognizant of these re*quirements a new high speed CCD input structure has been designed which is amenable to coupling with the CCD shift register and does not require additional input clocking circuits. The new structure makes use of high speed bipolar transistor technology and high speed circuit theory for common base structures. Moreover, incorporation of a bipolar mirror into the input structure overcomes the problem of interfacing the input structure with the outside world. Consider the input structure shown in Figure 4(a) consisting of a double diffused lateral transistor and its mirror drawn, for purposes of clarity, outside the silicon substrate. In the actual device, the mirror transistor represented by the transistor symbol is monolithic with the transistor in the N layer. This input structure is referenced as a mirror circuit because when it is drawn in a symbolic representation (Figure 4(b)), it resembles a bipolar transistor and its mirror. Also, the relationship between the current I_M to I_{CCD} is proportional to the base-emitter junction areas of the two transistors because the base-emitter voltages are equal for both transistors. The common base lateral transistor and the mirror can be fabricated by employing double diffused techniques to obtain a very narrow base width (less than 1 μm). The base width will be smallest next to the virtual collector producing a condition where the current injected into the emitter will preferably enter the collector via the narrow base region. Bias on the first gate produces a virtual collector thereby achieving an input structure where the collector of the bipolar transistor is part of the CCD channel. Such a configuration results in a higher injection speed because the transport time of charge across the collector is eliminated by making the collector the CCD holding well. The gate adjacent to the virtual collector can be used as an injection gate or can be simply connected to one of the CCD shift register clocks with a two phase or one and a half phase clocking format. The amount of charge injected into the virtual collector's holding well depends on the value of the input current I_{IN} and integration (clock dwell) time. The input current is produced by applying a voltage via a resistor to the emitter mode. The injected current I_{IN} is then divided between the bipolar input transistor and its mirror.
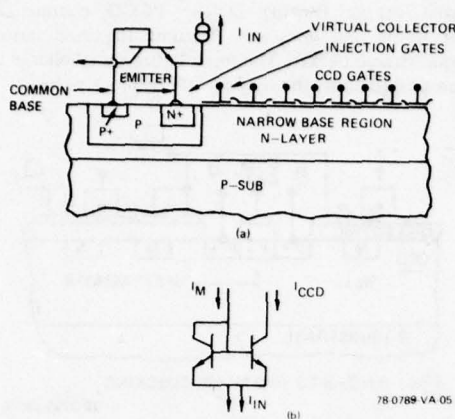
Figure 4. (a) Bipolar CCD Input Structure and (b) Circuit Diagram of Current Mirror
NOTE: The p-type base diffusion can contact the p-substrate without affecting the operation of the bipolar input structure

Experimental results on bipolar mirror structures show a precise current division according to the junction area over several decades of input current. Such a precise current division achieves two principal advantages: reduction of deleterious bandwidth effects by parasitic capacitance and reduction of the coupling difficulty between the CCD and an input signal.

Inherently, the CCD can accommodate only very low currents. Specifically, the current handling capability of a high speed CCD is in the 100-μA region. Generating such a low current level at high frequencies through low impedance lines is difficult and susceptible to induced noise currents by ac and dc offset voltages. Clearly, a higher level input voltage applied to the CCD's input structure should exhibit better noise immunity than low-level voltage signals. Moreover, reducing the input impedance of the CCD input structure yields a circuit less susceptible to bandwidth reduction by parasitic capacitances. Since the bipolar mirror input structure acts as a current transformer, a low input current into the CCD can be maintained while increasing the input current I_{IN} by applying a higher input voltage through a smaller series resistance, thereby achieving a wider input bandwidth. Typically, the base-emitter junction area can be made smaller than 100 μm by 4 μm while the mirror's junction area can be made 500 μm by 20 μm, resulting in a current attenuation of 16 to 1. The effect of the mirror transistor is to reduce the input im-

pedance at the emitter mode and reduce the effect of parasitic capacitances.

The operating speed of a bipolar transistor is determined by three regions: emitter frequency response, base transit time, and collector transit time. The emitter frequency response represents the speed with which the emitter-base voltage can change to accommodate a changing input current signal. A simple expression for the emitter frequency response (f_e) is the input transconductance (g_m) divided by the total capacitance (C_T) at the emitter node multiplied by 2π, i.e., $f_c = g_m/2\pi C_T$. The capacitance, C_T, is the sum of the emitter-base junction capacitance of the bipolar input transistor (C_B) and its mirror (C_M), and parasitic capacitance C_p. Note that capacitance C_M and C_B are proportional to each other by the ratio of currents flowing respectively through the mirror transistor and the bipolar input transistor by the emitter-base junction areas. Without loss of generality assume a proportionality constant determined by the ratio of the junction area to be 25. Hence, the CCD input current I_{CCD} will be 25 times smaller than the mirror current I_M. Substituting for g_m and C_T the following expression is obtained:

$$f_e = \frac{eI_{CCD}}{2\pi kTC_B}\left[\frac{1 + I_M/I_{CCD}}{\dfrac{C_p}{C_B} + \dfrac{C_M}{C_B} + 1}\right] = \frac{eI_{CCD}}{2\pi kT}x \quad (26)$$

$$\left[\frac{1}{C_B + \dfrac{C_P}{26}}\right]$$

Clearly, the effect of the parasitic capacitance (C_p on the input bandwidth at the emitter node is reduced 26 fold, a number equal to the current division of the input signal by the bipolar input structure. Hence, for a 100 μA CCD input current, an emitter area of 100 μm by 4 μm, base doped with 10^{18} boron atoms/cm^3 and emitter concentration higher than 10^{20} arsenic atoms/cm^3, an emitter frequency response of $f_c = 2.8 \times 10^9$ Hz is obtained. The large frequency response is due primarily to a 26-fold reduction of the parasitic capacitance. If the parasitic capacitance were not reduced, the emitter operating frequency response would be equal to 3.50×10^8 Hz. Therefore, the equivalent transit time for the emitter region is 3.60×10^{-10} sec. Using the diffusion equation, the transit time across the base, $t_B = 2 W^2/2.43 D_B$, for a 1 μm wide base (W) and 24 cm^2/sec for the diffusion

constant (D_B) is 3.5×10^{-10} seconds. Continuing the calculation for the transit time across a 5-μm virtual collector, $t_c = \pi L_c / V_s$, 2.6×10^{-10} sec are obtained as the minimum time required to transport electrons across the collector using a saturation velocity of 6×10^8 cm/sec for electrons. Summing all the transit times (emitter, base, and collector) a 1.03-GHz input frequency response for the bipolar mirror input circuit is calculated. Clearly, the input signal injection frequency is limited by the series input resistor and its shunting capacitor. With additional care, the 0.5 pF capacitor shunting the input resistor can be reduced, thereby achieving further improvements in the CCD injection bandwidth.

The calculations illustrated above have been refined using an ISPICE program, and the results are in good agreement with the above calculations.

4.0 High-Speed Nondestructive Readout (NDRO)

The accurate readout of analog charge packets from a high speed PCCD is a difficult problem. The usual output technique using a floating gate amplifier and a reset switch is found lacking because the output circuit bandwidth necessary for satisfactory operation is several times the signal bandwidth. This reflects the fact that several operations are required to reconstruct the input signal. Correspondingly, the noise associated with the wider band amplifier increases the noise contribution to the output signal. The nondestructive readout scheme presented in this paper is a novel approach for tapping a PCCD which overcomes the limitations inherent in conventional readout structures. The NDRO structure does not require a reset switch or several operations to reconstruct the input sample. Moreover, there is no floating readout diffusion which eliminates the $\sqrt{kTC}$ charge noise associated with setting and resetting the output diffusion.

The NDRO structure consists of a P-channel depletion - mode FET incorporated into the PCCD channel having its drain, channel, and source oriented transverse to the direction of charge flow (see Figure 5). Channel stops limit the width of the sensing P-channel FET and confine the signal in the CCD to flow under the charge sensing FET. Charge flowing in the PCCD channel passes under the sensing FET and modulates the FET's channel conductivity. Modulation is affected when the signal charge under the sensing FET decreases the depletion width at the P-N junction formed by the sensing FET and the N-type epi bias, thereby increasing the channel width (conductivity). Modulation of the sensing FET's conductivity by

signal charge flowing in the PCCD channel is monotonic and does not consume the modulation signal charge packet. The modulating signal charge is transported under the sensing FET by clock pulses.
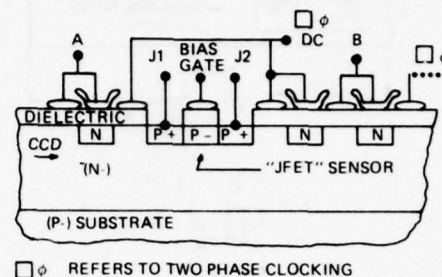
$\square \phi$ REFERS TO TWO PHASE CLOCKING

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Figure 5. Nondestructive Readout Structure for High Speed PCCD's

Two types of gates are incorporated around the nondestructive readout FET. The adjacent gates are dc gates and are used to shield the sensing FET from the clock pulses applied to the PCCD clocking gates. These dc gates are also used to adjust the dc potential of the PCCD channel to facilitate charge transport to and from the region located below the sensing FET. The ac clocking gate preceding the R/O FET (A) pushes the signal charge under the sensing FET while the succeeding gate (B) blocks, thereby confining the charge under the R/O FET. The charge injected under the R/O FET modulates the channel's conductivity to form an output signal dependent on the analog value of the charge packet. Charge is removed from under the sensing FET when the blocking gate (B) is pulsed attractive and the preceding gate (A) is maintained in the blocking state. After the signal charge is removed, gate (B) is returned into the blocking state and gate (A) is opened to let the next analog packet of charge into the sensing well under the R/O FET. Injection and removal of the signal charge from the sensing well is achieved at high speed because the dc bias or the readout FET produces a drift field to move the charge from under gate (A) to under gate (B). Also, the fringing fields induced by the voltage applied to gates (A) and (B) augment the transport of charge into and out of the sensing well. No $\sqrt{kTC}$ noise is associated with this R/O technique for there is no capacitor to charge and discharge as in conventional R/O structures. With exception of bulk trapping centers, the charge transport into and out of the sensing well should be complete. The noise associated with the R/O FET can be reduced by increasing the quiescent current flowing in the channel, thereby increasing the transconductance and reducing the noise voltage and sensitivity of the R/O FET.

5.0 On-Chip Driver Circuits

High-speed bipolar drivers on the PCCD chip reduce clock line interconnect capacitance, and are similar to typical ECL circuits.

There are two primary objectives for any on-chip clock driver circuit as shown in Figure 6. The first is low power dissipation and the second is the needed switching speed when driving the specified capacitive load. The illustrated circuit is composed of a differential ECL input stage and a push-pull type driver stage. Typically there could be four such driver stages, each driving 25 percent of the gates of the two-phase CCD to reduce the loading on each individual stage. This reduces the transient current which each driver is required to handle. If the circuit is switching at 800 MHz, total transient current of 0.9 A are typical. Using four drivers reduces the current per stage to 225 mA. The differential input stage is operated at +4 and −5.2 volts, making it totally ECL compatible. Therefore, all logic is dc coupled straight through to the CCD gates. The switching current is 7 mA, for a total dc power dissipation of 128.8 mW in the differential stage. Low power is achieved in a push-pull stage by not having any paths to ground directly from a supply and thus eliminating quiescent operating power. When the stage is in positive slew, the lower transistors, Q5 and Q6, are turned off and the only power dissipated is the transient current through Q7. When the capacitor is fully charged, the power dissipation goes to zero in the drivers. In the negative slew condition, Q7 is immediately turned off by the IR drop across the resistor caused by the collector current of Q5. Therefore, Q6 sees only the discharging capacitor current, and when the load voltage goes to zero, the only power dissipated is that across the resistor R3.
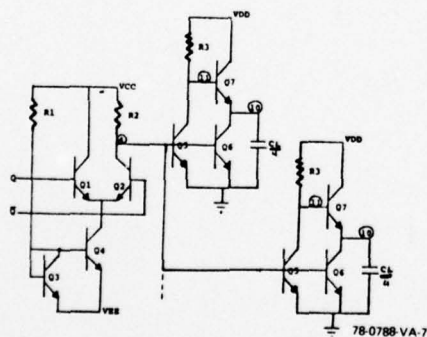
The high speed requirement is met by using a transistor to reduce the RC constant in the positive slew configuration, and a transistor to directly short the load to ground. This gives the lowest RC constants possible in both directions, to maximize speed. ISPICE simulation results (Figure 7) shows that the buffer is capable of operation in excess of 200 MHz.
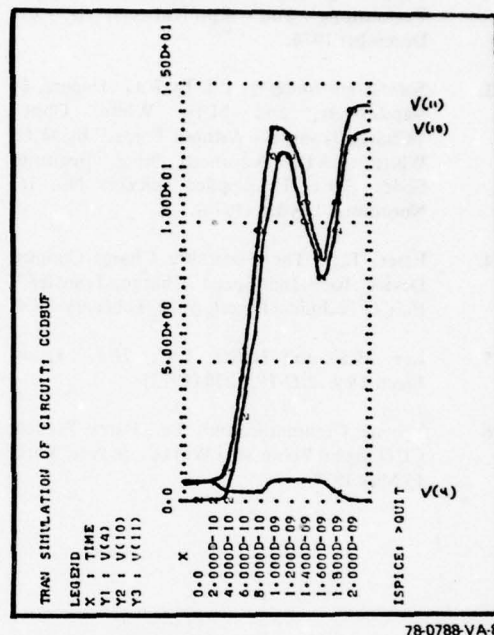

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Figure 7. ISPICE Simulation of On-Chip CCD Drive Circuit

6.0 Conclusion

New CCD techniques for achieving high-speed injection, transfer, and readout have been presented and analyzed. The high-speed bipolar current-mirror injection scheme allows an exact metering of small currents into the transfer structure and improves coupling to off-chip circuits by acting as a low impedance source. Analysis is presented that show high-speed transfer can be achieved without the use of submicron lithography.

The use of deep ion-implantation structures rather than epitaxial structures is proposed for improved leakage current performance. A unique nondestructive readout scheme is proposed that is effectively reset by the CCD clock requiring no additional clock waveforms for signal reconstruction.

78-0788-VA-7

Figure 6. On-Chip CCD Drive Circuit

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DISPLACEMENT CHARGE SUBTRACTION
CCD TRANSVERSAL FILTERS

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ABSTRACT

One-sided CCD transversal filters with a tap weight structure that eliminates the "common mode" sense electrode area (and minimizes the corresponding nonlinear depletion capacitance) are described. The resulting low-capacitance sensing nodes allow these filters to be input noise limited.

Differential amplifiers are not required when displacement charge subtraction (DCS) is used; it provides inherent signal differencing on a single node connecting all floating sense electrodes. Signal packets enter under some electrodes when other signal packets leave from under other electrodes, thereby causing signal subtraction. And because the ϕ_1 and ϕ_2 clocks overlap the sense electrodes equally, clock pickup is eliminated.

DCS in combination with the one-sided structure can be implemented by separating negative and positive tap weight sections by one half clock cycle. One-sided DCS matched filters have been fabricated and tested. Measurements of a 62-tap p-channel device indicate a 91-db dynamic range (rms signal-to-noise ratio for a 0.6-percent total harmonic distortion) and 68-db common mode rejection for the subtraction function without the use of a differential amplifier.

INTRODUCTION

Charge coupled device[1, 19] transversal filters (TVF)[2-6] have shown very impressive potential in the fields of visible and infrared signal processing,[7, 8] radar signal processing, [9, 11] communications,[12-14] and spatial image processing.[2,9] Their inherent low noise, coupled with current transfer efficiencies and current and near future precision lithography[28] provides a solid foundation for a truly revolutionary signal processing device family. However, conventional two-sided split electrode structures, though providing impressive performance characteristics, are subject to several limitations, such as limited signal-to-noise ratio (S/N) caused by excess sensing node capacitance, difficulties with clock pickup, poor common mode rejection due to capacitance imbalance of the sensing nodes, differential amplifier limitations, and marginal linearity (or complex linearizing and output sensing schemes). This paper introduces a unique combination of simplifications to the basic split electrode TVF configuration that substantially reduces these limitations and improves performance while conserving silicon area.

Single-phase clocking simplifies floating electrode voltage reference setting.[5, 6, 15] In conjunction with single-phase clocking, a one-sided structure eliminates excess nodal capacitance and thereby provides the largest possible signal amplitude by avoiding connection of the sensing node to any unwanted fractions of the split electrodes and associated unnecessary nonlinear depletion capacitance. With these simplifications, the dominant noise of the device can be limited to the CCD input noise with small contributions from other sources.[11, 16, 17] A one-sided structure also facilitates device layout. Additionally, displacement charge subtraction can be used to obtain precision subtraction without the need for

relative gain adjustment, and can thereby eliminate the need for output differential or instrumentation amplifiers.

Combining DCS with the single-sided structure results in small, precision signal processing devices that will require only a minimum of support circuitry and power and provide a high process yield potential. The operating frequency is not limited by differential amplifier characteristics.

ONE-SIDED CCD TRANSVERSAL FILTERS

Figure 1 illustrates a conventional two-sided TVF structure[2, 18] of width W, with N weighted electrodes (47 shown). For simplicity, the CCD register input and output circuits are not shown. The upper (negative) split electrode portions are both connected to the negative input of a differential amplifier; likewise, the lower split electrode portions are connected to the positive differential amplifier input. A SET switch is used for defining the potential of the sense electrodes (and associated surface potential thereunder) between samples. The sense electrode node clamping function is referred to as SETTING to indicate that the electrodes are "set" to a reference voltage. Each output summing node has an average capacitance C_2 nominally equal to $WNc/2$, where c is the capacitance per unit width of a floating sense electrode which involves neighboring electrode overlap capacitance in parallel with the series combination of electrode oxide capacitance and depletion capacitance (which for this discussion is assumed to be constant). For a CCD signal charge of $q*$ per unit width, the peak of the impulse response signal S_{P2} is $q* W/C_2$. Therefore, the peak impulse response signal is

$$S_{P2} = 2q*/Nc \qquad (1)$$

(and is independent of CCD width). This assumes C_A (amplifier and any added capacitance) is negligible.

As ϕ_1 rises (p-channel) charge is transferred over the d-c electrode potential and into the potential well that is forming under the floating electrode (see Figure 1c). At this time ϕ_{SET} is "off." Displacement currents flow through the depletion capacitance C_d to the substrate and through the oxide capacitance C_{ox} to the sense node and to the other electrodes, including the overlapping clock and d-c electrode capacitances. The resulting displacement charges are stored on the nodal capacitance and cause the sense node voltage to shift positively in proportion to the tap weight length (with nonlinearities of C_d).[2, 18-21] The bottom of the potential well also shifts in response to the voltage shift on the sense node. An examination of bit i of the structure shows that to obtain a small net positive signal, a large negative signal and slightly larger positive signal are processed and subtracted. The capacitance of the total signal is Wc, whereas the capacitance equivalent of the desired signal is $h_i Wc$, where h_i (≤ 1) is the weighting coefficient. For i (as illustrated) this coefficient is equal to about +0.3. All shaded areas in Figure 1b are involved in the outputs and contribute to sense node capacitance.

Figure 2 illustrates a one-sided TVF in which all excess electrode area has been eliminated by connection to a bias voltage V_{DC}. Only the shaded areas in Figure 2 are involved in its outputs. A stop diffusion is located under the split electrode gap region (see inset in Figure 1b). It must extend slightly under the surface d-c electrode region ahead in order to ensure that lateral charge transfer does not occur during the transfer of charge under the sense electrodes. The use of stop diffusions under the electrode gaps allows a variation in potential between the two sides, thereby greatly simplifying the output sensing circuit. The stop diffusion separator also improves tap weight accuracy.[23] Two limitations of this technique must be considered. First, nonlinearity of depletion capacitance causes distortion, which may limit the useful dynamic range in some applications. However the one-sided TVF minimizes the depletion capacitance (for a given signal) under the sensing node so that any added capacitance to the sensing node is more effective in reducing nonlinearities. The second problem is related to lateral charge transfer between sense electrodes. If lateral charge equilibration is not completed before the subsequent charge splitting operation, splitting precision is affected at high clock rates.[20-22] These two limitations are being investigated.
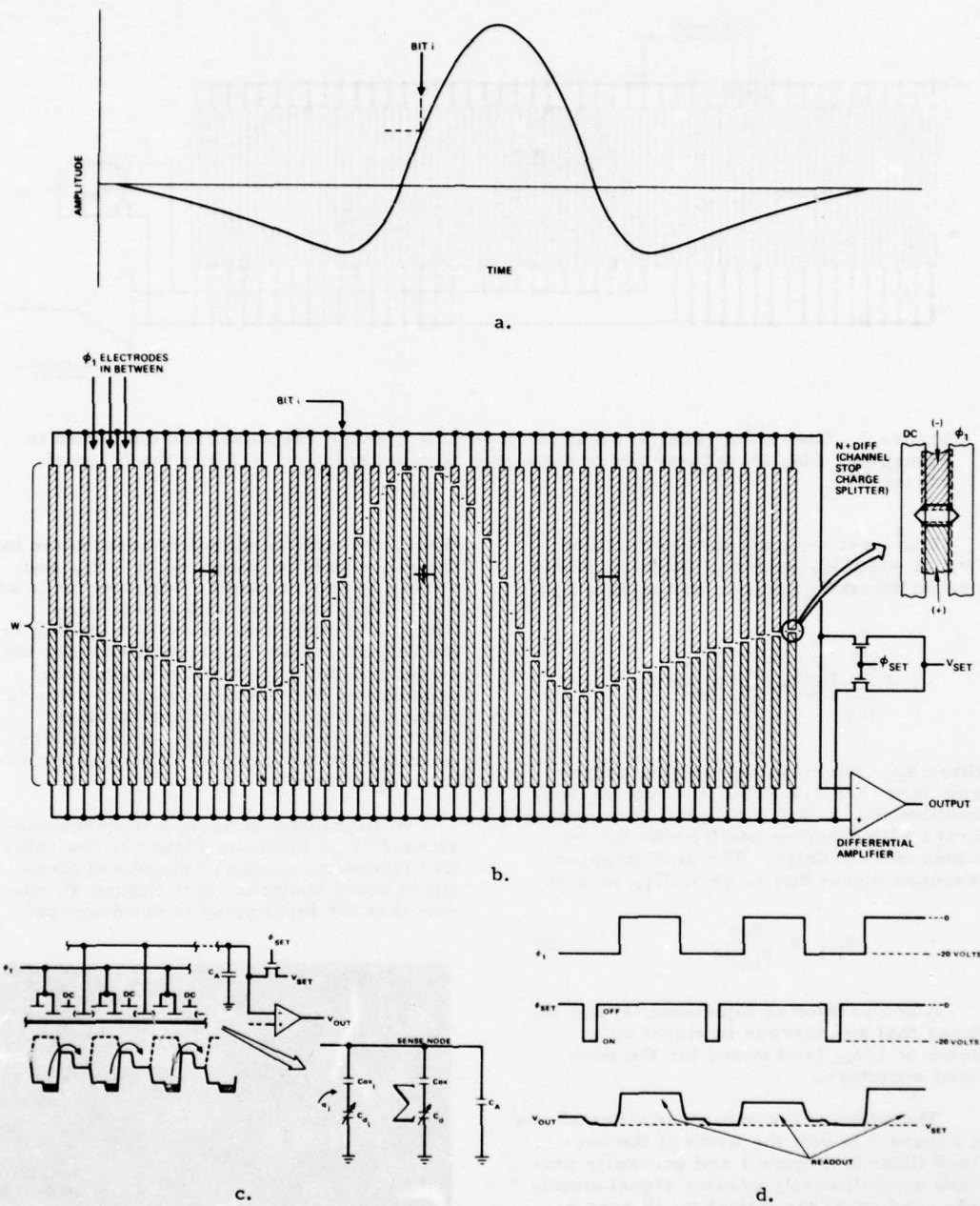
Figure 1. Desired impulse response waveform (a), conventional two-sided transversal filter, with stop diffusions located under electrode gaps (b), schematic/potential diagram (c), and clock waveforms (d).
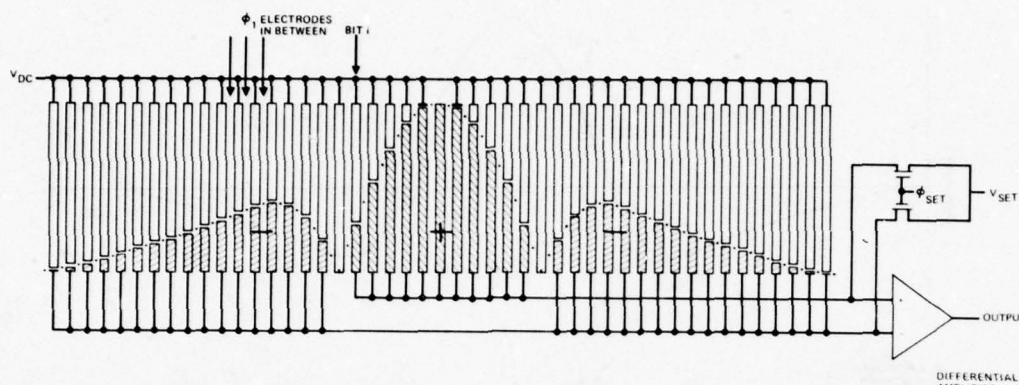
Figure 2. One-sided transversal filter providing impulse response function shown in Figure 1a, with about three times the signal amplitude (h_m = 0.33) of the filter of Figure 1(b).

For a zero d-c response one-sided TVF of width W, each tap weight node has a capacitance C_1 equal to (neglecting C_A):

$$1/2 \sum_{i=1}^{N} \left| h_i \right| Wc = h_m NWc/2$$

where h_m, the mean tap weight, ranges from less than 0.1 to 0.7 for typical filter functions (h_m = 1.0 for digital transversal filters with discrete coefficients having values of ±1.0 only). The peak impulse response signal S_{P1} is $q* W/C_1$, so that

$$S_{P1} = \frac{2q*}{h_m Nc} \qquad (2)$$

A comparison of Equations (1) and (2) shows that an increase in signal by a factor of $1/h_m$ is obtained for the one-sided structure.

The width of the one-sided filter shown in Figure 2 is half the width of the two-sided filter in Figure 1 and generally provides a significantly greater signal amplitude, and equal tap weight mask resolution. This increase in signal amplitude can in turn increase the signal-to-output amplifier noise ratio by $1/h_m$. For a one-sided filter equal in width to a two-sided

filter, the ratio of signal to reset noise for the sense node is improved by $1/\sqrt{h_m}$ and the tap weight resolution becomes twice as fine. As is the case with a two-sided filter, any additional capacitive loading in the output or clamping circuit reduces the signal and the S/N, but some additional capacitance may be necessary in order to reduce pickup from overlapping clock electrodes (non-DCS single-sided filters) or to reduce nonlinearity caused by depletion capacitance.

A microphotograph of a matched one-sided TVF is shown in Figure 3. The relative frequency response shape and measured noise spectrum (see Figure 4) indicate that the input noise is dominant and
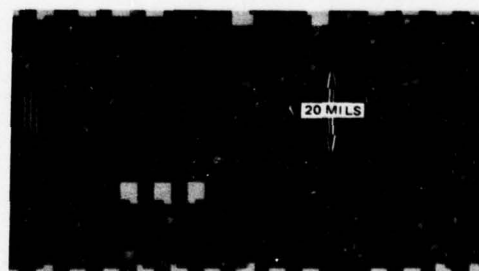

Figure 3. Microphotograph of a one-sided matched transversal filter (2091 chip).
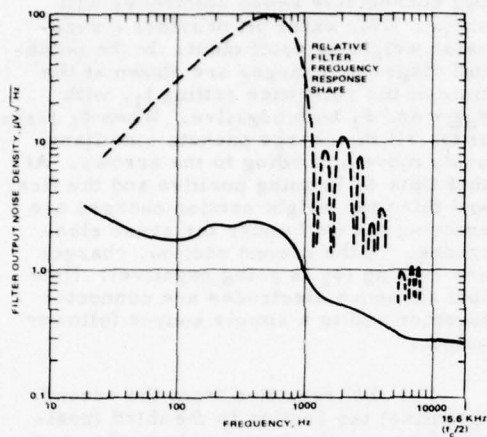
Figure 4. Relative frequency response and output noise spectrum of the one-sided filter of Figure 3.

can be clearly identified in the spectrum since it follows the frequency response shape. The noise integral of this curve is 79 μvolts rms. The filter output signal at its peak response point for low distortion was approximately 0.5 v rms, which provides a dynamic range of about 76 db (when measurements were made, no harmonic distortion data was taken).

DISPLACEMENT CHARGE SUBTRACTION

Figure 5a illustrates the charge flow with respect to a floating sense electrode whose voltage is "set" before the transfer of charge q_a (holes) under the sense electrode. After ϕ_{SET} goes off, ϕ_1 rises and charge flows according to the arrow, causing displacement currents to flow through C_d and C_{ox}. The resulting incremental voltage signal is positive for a p-channel CCD.
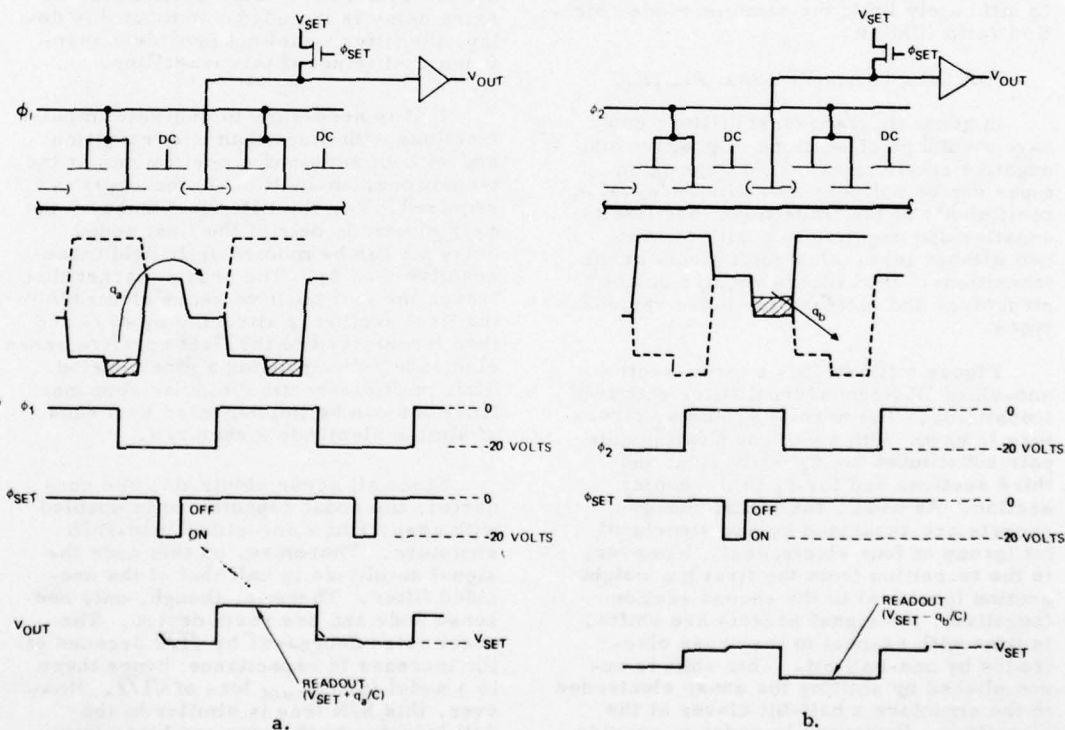
Figure 5. Displacement charge subtraction principle based on ability to set a floating gate voltage without signal charge underneath for positive excursions (a) or with charge underneath for negative excursions (b).

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In Figure 5b, ϕ_{SET} is timed to set the voltage of the sense electrode while charge q_b is in the potential well that is formed under this electrode (i.e., when the neighboring clock ϕ_2 is high). When charge is subsequently transferred, it leaves the region and thereby induces a negative incremental voltage signal. If ϕ_2 is established as the complement of ϕ_1, the two floating sense electrodes (of Figure 5a and 5b) can be connected and will provide an incremental voltage signal of $(q_a' - q_b')/C_T$, where C_T is the combined floating sensing node capacitance and q_a' and q_b' are fractions of q_a and q_b (each of which divide and flow partially through the depletion capacitance to the substrate and partially through C_{ox} to the sensing node). C_T is common so that q_a' and q_b' subtract with substantially zero common mode error, because when they are equal the surface potentials and depletion capacitances are equal, whether high or low. Second-order effects, such as total positive and negative electrode area differences, appear to ultimately limit the common mode rejection ratio (CMMR).

THE DCS TRANSVERSAL FILTER

In general, transversal filters can have a number of sections of positive and negative coefficients. Four transition types can be defined: two with zero-value coefficients at the transitions (positive to negative and negative to positive), and two without zero-value coefficients at the transitions. DCS filters require unique structures and clocking for these various types.

Figure 6 illustrates a three-section, one-sided DCS transversal filter with two transitions. The normal ϕ_1 and ϕ_2 structure is used, with a d-c and floating gate pair substituted for ϕ_2 in the first and third sections and for ϕ_1 in the center section. As usual, the signal charge packets are separated by one structural bit (group of four electrodes). However, in the transition from the first tap weight section (positive) to the second section (negative), the signal packets are shifted in time with respect to the sense electrodes by one-half bit. This shift is accomplished by shifting the sense electrodes in the structure a half-bit closer at the transition. However, in order to provide charge transfer, an additional one bit delay is needed at this transition; otherwise

two consecutive sense electrodes will occur. This extra bit provides a zero-value weighting coefficient. In the potential diagram, charges are shown at the time of the reference setting t_1, with ϕ_{SET} and ϕ_1 both negative. When ϕ_1 rises at t_2, all the charge packets simultaneously move according to the arrows. At that time ϕ_1 is going positive and the first and third tap weight section charges are entering the well under the sense electrodes. In the second section, charges are leaving (ϕ_2 is going negative). Note that all sense electrodes are connected together and to a simple source follower output.

For the transition from the second (negative) tap section to the third (positive) section, the floating electrodes are structurally a half bit farther apart. It is therefore unnecessary to add a delay bit at this transition to obtain charge transfer. To illustrate a symmetrical impulse response with a zero value coefficient, an extra delay is included. Without this delay, the filter would not provide a zero-value coefficient at this transition.

If it is necessary to generate impulse functions with more than one transition and without zero-value coefficients at the transitions, an additional clock $\phi_{1/2}$ is required. For the filter in Figure 6, the $\phi_{1/2}$ electrode pair of the first added delay bit can be momentarily held more negative than ϕ_1. The charge packet that leaves the last positive sense electrode in the first section is attracted by $\phi_{1/2}$ and then transferred to the first negative sense electrode without losing a clock period. Thus multiple-section impulse response functions can be implemented by means of simple electrode structures.

Since all sense electrodes are connected, the nodal capacitance is doubled with respect to a one-sided, non-DCS structure. Therefore, on this node the signal amplitude is half that of the one-sided filter. There is, though, only one sense node and one reset device. The reset noise decreases by $\sqrt{1/2}$ because of the increase in capacitance; hence there is a nodal $(S/N)_{reset}$ loss of $\sqrt{1/2}$. However, this S/N loss is similar to the S/N loss due to the rms combination in the differential amplifier of two reset noise sources of a non-DCS filter.
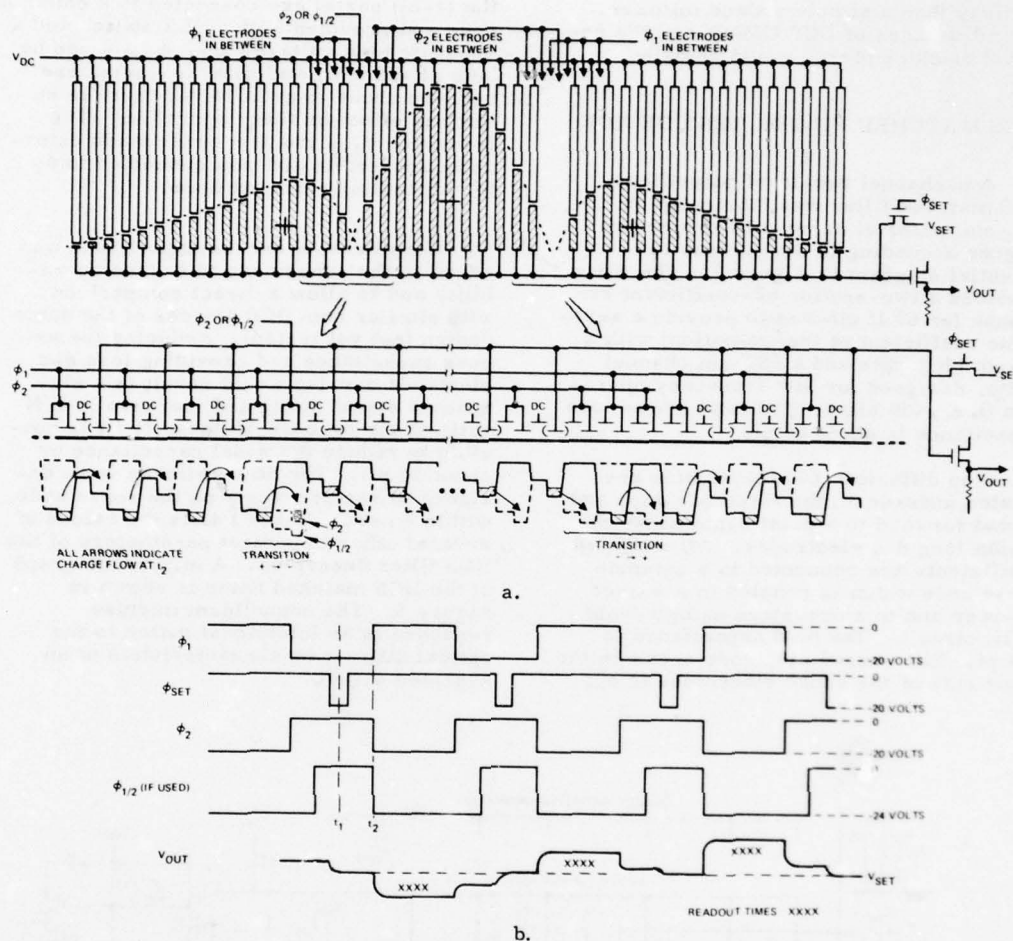
Figure 6. One-sided DCS transversal filter showing electrode structure and charge flow in (a) at time t_2 indicated in clock waveforms in (b).

For matched filters and bandpass filters that require zero d-c response, the sense electrode overlap of ϕ_1 and ϕ_2 will be equal in total length because $\Sigma + h_i = \Sigma - h_i$. Clock pickup is therefore substantially cancelled if the clock amplitudes and rise and fall times are equal. For filters requiring d-c response, simple coupling of the appropriate clock signal to the sense node can be used with only a small increase in sense node capacitance. Alternatively, a second, parallel filter with the impulse response function inverted and the input inverted (or V_{in2} rather than V_{in3} modulated) can be implemented with the sensing nodes of both filters made common. In this way the clock pickup will cancel for non-zero d-c response filter functions.

A single low noise operational amplifier charge integrator[19] can be used on the sense node if desired. This configuration minimizes the nonlinearity caused by depletion capacitance and it can be arranged to provide better thermal d-c

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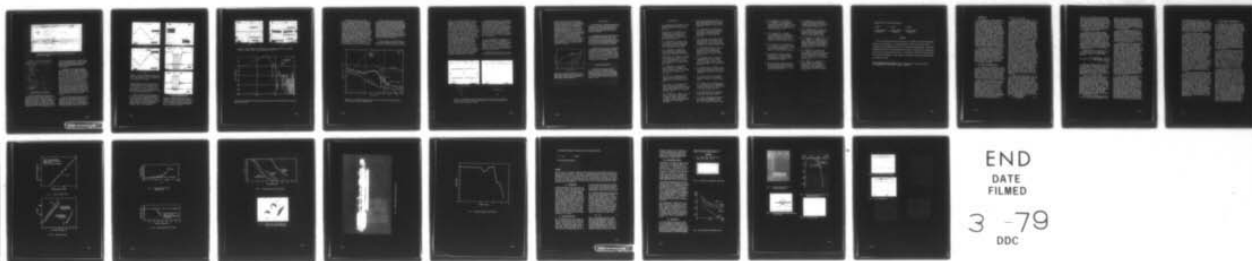
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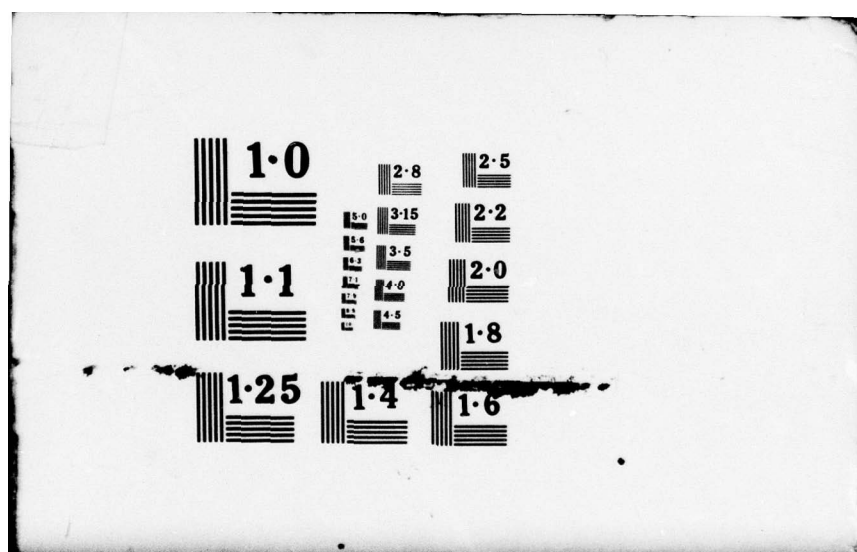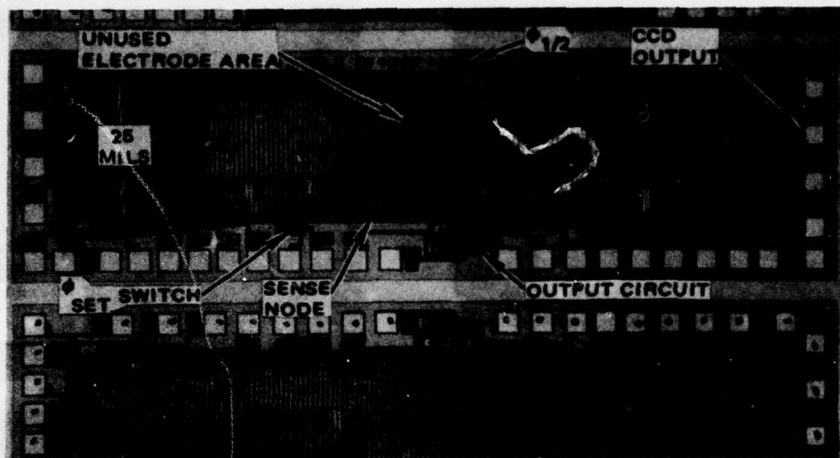
Figure 8. Microphotograph of DCS matched filter test
device (2155 chip).

TABLE 1. DCS Filter Parameters

Register: 68 bits, 62 tapped; 2-mil bit length, 25-mil channel width.
Capacitances, pf (calculated):

Input electrode (of V_{in3})		2.0
Sense electrodes	8.2	
V_{dc} overlap	31.3	
$\phi_1 \cdot \phi_2$ overlap	9.6	
Excess added (over stop diffusions)	16.1	
Miscellaneous	0.4	
Total sense node		65.6
CCD output diffusion		2.0
ϕ_{set} switch, μm	W = 120	
	L = 10	
Sample/hold		
Capacitor, pf		3.4
Source follower dimensions, μm	W = 68	
	L = 12	
Current source dimensions, μm	W = 48	
	L = 12	
Measured gain (overall S/H)	0.74	
Measured bandwidth with external cabling	100 kHz;	

EXPERIMENTAL RESULTS

The key parameters of interest were
cancellation of clock pickup, CMMR of the
subtraction function, distortion, noise
spectrum, and S/N. A charge equilibration
input was used with V_{in1} fixed at a large
negative potential, V_{in2} fixed and defining
the "fatzero" (with V_{in3} d-c level), and V_{in3}
modulated.[24,25] For higher gain, V_{in1}
can be used to define the "fat zero" with
V_{in2} biased highly negative. The primed
inputs, a summing input arrangement,
were simply paralleled for these
measurements.

In Figure 9, the impulse response
waveform with a zero-value coefficient at
the transition (a) is modified by shifting
ϕ_{SET} into phase with ϕ_2 thereby eliminating
the zero-value coefficient at the transition
(b). The pattern of the impulse response
matches the pattern seen in the chip photo.
Both cases are shown expanded in the
double exposure in Figure 10a where the
sample/hold circuit was disabled. The
zero-value coefficient is seen in the upper
trace at the center. Figure 10b shows a
clock-triggered, expanded, multiple-trace
filter output without the sample/hold oper-
ating with clock amplitude and rise times
and fall times misadjusted. In Figure 10c
clock amplitude and rise and fall times are
properly adjusted to eliminate clock
pickup.

The DCS filter step response is shown
in Figure 11a to illustrate overall wave-
form linearity and CMMR. The long-term
response to a step, as seen with a low-
frequency square wave, should approach a
constant value; this value can be estimated
from Figure 11b on the 5 mv/cm scale.

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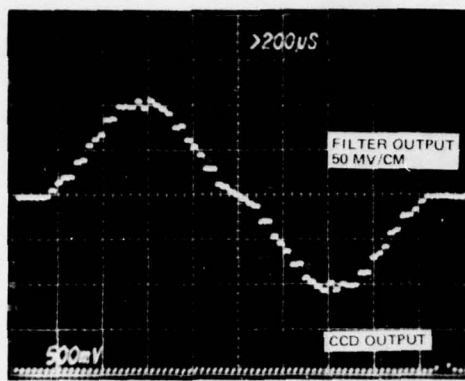
(a)
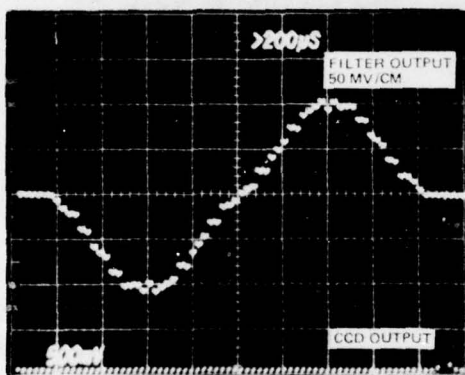
(b)

Figure 9. Impulse response waveforms of
DCS matched filter with (a) and without (b) a
zero-value coefficient at the tap weight sec-
tion transition; f_c = 20-KHz.

DVM measurements for an input d-c level
change providing a CCD output change of
1 volt (similar to the CCD output of Fig-
ure 11) caused a 0.6-mv d-c shift in the
filter output. This shift corresponds to an
equivalent common mode signal of 1.6 volts
and a resulting CMMR of 68-db.

Figure 12 illustrates the calculated
frequency response (tap weight digitization
round-off was not included) and the mea-
sured response for operation at a 20-kHz
clock frequency. Measurements were made
using an HP3325A synthesizer function
generator and a Quan-Tech 2449 wave
analyzer using a 7 Hz bandwidth.
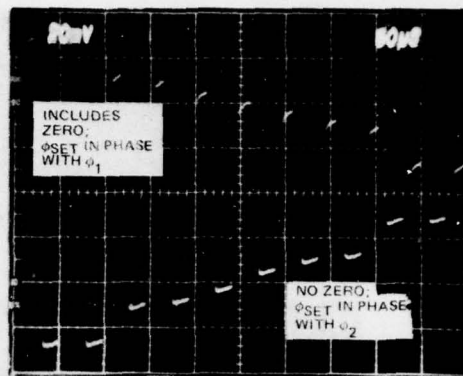
(a)   Filter Outputs
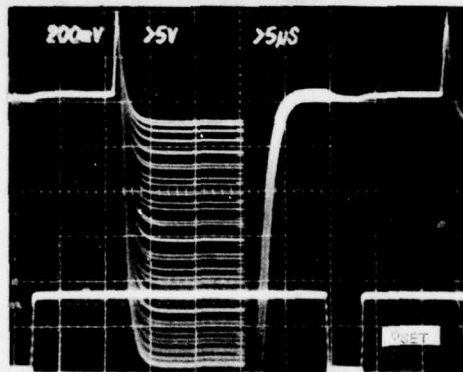
(b) Filter Output, No S/H
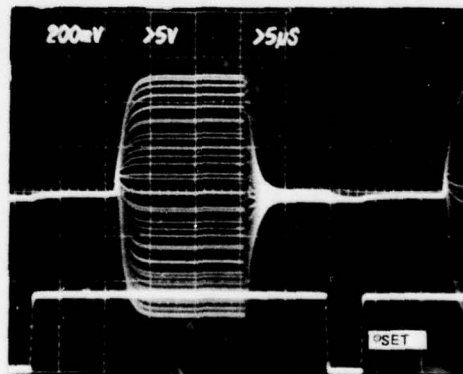
(c) Filter Output, No S/H
(ϕ_1 and ϕ_2 Matching)

Figure 10. Double exposure of transition
expanded   without S/H (a) and multiple
exposure showing clock pickup cancellation,
signal modulation and ϕ_{SET} clamping (b).
In (c), rise and fall times and amplitudes
have been properly adjusted.

(a)   (b)
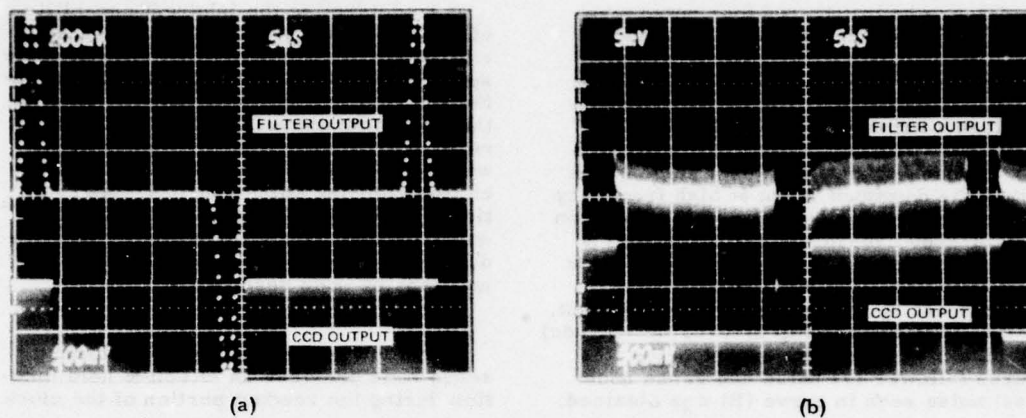
Figure 11. Step response of DCS filter showing general linearity (a) and CMMR
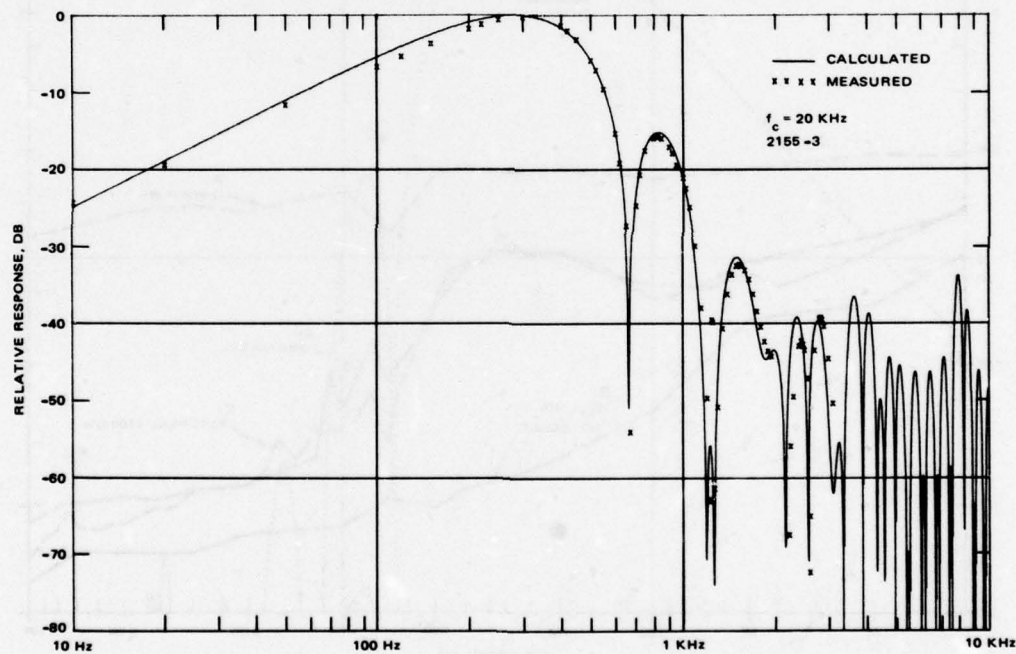with filter output vertical scale expanded to 5 mv/cm (b).

Figure 12. Calculated and measured frequency response of DCS matched filter operating
with a 20-kHz clock.

Figure 13 illustrates four noise spectral density measurements that were taken. The upper curve (A) corresponds to operation with the on-chip S/H and has an integrated value of 134 μv rms, which provides an rms signal to noise ratio of 78 db for a filter output of 1.06 volts rms (3 volts peak-to-peak). Reset noise of the S/H is the dominant noise at high frequency in curve (A). This measurement was taken using a X100 nanovolt amplifier (Keithley 103A) following the filter output to provide sufficient amplitude for a narrow band (7-Hz) noise spectral density measurement. By disabling the on-chip S/H (set to -20 vdc) and disabling all clocks except ϕ_{SET}, the source follower 1/f noise and sense node reset noise seen in curve (B) was obtained.

To determine the inherent capability of the filter, a discrete S/H was placed after the X100 gain amplifier and the noise spectrum (C) was found to generally follow the shape of the filter function, indicating that the dominant noise is no longer output reset or S/H noise, but CCD input noise with contributions from 1/f, FIS, and charge splitting noise sources. A reduction of sensing node capacitance and/or a small on-chip gain followed by a correlated double S/H would reduce the effective 1/f and sensing node reset noise.

The low leakage on the DCS floating sense node provides an effective hold function during the readout portion of the clock
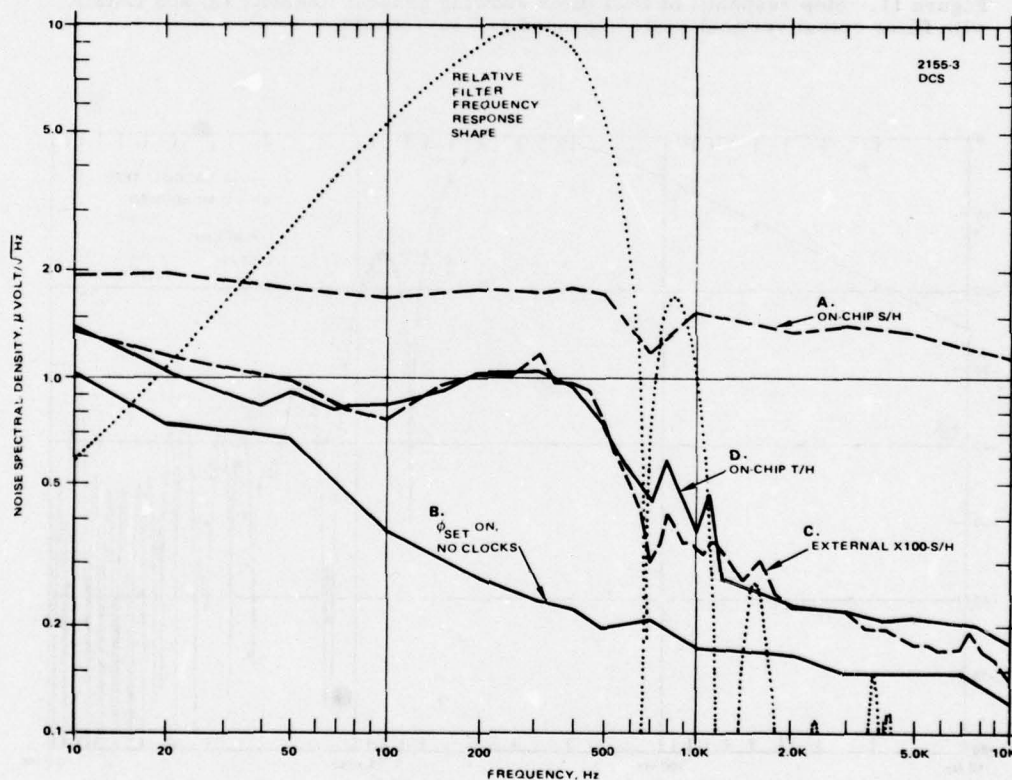

Figure 13. Noise spectral density curves of DCS matched filter operating with a 20-kHz clock, referred to filter output.

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cycle. To reduce the effective noise contribution of the sample and hold, it can be changed to a track-and-hold so that it is held ON as long as the readout signal is stable. Then the noise of the S/H is only in the output signal during the hold time and not during the track time. Furthermore, the clocking can be greatly skewed so that the ϕ_1, ϕ_2, ϕ_{SET}, and the input diffusion clocks all occur over a relatively short time (compared to that of Figure 10) with respect to the readout time. Thus the track time can be made large and the hold time very small (in low frequency applications). Figure 14 (a) illustrates the input diffusion, ϕ_1 and ϕ_{SET} clocks for track-and-hold (T/H) skewed clocking, along with the filter output with the S/H switch held ON at -20 vdc. Figure 14 (b) shows the same filter output when the S/H switch is provided a track-and-hold waveform as shown (it was necessary to couple a small complimentary T/H pulse to the filter output with a resistor and a capacitor to cancel the capacitive coupling of the S/H switch).

The reset noise only occurs during the short hold time and therefore eliminates most of the S/H noise contribution. This is demonstrated in Figure 13, curve D, which is the measured noise spectrum for the DCS filter using its on-chip sampling circuit as a track-and-hold; virtually the same input noise limited performance as curve (C) is shown. Integration of this curve to 10 kHz ($f_c/2$) yields an rms noise of 31.4 μvolts. For a 1.06-v rms signal, the S/N is 91 db.

The availability of compatible MOS differential amplifiers and support circuitry(23, 26, 27) should provide the capability for temperature stable outputs that include linear gain, correlated double sampling, and the track-and-hold function followed with a band-limited output buffer to further improve S/N.

Distortion measurements were taken by setting the input sine wave source and
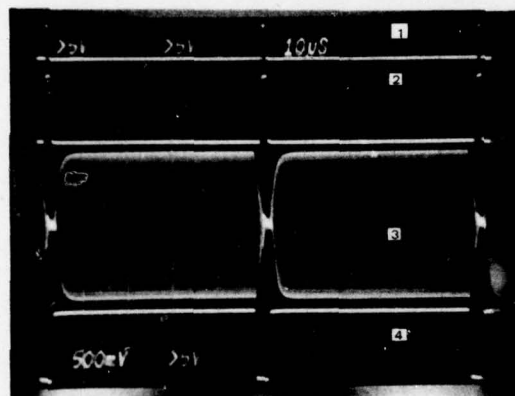
1) INPUT DIFFUSION CLOCK

2) ϕ_1 ($\sim \bar{\phi}_2$)

3) FILTER OUTPUT
   (NO S/H)

4) ϕ SET

(a)
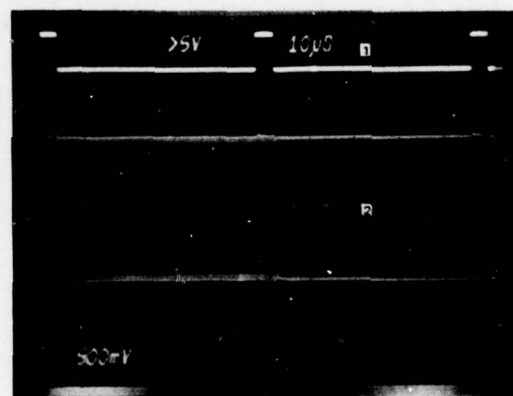
1) ϕ T/H

2) FILTER OUTPUT
   WITH TRACK AND HOLD

(b)

Figure 14. DCS filter outputs showing clocks for skewed clock arrangement used for track-and-hold. In (a) the S/H switch is at -20 vdc while in (b) it is driven with a track-and-hold clock.

the wave analyzer to the peak response frequency f_o of the filter, and setting the input for the desired filter output amplitude. The filter response was considered the reference zero db level. The input was then adjusted to $f_o/2$, $f_o/3$, etc. (with no amplitude change) and the harmonic distortion was measured at f_o. The "fat zero" to provide the lowest second-harmonic distortion for a 2.5 volt p-p fundamental was determined at the beginning and used throughout for all harmonics and input levels. The harmonic distortion is plotted in Figure 15 against filter peak-to-peak output amplitude. The rms combination of all harmonics for a 3-volt peak-to-peak signal is 0.6 percent.
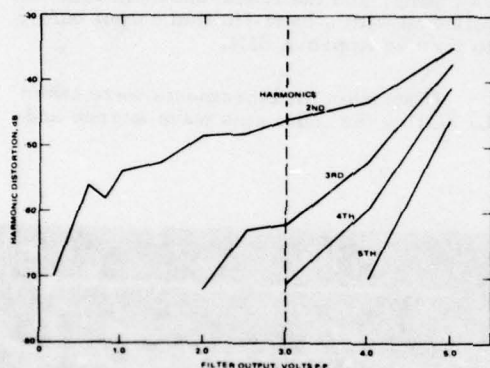
Figure 15. Harmonic distortion content in filter output at filter peak response frequency (for inputs at lower frequencies) vs filter output signal amplitude.

CONCLUSIONS

The operation of a fundamentally simple means for precision subtraction (DCS) on floating sense electrodes has been demonstrated and will open opportunities for a variety of charge transfer device structures and functions.

An optimized one-sided split electrode TVF design that eliminates unnecessary common-mode electrode structure and minimizes non-linear depletion capacitance has been demonstrated; it dislodges the output circuit from the position of dominant noise source in CCD transversal filters.

These schemes have been combined in a one-sided DCS matched filter with demonstrated input-noise-limited performance. The filter provides an rms signal-to-noise ratio of 91 db, 0.6 percent total harmonic distortion, and a subtraction common mode rejection ratio of 68 db. With the elimination of clock pickup, output circuit requirements have been simplified.

ACKNOWLEDGMENT

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Intensified CCD for Ultrafast Diagnostics*

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Abstract

Many of the present laser fusion diagnostics are recorded on either ultrafast streak cameras or on oscilloscopes. For those experiments in which a large volume of data is accumulated, direct computer processing of the information becomes important. We describe an approach which uses a RCA 52501 back-thinned CCD sensor to obtain direct electron readouts for both the streak camera and the CRT. Performance of the 100 GHz streak camera and the 4 GHz CRT are presented. Design parameters and computer interfacing for both systems are described in detail.

I. INTRODUCTION

Many present laser fusion diagnostics,[1] such as measurements of the laser beam, X-ray, neutron and alpha intensity vs time are recorded using either an ultrafast electronic streak camera or a wide bandwidth oscilloscope. The temporal resolution of these instruments ranges from the order of ten picoseconds for the optical and the X-ray streak cameras to a few nanoseconds for a neutron time-of-flight detector and recording system. A characteristic of most laser fusion experiments is the generation of a very large volume of data due to the many parameters that are simultaneously monitored. To perform these experiments quickly and efficiently, a diagnostic instrument used for laser fusion should be able to interface directly with a central computer, whereby direct data processing by the computer can be implemented.

The motivation behind the work described in this paper is based on the need to directly computerize existing laser fusion diagnostic instruments. The approach we have chosen is to use a back-thinned RCA 52501 charge-coupled device (CCD) to replace the normal phosphor in both an ultrafast streak tube and a wide bandwith cathode ray tube (CRT). The CCD is used to directly image the electrons generated by the respective instruments.

II. RCA 52501 CCD CHARACTERISTICS

It is important to determine the characteristics of the sensor in the mode in which the device is required to operate. For both the CRT and the streak camera instruments, the CCD sensor is used as a direct electron imager. The electron excitation time per CCD pixel ranges from a dc illumination condition during setup down to about ten picoseconds per pixel during actual data taking.

Figure 1a shows the response of a back-thinned ($\sim$ 10 μm thick) and back e-beam illuminated RCA 52501 CCD to 4, 5 and 6 keV energy electrons. For the case of the ultrafast streak[2] camera, the desired information is contained in the form of an intensity vs position profile. It is therefore necessary to determine whether the CCD sensor is linear (i.e. γ = 1) to input electron excitation and furthermore, to verify that this linearity is maintained when the input electron pulse duration is reduced to the picosecond range (i.e.

reciprocity is preserved).

Although the CCD data shown in Fig. 1a is derived using electron pulses in the microsecond range, similar experiments were performed using a 50 ps 1.06 μm coherent light source. If the assumption that the CCD is insensitive to the manner in which the electrons are produced is valid, then it can be concluded that the RCA 52501 CCD is linear to electron excitation and its reciprocity is maintained down to at least the 50 ps range. It should also be noted, however, that not all the CCD sensors have this desirable reciprocity property. For example, the Fairchild 202 CCD is linear in the dc illumination mode (i.e. γ = 1), but the sensor has a transfer function gamma value of 1.3 when a 50 picosecond light pulse is used. The deviation in sensor linearity was observed in all of the 202 and 211 CCDs tested. Since the RCA and Fairchild CCDs differ both in the chip's construction (i.e. surface vs buried channel) and in its architecture (i.e. frame vs interline transfer), it was not clear if either difference was the cause of the reciprocity failure. To help answer this question, we have obtained some preliminary data on the reciprocity behavior of an experimental RCA all buried channel CCD. Initial analysis indicates that both the RCA and Fairchild all buried channel CCDs exhibited reciprocity failure in the tens of picosecond time domain. No adequate theory has been forwarded to even suggest that the buried channel structure is responsible for the reciprocity failure. If indeed the buried channel device exhibits this reciprocity failure, then buried channel CCD sensor may not be applicable for ultrafast diagnostics.

In most ultrafast diagnostics, such as a 10 ps resolution streak camera or a 4 GHz CRT, some form of signal amplification is required to bring the output to a usable level. In the conventional case, where a phosphor is used to image the electrons, an optical or electron image intensifier, such as a microchannel plate, is used to increase the light output from the phosphor to a level suitable for film recording. In our case where the CCD is used in place of the phosphor, signal amplification is obtained by direct electron multiplication within the silicon. The CCD gain (G) can be calculated at room temperature by:

$$G = \left[\frac{E_{in} - E_{dead}}{3.66} \right] , \qquad \text{Eq. 1}$$

Where E_{in} is the incident electron energy and E_{dead} is the CCD back layer dead energy in eV. Figure 1b shows the CCD gain vs input electron energy result for the RCA 52501 CCD. Details of the technique used for the gain measurement are given elsewhere.[3] For comparison, a plot of the ideal gain curve is also shown where the E_{dead} energy in Eq. 1 is set equal to zero. Data for a Fairchild 202 CCD is also shown.

Typically for a S-1 photocathode streak camera when operating at a streak speed of 35 ps per mm, the maximum number of photoelectrons that each CCD pixel (30 μm x 30 μm) receives is on the order of 10^3 electrons. For the present RCA 52501 CCD, the full well capacity is between 5×10^5 to 1×10^6 electrons. Using these values, the CCD electron gain required for an ultrafast streak camera is between five hundred to one thousand. From Fig. 1b, this CCD gain value corresponds to an input electron energy of around 4 to 6 keV.

When the sensor is incorporated into an ultrafast CRT, the CCD output O_{CRT} in units of the number of electrons/pixel is given by:

$$O_{CRT} = 6.25 \times 10^{18} \cdot \left(\frac{E_{in} - E_{dead}}{3.66}\right)(i)\left(\frac{\Delta t}{N_{cell}}\right)\left(\frac{d_{cell}}{d_{spot}}\right)^2$$

Eq. 2

Where E_{in} and E_{dead} again are the input electron energy and the CCD dead layer energy respectively. The CRT beam current is denoted by i, and Δt is the total time required to sweep the electron beam across N_{cell} number of CCD cells. The diameter of the electron beam is given by d_{spot} and the CCD cell size is denoted by d_{cell}.

Figure 1c gives the blooming characteristics of the RCA 52501 CCD using a continuous incoherent 1.06 μm light source. The vertical anti-blooming characteristics has been optimized by adjusting the RCA CCD image section voltage ($V_{\phi AL}$) of the nonstoring electrodes so that they are in the accumulation condition (i.e. $V_{bb} > V_{\phi AL}$). The voltage on the storing electrodes ($V_{\phi AH}$) is arranged so as to obtain, during light integration, a well size in the image area smaller than or equal to any subsequent wells encountered in the A→B, B→C and C→output charge transfer process.

Although the CCD blooming data given in Fig. 1c was obtained using photon illum-

ination, similar qualitative experiments were also performed using electrons as the input excitation source. We have verified that the general CCD blooming characteristics are similar in either the electron-in or photon-in mode. These experiments tend to verify that CCD behavior, in most cases, is source-independent.

A good anti-blooming property is important in instruments such as a streak camera where severe localized sensor saturation can occur. With this anti-blooming characteristic, those portions of the streak data that are in close proximity to the highly saturated data will not be destroyed by the vertical blooming associated with many present CCD sensors.

The practicality of an intensified CCD instrument depends greatly on the useful lifetime of the sensor in the electron beam environment. The damage mechanism for a front e-beam illuminated CCD is well documented.[4] Briefly, this electron damage is induced by a non-uniform accumulation of positive charges in the SiO_2 insulator. This positive charge build-up is due to a difference in the electron and hole mobilities in SiO_2 while under the influence of the E-fields generated by the normal operation of the CCD. For the backside e-beam illumination case, the problem of the direct electron/hole pair production in the SiO_2 layer induced by the incident electrons is eliminated, since the electrons are no longer required to transverse the SiO_2 layer before reaching the Si. However, CCD damage can still occur by the indirect creation of the electron/hole pairs in the SiO_2 insulator via the soft Bremsstrahlung X-rays that are generated when the electrons impact into the Si.

Fig. 1d shows the experimental results of two CCDs under e-beam illumination. Both CCDs were operated using incident electron energies so as to obtain full well CCD outputs with both sensors having electron gain of 1000. The electron pulse density was equal for both the RCA and Fairchild CCDs, and typically this density was around one electron per square μm. It is clear from Fig. 1d that the electron-induced damage due to the front e-beam illuminated CCD (Fairchild 202) is many orders of magnitude greater than the back-illuminated device (RCA 52501). Translating these CCD damage data into practical operating time durations, the Fairchild 202 CCD will exhibit noticeable damage within one minute

of continuous electron exposure. In contrast, the RCA 52501 CCD yields no detectable sensor damage even after several weeks of continuous e-beam illumination. However, we assume, although not experimentally verified, that if the RCA 52501 CCD were illuminated from the front side, electron damage would occur in a time duration similar to the Fairchild 202 and 211 CCDs.

The vertical and horizontal spatial resolutions of the intensified CCD sensor are pertinent to both the streak camera and the CRT operations. Briefly, the ultrafast streak camera is used to measure the temporal light intensity profile of an event. The intensity vs time of the input light pulse is converted via the streak camera into intensity vs position on the CCD sensor. Basically, the streak camera can be viewed as an optical CRT in which the usual thermionic cathode is replaced by an optical photocathode and in which output intensity is recorded. In normal operation, an optical slit image is focussed onto the photocathode, and the resulting photoelectrons are focussed and swept across the CCD at a high speed. The CCD axes are aligned so that the streak tube sweep direction is parallel to the horizontal sensor axis. The horizontal resolution of the CCD therefore determines, in part, the temporal resolution of the streak camera. The vertical sensor resolution which is along the direction of the slit image will partly determine the maximum number of independent channels that the streak camera can monitor simultaneously.

Figure 2 shows the experimental results for the horizontal and vertical spatial resolutions of both the standard thick sensor and the special thinned (~ 10 μm) RCA 52501 CCD. The data were generated by imaging a standard Air Force resolution pattern using a 1.06 μm light source. The degradation of the horizontal spatial resolution at 1.06 μm wavelength for the thick CCD is due to the deep penetration of the photons into the silicon substrate. The resulting back thermo-diffusion of the electrons generated deep in the silicon to the front-side CCD wells results in the degraded horizontal resolution. A similar horizontal spatial degradation would be experienced if a thick CCD were used to image the electrons from the back side.

III. STREAK TUBE/CCD IMPLEMENTATION

Figure 3 shows a streak tube equipped with an internal CCD. The device consists of a RCA 73435 streak tube mated to a special RCA 52501 back-thinned and back e-beam illuminated CCD. The vacuum header in which the CCD is mounted is equipped with an optical window so as to enable an optical fat zero bias to be implemented from the nonvacuum side. During actual CCD operation, the storage area of the sensor is blocked so that neither the LED bias light nor the electron beam illuminate that area. The streak tube has a S-1 photocathode which utilizes a modified low temperature schedule to prevent degradation of the CCD sensor. Many of the CCD parameters, such as the dark current and inter-electrode leakage, were monitored before and after photocathode processing.

In the actual operation of the streak tube/CCD device, the photocathode voltage was lowered from the usual -17 kV at the cathode down to approximately -6 kV. This reduction of the operating voltage is required to maximize the dynamic range of the total system. To illustrate this concept more clearly, let us consider two extreme cases. In the first case, if the streak camera's photocathode is at a very high negative voltage, then an incident electron onto the CCD will produce a large number of electron/hole pairs; see Eq. 1.

In the extreme case, if one incident photoelectron saturates the CCD cell, then the system dynamic range for the streak camera/CCD instrument is reduced to unity. Now consider the opposite situation; if the streak tube's photocathode is at a very low negative voltage, then an incident electron onto the sensor yields a very small number of electron/hole pairs. Again, going to the extreme, if the incident electron energy is around the dead layer value (i.e. ~ 2 keV), then the sensor gain is near unity. The dynamic range in this condition is primarily governed by the maximum photocathode current density. For an S-1 photocathode, the maximum current density is about 1000 electrons per CCD pixel per 10 picoseconds. Hence for a 10 picosecond resolution system, the number of electrons available per CCD cell is 1000. The system dynamic range in this case is less than unity since the CCD electron equivalent noise for the RCA 52501 sensor is around 10^4 electrons. Between these two extremes, the streak tube/CCD

will not be limited by either photocathode saturation or by CCD well saturation, and reasonable dynamic range of several hundred can be obtained.

The streak camera/CCD data acquisition system consists of a LeCroy 8258 8-bit transient digitizer coupled to a multiplexed 192K dynamic local memory. The digitized data are processed by an LSI/11 computer through a standard CAMAC data highway. The processed data are stored on floppy disks for further analysis. A typical local LSI/11 processing consists of a point-by-point dark current subtraction followed by a CCD gain normalization. Both of the 320 x 256 point data for the dark current and sensor gain profile are stored on disk.

For most ultrafast diagnostics, system synchronization is very important. For the case of a streak camera, synchronization to the order of tens of picoseconds is generally required to prevent loss of data. This precise timing is usually provided either optically or electrically to the streak camera. For the CCD recording sensor, however, it is only necessary to time the CCD cycle such that the streak camera data are not deposited onto the sensor during the A to B transfer time, because during this time, the nonstoring CCD electrodes are brought out of accumulation and hence the sensor loses all of its anti-blooming characteristic. This rather relaxed timing requirement is implemented by phase-locking the CCD master clock to a low frequency pulse generated by the laser system's master computer. Any one of these pulses (~ 10 Hz) may be used to initiate the laser firing sequence; hence within a few microseconds after the timing pulse, the laser will generate data onto the CCD sensor. With appropriate delays, the streak camera data can always be arranged to arrive during the middle portion of the CCD integration cycle.

IV. CRT/CCD IMPLEMENTATION

Figure 4 shows a wide bandwidth CRT equipped with a CCD electron sensor. The device consists of a specially designed EG&G CRT coupled to an RCA back-thinned (~ 10 μm) 52501 CCD. The CRT deflection structure consists of a transmission line serpentine with an electrical characteristic impedance of 50 ohms. The serpentine deflection structure is designed to provide maximum signal deflection sensitivity by matching the signal phase velocity to the propagation velocity of a

5 kV electron.

The CRT/CCD is processed by baking the structure at 200°C for eight hours before cathode activation. The thermionic cathode is then aged for 24 hours to maximize and stabilize the current output. The CCD's optical imaging quality was monitored before and immediately after the processing cycle and was found to have degraded a slight amount.

The signal channel amplitude response of the CRT is shown in Fig. 5. The graph is a plot of the relative power required to deflect an electron beam vertically one centimeter at the CCD focal plain versus the frequency of the input signal. The variations of the deflection response are due to the many small local resonances of the various substructures of the deflection response are due to the many small local resonances of the various substructures of the deflection serpentine. The sensitivity of the deflection structure is measured to be approximately 10 volts per cm and the spot size at the CCD focus plane is about 200 μm. The axes of the CCD are aligned so that the signal deflection is parallel to the CCD vertical axis.

The data acquisition system required to support the CRT/CCD instrument can be identical to that described for the ultrafast streak camera/CCD system. In the CRT case, the dynamic range of the CRT/CCD is determined by the vertical spatial resolution rather than by the intensity of the electron beam. Because of this difference between the CRT and the streak camera, it is more economical to slow down the CCD scanning rate and to trade away the sensor's dynamic range, which in this case is not required, for a slower A/D and memory. In this manner it is possible to reduce the electronic system cost by a considerable amount.

In addition to the factor-of-four reduction of the CCD scanning speed, the electronics were further modified to provide a continuous scanning mode in which both the image and storage registers are clocked synchronously at all times. Both the usual image integration period and the fast A to B image transfer action of a normal T.V. mode were deleted. The remaining B to C transfer mode, in which the B shift register provides one CCD cell transfer for every 320 horizontal C shift register transfers, is extended, in the continuous mode,

to include the A image registers.

By changing the clocking scheme to the continuous mode, the system can now be used only in the pulsed illumination condition. The input pulse duration must be short, compared to the CCD vertical clocking period, in order for the sensor to exhibit good vertical resolution. This pulse duration requirement is, of course, easy to satisfy for the ultrafast CRT application, since the electron beam deposits its information onto the CCD in a few nanoseconds and the vertical clocking period for the slow scan case is in the order of tens of milliseconds.

The motivation behind using this continuous scanning technique is the ease in which the CCD can be synchronized to the external world. In this mode, the CCD is always shifting out the sensor's dark current and the external A/D is continuously digitizing the output. No memory storage is implemented until after the event time, upon which the next horizontal line clocked out by the CCD is, by definition, the first line of the picture. The memory will now commence to store the first and the subsequent 255 lines at which time a complete CCD picture is then obtained.

Note that unlike the previous phase-lock technique, no prewarning synchronization pulse is required to prepare the CCD for the data-taking sequence. However, this *continuous scanning mode*, by its very nature, prevents the implementation of the anti-blooming technique. This lack of anti-blooming ability is not important for the CRT/CCD operation, since the beam current of the CRTs can be adjusted to prevent sensor overload.

V. CONCLUSIONS

Two ultrafast laser fusion diagnostic instruments have been designed and fabricated which *incorporate a back-thinned RCA 52501* CCD sensor.

The RCA sensor has been characterized in the electron-in mode and provides relatively high gain at lower tube operating voltages. This reduced voltage can also allow effective increase deflection sensitivity in the streak tube.

In performance the 3 GHz response of the CRT was obtained.

The data acquisition system is designed to implement direct computer accessing and

processing for both the CRT/CCD and streak tube/CCD instruments.

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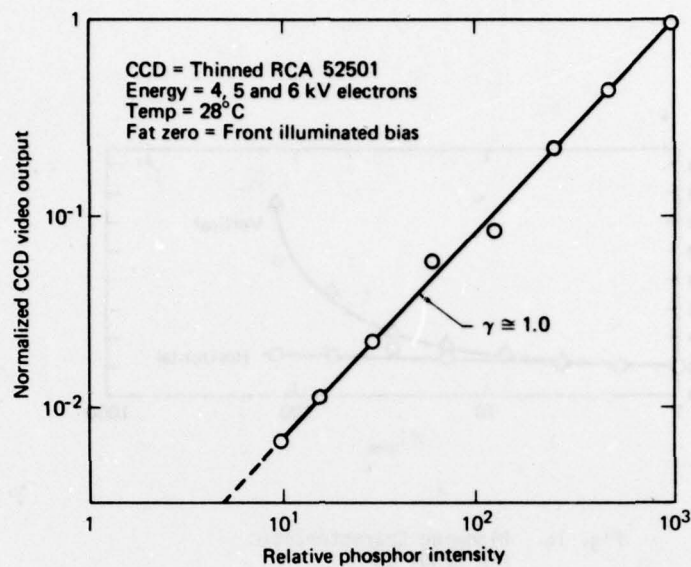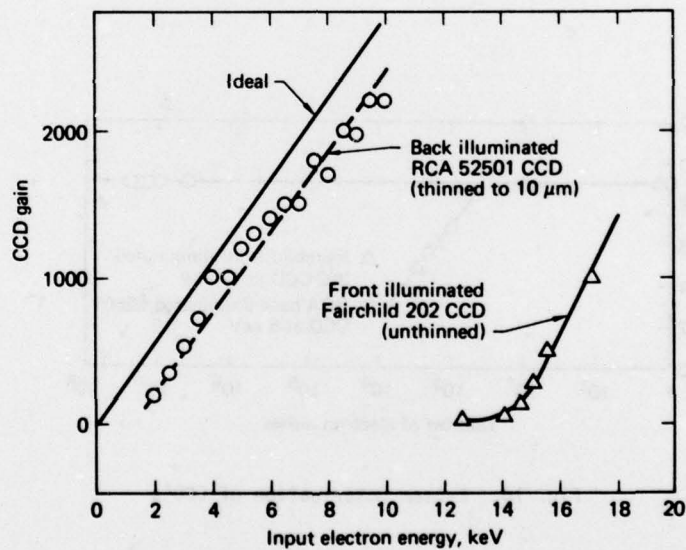
Fig. 1a. Signal Transfer Curve
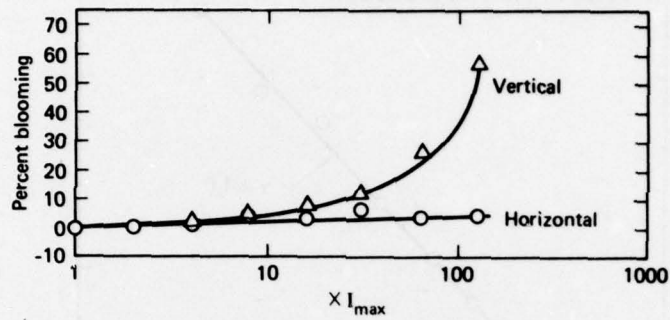

Fig. 1b. E-Beam Gain Curve
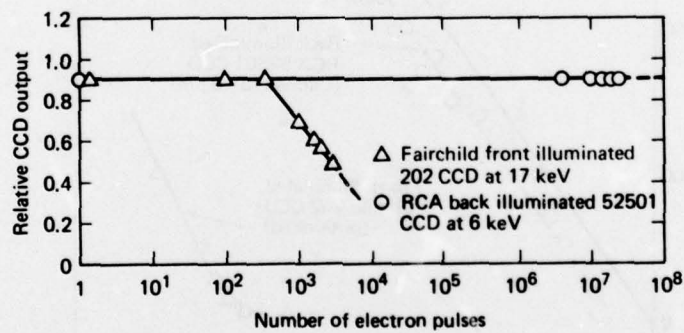
Fig. 1c. Blooming Characteristic
RCA 52501 CCD

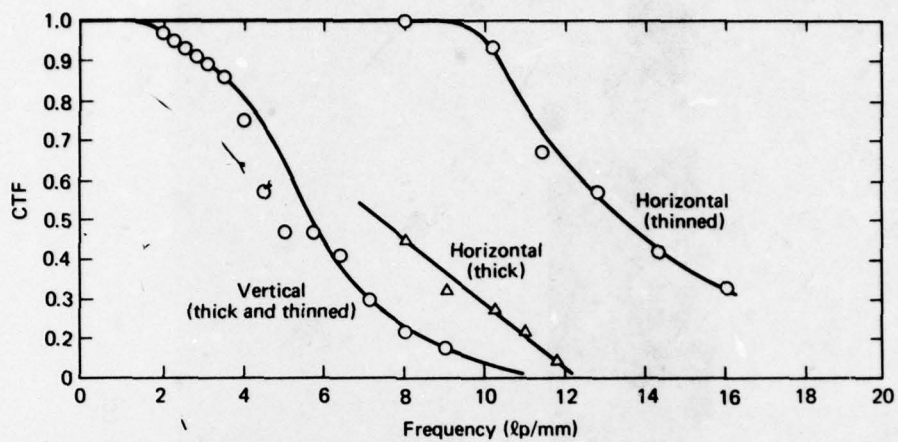

Fig. 1d. E-Beam Deterioation of CCD's

4-118

Fig. 2.   Frequency Response Curve CRT/CCD

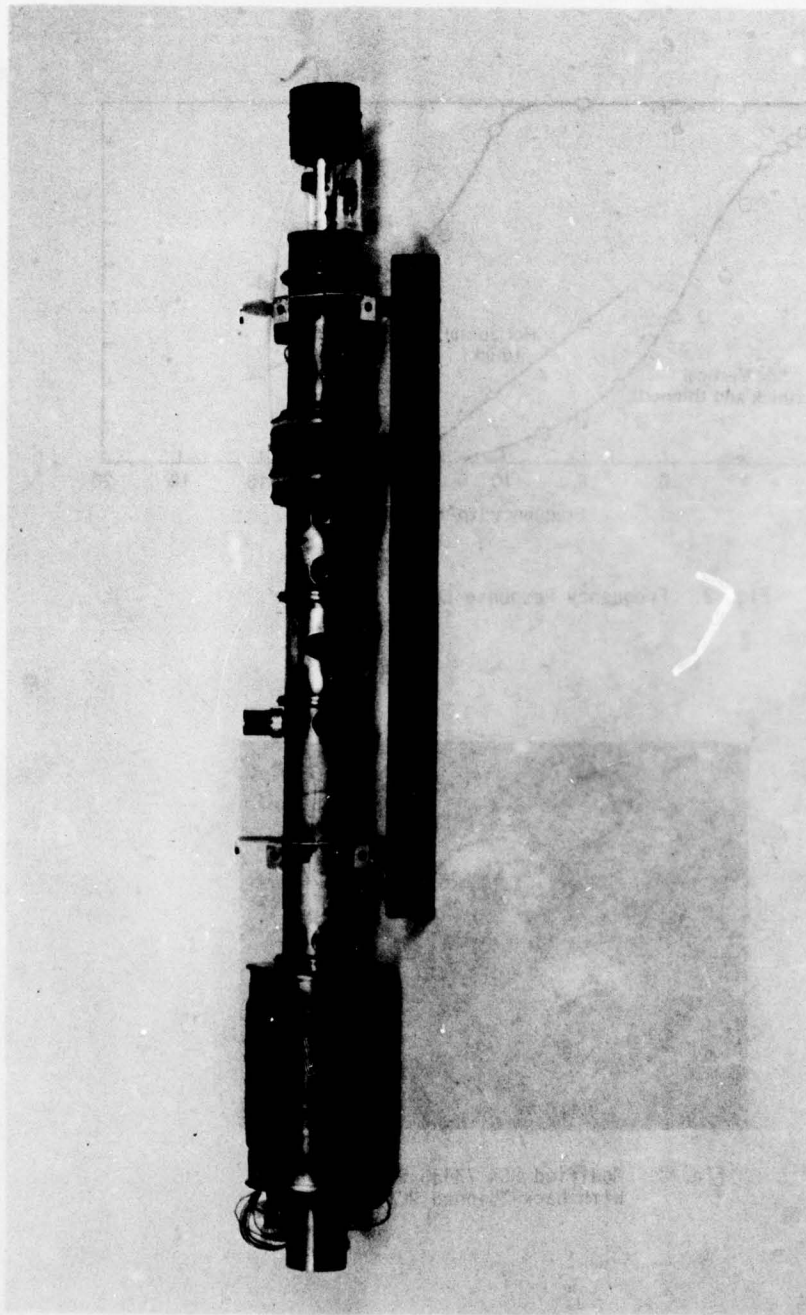Fig. 3.   Modified RCA 73435 Streak Tube
With Back-Thinned RCA 52501 CCD

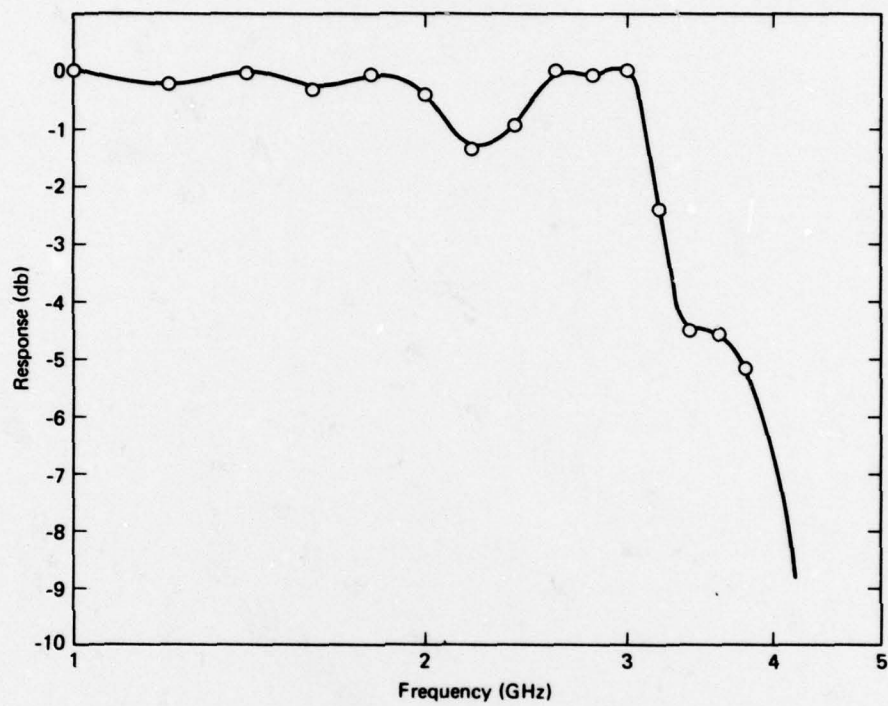Fig. 4. Modified EG&G CRT with RCA 52501 CCD

Fig. 5. Frequency Response Curve CRT/CCD

LOW FREQUENCY OPERATION OF NARROW BAND CCD TRANSVERSAL FILTERS

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ABSTRACT

The use of CCD's in acoustic signal processing applications requires large total time delays to obtain low frequency correlations. The maximum delay is ultimately limited by the storage time of the CCD well. This paper describes the performance of a 1.0 Hz low pass transversal filter with on chip delays in excess of one second. To achieve a 1.0 Hz passband with less than 1.0 dB band pass ripple and stopband suppression greater than 50 dB, the 101 filter stage filter was designed to be clocked at 100 Hz. The analytical design of the filter is further described, and measurements of device performance based on current available data are presented.

I. INTRODUCTION

Charge coupled device CCD delay lines can be used to accurately delay samples of analog signals. While it has been shown that CCD's operate well in the mid-frequency range (1.0 kHz < f < 10.0 mHz), measurements of their performance below 1.0 kHz have been previously neglected. However, this is the frequency region of interest in acoustic signal processing applications such as matched filtering or beamforming to optimize the detection of acoustic signals propagating through the ocean. The device discussed in this report was designed to operate at clock frequencies as low as 100.0 Hz, providing on chip time delays in excess of 1.0 second. A split electrode lowpass transversal filter was chosen as the vehical for this study because its design and operation are understood[1] for f > 1.0 kHz.

II. DEVICE DESCRIPTION

The CCD transversal filter chip shown in Fig. 1 contains two CCD delay lines compatible with the double layer polysilicon process. One delay line forms a .240" x .060" 1.0 Hz transversal filter using a set of tap weights to configure the split electrodes. The second delay line is .240" x .012" and exists primarily to can-

cel the differential mode clocking noise and dark current contribution to the main filter output. This auxiliary channel is also weighted and can be used as a 10.0 Hz lowpass filter without noise cancellation.

The tap weight coefficients were selected by a computer program which determined the best equi-ripple approximation to the (ideal) desired lowpass filter frequency response. The impulse response and therefore the weighting coefficients can then be determined by sampling the inverse discrete Fourier transform of the calcluated response. Several runs of this program have generated the set of curves in Fig. 2, relating the stopband suppression in dB (R) to the number of delay stages (N) and the transition bandwidth (bw_t) of such filters. A point of inflection of these curves occurs when

$$bw_t \sim \frac{1}{N\tau} \tag{1}$$

where τ is the delay per stage. This occurs because narrow band filters have transition bandwidths equal or greater than the filter bandpass. From Fig. 2, 101 stages were chosen to achieve 55 dB band stop suppression at the expense of a 200% transition bandwidth. It is interesting to note that for these filters should a transition at less than 100% be

desired, choices for N > 90 should be avoided as they have very little effect on R and thus only waste silicon real estate. The analytical frequency response due to the calculated weighting coefficients is shown in Fig. 3.

III. EXPERIMENTAL RESULTS

A photograh of the impulse response of the filter with f_c = 1.0 kHz is shown in Fig. 4, with the corresponding frequency response for f_c = 1.0 kHz and f = 438 Hz plotted in Fig. 5. The observed 3 dB cutoff for the curve with f_c = 1.0 kHz is $f_{3\ dB}/f_c$ = .0165 compared with the theoretical value of .0175. At the lower frequency, $f_{3\ dB}$ has shifted to $f_{3\ dB}/f_c$ = .0198 due to dark current contributions of the signal at lower frequencies. At higher input frequencies the rolloff becomes independent of the clock frequency.

The frequency response has not been measured at lower clock frequencies, nor the ultimate value of the stopband suppression been measured due to limitations in the technique used to obtain this preliminary data. The fact that $f_{3\ dB}$ is extremely close to the analytical value for both clock frequencies suggests the usefullness of this design approach for low frequency narrow passband filters. The measured band stop suppression R > 40 dB indicates these filters will be useful for the matched filtering applications discussed previously.

While the frequency response has not yet been obtained at f_c = 100.0 Hz, an estimate of the filter performance at this clock frequency is made by observing the output signal of the delay line as the total delay time on the chip t_d = nτ is increased. The result shown in Figs. 6a - 6c indicates that a useful output signal is detected from the output diffusion of the CCD delay line as t_d approaches 1.0 second.

IV. DISCUSSION

It is clear that CCD's can play a major role in obtaining analog delay even as the clock frequency is decreased and thus t_d increased to 1.0 sec. It can be expected in the future that as semiconductor material and IC processing improves, even long delay times will be possible without serious degradation of device performance.

Thus low frequency correlations to the tenths of Hz will become available.

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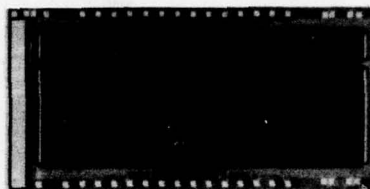1. R. D. Baertsch et. al. IEEE Trans. Elect. Dev., (Feb. 1976).
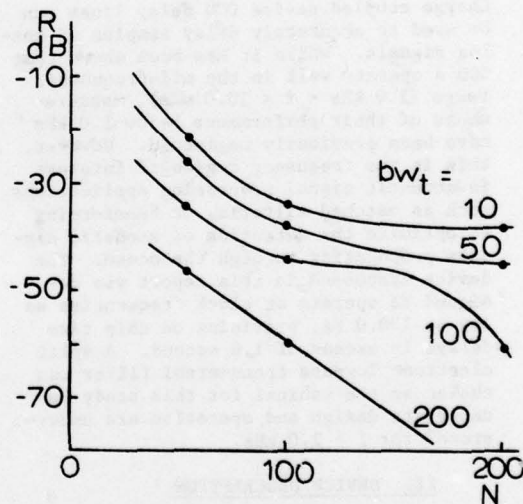
Fig. 1 The NOSC-013 Transversal Filter Chip

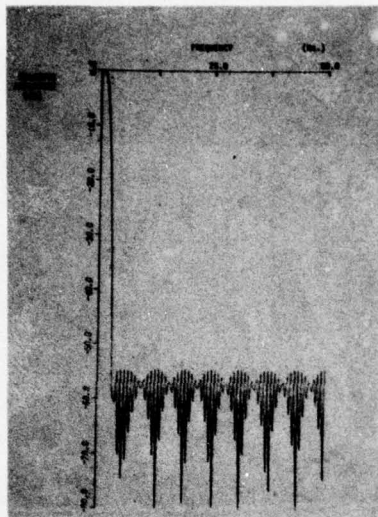Fig. 2 Narrow Band Filter Design Curves

Fig. 3   Low Pass Filter Analytical
Frequency Response
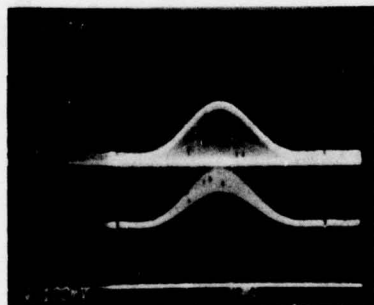

Fig. 5   Measured Frequency Response of the
Transversal Filter

Fig. 4   Transversal Filter Impulse Response,
f_c = 1.0 kHz

Fig. 6a   33.33 msec delay

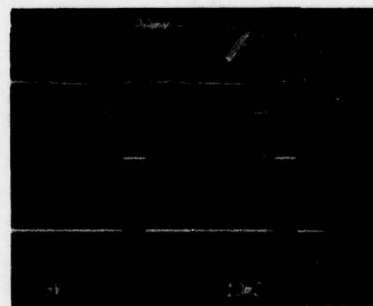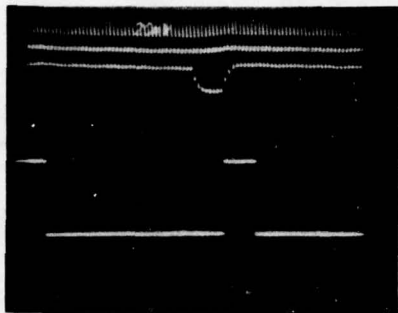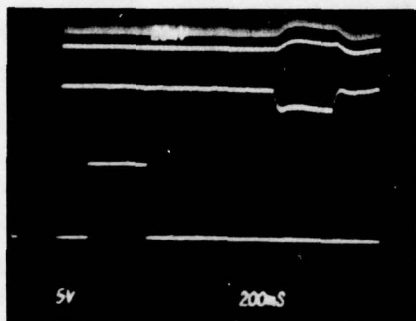**Fig. 6b 212.1 msec delay (2x input)**

Fig. 6c 1.01 second delay